

Date – 09/06/2011

Attendees: CJ Clark, Bill Tuthill, Brian Turmelle, Adam Cron, Adam Ley, Carl Barnhart, Dharma Konda, Francisco Russi, Roland Latvala, Craig Stephan, Roger Sowada, Carol Pyron, Ken Parker, Dave Dubberke, John Seibold, Bill Bruce, Peter Elias, Josh Ferry, Bill Eklow,

Missing with pre-excuse

Missing: Lee Whetsel, Neil Jacobson, Mike Richetti, Ted Cleggett, Matthias Kamm , Ted Eaton, Wim Driessen, Heiko Ehrenberg, John Braden,

Agenda:

- 1) **11:00** Patent Slides and Rules of Etiquette
- 2) ECID review
- 3) More on “Should CAPUPD be a standard cell “?”
- 4) More on PowerMUX from Friday
- 5) PDL Level 1
- 6) SAMPLE relaxation – is it ready?
- 7) Mixed R_F/R_A
- 8) Example Homework assignments

Meeting Called to order at 11:03 am EST

Minutes:

Review Patent Slide – Reminder sent out over email.

Solicited input from anybody who is aware of patents that might read on our standard.

No responses.

Review of Working Group Meeting Guidelines

Bill Bruce has joined the working group.

ECID Review

Carl has created a section fro the ECIDCODE Instruction

Publicly documented ECIDCODE will have the ECIDCODE instruction to be compliant

Vendor can’t call private ECID with ECIDCODE instruction

CJ asks what part of ECID code would be problematic

Bill E: do we need something at the die level.

Carl: this is at a per tap basis right now.

CJ : on a per tap basis having an ECID would show which taps are valid and working. Could be useful on a multitap die

Bill E: specifically referring to the “chip”. Do we want to expand it to “chip/die” or something similar.

Carl: can changed Electronic Chip Identifier to Electronic Component Identifier. Was using industry meaning of ECID.

Bill Bruce: if industry calls it “CHIP” than it should stay chip

Are any of these implemented with RFID?

Bill E: not yet. It is a good 5 years before this happened.

CJ: if it is RFID it’s not through JTAG.

Bill B: Need to make a rule for PDL proc

Carl: does it need to be in PDL

Carol: has to be PDL because that is what we are standardizing on it.

Carl will make the rule

CJ: does anyone else have a problem with ECID?

Bill B: how many Bits do these tend to be?

Carl: low hundreds

Dharma: is it a variable length

Carol: it is fixed for a given chip. It is in register access

Dharma: can be different between chips?

CJ: yes.. per BSDL for the chip.

Francisco: we might be rushing through ECID

CJ: this value is more a database lookup. Fields aren’t broken out on the silicon

Bill B: nothing about ECID type is the same for all chip types

Ken: where in BSDL will this go

Carl: put all instructions together. Immediately after device id and user code descriptions.

Bill E: will give this to the ASIC engineers and see if it will meet the specs from the vendors and is complete.

Bill B: how do I know this works.

CJ: Fixed bits to know what you are scanning out. If you are getting all 1’s or all 0’s you know..

Carl: the only thing you can verify is the length of the register

Bill B: use the capture field to make those bits valid in a certain places.

Bill E: end user should know what the value is and will know if it is invalid.

CJ: how do you know if you are not scanning back a legitimate value back?]

Bill E: send a list of all the ECIDs back to component supplier and get feedback if they are valid or not. The component supplier should know what the ECID should be

CJ: feedback loop is slow though. Too much time if you are sending back invalid numbers.

Carl: there is nothing that stops an Engineer from adding breadcrumb bits and using register attributes field to work with bread crumbs. Nothing preventing you.. just not mandatory.

John B: agrees with what Carl

Ken: add a recommendation

Francisco: would be nice if we had a ready bit.

CJ: non all 1’s or non all 0’s

CJ: Bill Bruce does having a recommendation satisfy your concerns?

Bill B: recommendation is better than nothing
Carl asks if there are any objections to adding the ECID text into the current draft?

Carol: existing chips will be able to put out new version of BSDL. What about existing ECIDs that don't meet this requirement?

Carl: private instruction

Carol: concerned about the word of public?

CJ: asks if there are any objects to bring it into the draft

No Objections noted.

Should CAPUPD be a standard cell

Connect the PO to the PI of the cell

Seems simple for the standard to identify CAPUPD

CJ: this is for clause 9 TDRs that are user defined

Carol: no problem with this being an option. Would like to say "self capture update"

CJ: say SelfMon instead of CapUpd? Good point

CJ: desirable implementation of NOPI.

CJ: add NoUpd

Ken: not suggesting a new BC Cell ?

Carl: no.. For register fields and register type assignment only

CJ: would be new keyword. CAPUPD. It is just a wire.

Bill B: purpose to support DEBUG?

CJ: for test. Ability to communicate to tools and end users.

CJ :Any Objections to adding this?

No objections noted.

Carl asks CJ for some descriptive text for a starting point

Francisco: no gated clock so there is no need for feedback loop?

Carl: correct.

CJ: note that the recommended design in clause 9 is not to have a gated clock.

Carol: why is a non gated clock desired here?

Carl: because that is the way people typically code and it involves distributing fewer signals. Makes no difference. You can do it either way, but it just a recommendation

PowerMux

CJ had presented PowerMux to the group on Friday

Not a SIB. Simple method of allowing a tool to understand what the length of the scan path is if a chain is taken out.

Adam C: thinks this is a good thing but doesn't need to be associated with Power. Could be contentious because 1687 is trying to do something similar.

CJ: different from 1687 is a different approach. We are doing it in BSDL

Josh: Altera uses a test data register to select another test data register. To define the scan chain

CJ: we don't support that and won't have support for that.

- **Meeting adjourned: 12:03 EST.**
Next Meeting: 9/20/2011 11:00 AM EST

0 Motions Made

HomeWork Status

John has passed his examples in to the working group. CJ is running them through the parser.

Carol – is still working on examples
Heiko is still working on examples.
CJ is still working on port assignments

Homework assignments.

Heiko and Carol's assignments are outstanding and will be done for next week's meeting

CJ will have examples of port assignments
Bill E – work on more concrete example and definition of the ESSID register

NOTES:

1149.1 working group website - <http://grouper.ieee.org/groups/1149/1/>

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JOIN the meeting as GUEST – will have to ask to present

Meeting time: Tuesdays 11:00 AM (EST) (Recurring)

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