

Date – May 11, 2010

Attendees: CJ Clark, Bill Tuthill, Carl Barnhart, Ken Parker, Adam Ley, Adam Cron, Wim Driessen, Roland Latvala, Francisco Russi, Dave Dubberke, Carol Pyron,

Missing with pre-excuse:

Missing: Bill Eklow, Heiko Ehrenberg, Ted Eaton

Agenda:

Continue discussion on INIT

Minutes:

There has been a large email discussion on whether or not INIT_SETUP needs to be mandatory if there is an INIT_RUN instruction. Currently the INIT discussions have allowed INIT_RUN to exist with INIT_SETUP being optional.

CJ - Documentation is important. Without side file describing initialization there is no documentation.

Carl – agrees.

Carl – issue seems to be with hardwired pins. If these pins are hard strapped, I don't care about init setup and just want to run INIT_RUN sequence.

CJ – no hard strapping defined in BSDL. So there are no guarantees that the board designer will correctly strap the pins. Doesn't like having pins control init states with no knowledge of what is really going on. Pins being set a certain way are a functional operation. Need an INIT_DATA bit to control logic the same as the pins so that we have a way to control the logic when pins are not connected.

Carol – with Carol's chips, they need compliance enable pins to be at a certain value to keep chip from being damaged.

Carol – Can't toggle pins during a given test. Will cause damage if they are toggled.

CJ – not trying to toggle pins, just trying to control them.

Carl – What Carol is describing are not 1149.1 pins. They are outside the JTAG standard.

Carl – making CE pins to make a fixed value. Non compliant to 1149.1

Carol – considered making linkage pins but no way to document how to set up pin.

CJ – how do you guarantee through documentation that the customer doesn't take advantage of using different power supplies?

Carol – state has to be fixed at power up.

CJ – what hardship would you have to put the MUX present and allowing the init to control

Carol – giving back door to user and can fry transistors. Rather have board designer strap the pin

Cj – on strapped functionally?

Carol – strapped period!! Same as VDD pin.

Carol – other aspect is time Zero. Need to have value set at time 0

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CJ - need side file to setup IO before driving data . gives clear documented way of how IO is set up

Carol – side file does not work with time zero

Carl – need to agree that this circuit that carol has to deal with is non compliant.

Anything that is programmable needs an init data override.

Carol – I/O can't have changeable voltage due to silicon type.

CJ –looking for a rule in the standard to put in INIT_DATA control. If you can't use the INIT_DATA bits to control the IO than the chip would be non compliant.

Ken – in the diagram of the receiver with 3 wires going in to it . What does the verb “strap” mean. (to make sure everyone is on the same page)

Carol – pin is tied on the board.

Ken – are they power and ground pins?

Carol – yes but can be configured differently so they can't be called power and ground.

Ken – of the 2 wires that we are going to strap.. Does this have to be done before power to receiver is turned on?

Carol – ramping sequence but yes

Ken – the 2 voltages should be there before receiver comes live.

Carol – yes.

Ken – as a test engineer I would need to be aware that those two pins need to be powered and stable before powering on chip. Nothing unusual about that . What is different is that we see more and more power sequencing and regulation built into the board itself.

Ken – so regardless, to test I need to observe this sequence or risk damage to chip.

Ken – so once power is on we do testing. Do we have a time zero requirement?

Carol – if the voltage SEL pin configuration mismatches what the voltages are, that is when you risk damage. That is why voltage selects can't be toggled when powered up

CJ – how sensitive are these mismatches?

Carol – if the I/O thinks it is at lower voltage that what it is supplied that is where the risk is. Will open the wrong gates and see wrong voltages and cause damage.

CJ – there is always the risk for damage if we don't know what we are doing. Not a unique situation.

CJ – question is can we put a “zero” on receiver (or high-z) to make it safe while setting voltage selects. Only after setup is complete will we change voltage going to Receiver.

Carol – could have non-frying default but can't guarantee that the correct voltage is supplied to receiver.

Carol – there are two forms of programmable I/O. Mission mode programmable and chip is locked down after programming.

Carol – have most features of the chip on INIT_DATA structure. Just couldn't see a way to safely add the voltage select pins to the INIT_DATA.

CJ – not comfortable with separate instructions for INIT - having INIT_RUN without INIT_SETUP.

Carol – wanted to be able have a parameter-less setup which didn't require INIT_SETUP. Wanted to be able to simply kick off an internal state machine to do setup without outside control.

Carl – INIT_RUN decode can be enough to kick off initialization sequence to put chip in “safe and cool” state.

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Carl – if we as a group want a rule for the initialization process the only source of parametric data for initialization of the chip from the init-data, I can support that. Carol's problem is outside of the domain of INIT_RUN. Carol's circumstance is more of a power sequence and not 1149.1 compliant.

Carol – agrees that there won't be INIT_DATA on voltage selects.

CJ – rather see rules written to call these out specifically what to do. Would like to see narrow rules that show what to do in situations like Carol's

Roland – agrees with Carl's summary. Not a Boundary scan issue but a power sequence issue.

Ken – if you call it a compliance enable you will need a BSDL for each configuration.

Carol – CE supports X's in BSDL file

Ken – bottom line if 2 signals are strapped. We can monitor the pins. If those pins are coming from somewhere, as part of a test, they need to be held appropriately so not to fry the device, and upstream part needs to be setup first. Points towards a power sequencing problem.

CJ – does your chip have a TRST pin?

Carol – yes.

CJ – there are some things that you can play with holding TRST low.

Meeting adjourned: 12:09 EST.

Next Meeting: Tuesday May 18, 2010 @ 11:00am EST

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.

1. Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1

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- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.