IEEE 1149.1 Boundary Scan Working Group Minutes

Date - 6/29/2010

Attendees: CJ Clark, Bill Tuthill, Wim Driessen, Ted Eaton, Carl Barnhart, Carol Pyron, Dave Dubberke, Adam Ley,

Missing with pre-excuse:

Missing: Bill Eklow, Roland Latvala, Heiko Ehrenberg, Ken Parker, Francisco Russi, Adam Cron

Agenda:
Address questions by Carl that he sent in email (6/26/2010)

Minutes:
Meeting started at 11:03am EST

(question #1)
CJ - Need to fit in BSDL language. Positional based vs. keyword based.
Carl – do we require all the unused bits in INIT_DATA or INIT_STATUSbe documented with fields.
CJ – we do not require all bits to have fields. We know the bits exist from BSDL
Carl – register INIT's name is a field.
CJ – not broken down into BSDL extensions.
Carl – not specify all bits in fields.
CJ – one could but not the normal flow.
CJ – using PDL, you would have iread/iwrite register name. it would really be an alias name to the register bit positions. Nothing wrong with setting the bits. But wouldn't normally do it.
Carl- we are allowing init_run and init_setup procs to allow someone to init_data(35)=1 can reference the field and register names in init_setup and init_run procs.
(question #2)

Carl – Do you have to have mnemonics for fields?
CJ – no. Carol's example is just examples of using mnemonics. Not required.
Carol – Side file can be 1 or 0's or mnemonics.
Carl – if not required. Setting a direction is not sufficient for Init Data register ? setting a direction on a mnemonic doesn't seem to work.
CJ – we are trying to provide a description in the standard on how to get data into the INITSETUP register.   Some of these things are getting into the area of preventing a user from doing something wrong.

(question #3)
CJ – have the ability of setting the direction through mnemonics through TDI/TDO or read/write. If the vendor doesn't supply the mnemonic. What does the standard do to help people.

Carl – this is just INIT DATA . Direction significant because if it is a capture it is capturing on a 1 to 1 basic. CJ has been adamant that we need to observe this. INIT DATA register is only TDR that has requirement to differentiate. Can't do that if we put the direction on the mnemonic. Doesn't see where putting the direction on the mnemonic name enough to give you the information. If the direction is on the mnemonic and the mnemonic isn't used than the BSDL doesn't know.

CJ – don't agree.

Carol – Chip Developer creates BSDL. Describe features of TDRs and give mnemonics. Register fields are inherently capture bits or update bits.   When in Capture mode (TDO mode) this is the mnemonic associated with these bits.   It's the register bit that needs to be described as capture/update (direction) not the mnemonic.

CJ – objective that we are concerned about is that someone might make a mistake in the side file and that they will try to read status on bits that are meant to update. And visa versa.

Carl – partial concern. Lots of BSDL. Needs to have enough info in BSDL for DFT synthesis tool to make connections.   Needs to be enough info for side file writing tool to write a file from scratch.

Carl – how do you describe the structure of the Chip to generate files automatically from BSDL.

Ted- want to generate verification vectors that do much better than just measure length. Want tool to figure out more than just the length of the TDR.

Carl – This will be something people attack. Information in BSDL.

Carol – point about the DFT synthesis is a valid point. BSDL guides the tools to generate other information.   \

CJ – not sure guidance is done with BSDL.

CJ – lets go back to Wim's suggestion. Attribute register_fields of TDI or TDO - Just trying to provide a simple check.

CJ – if this is a big care about and we need to know if it is a capture/capture-update/update lets describe it in some syntax.

 CJ – bigger picture – still in mind-set that BSDL is what we hand to people to read. With INIT operation we are trying to move the BSDL into a more machine readable format.   Not in the same camp that BSDL is the only thing that we provide.

Carl – the BSDL is the one thing that is specified by the Standard. We are breaking that mold by specifying a side file.

Wim – tools will help build side file. The name of mnemonic is not enough to build side file.

Carol – intends to add info field to the next revision.

CJ – need something equivalent to BC_1 style capture information.

Carl – if we have a field. Need a rule for INIT DATA to describe more information

Carl – INIT STATUS is a standard TDR. Register is capture-only.

Carol – correlation doesn't have to be bit for bit. Could have several bits in a row.

CJ – could do it in groups.

CJ – we should come up with a keyword where Carol had her TDI/TDO in BSDL example.

CJ – possibly use a value (keyword) to describe direction – CAP(capture)/ CAU(capture update) / UPD (update)
Carol – should make mnemonics have an input side or output side or both?

(Question #4)
CJ – what do we do with TDR bits that may appear in multiple TDRs
Carl- won't allow fields to be shared between registers?
CJ – no. we allow it. But there is no coordination that says that these are the same bits.

Meeting adjourned: 11:56am EST.

Next Meeting: 11:00am EST

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.
1   Observe only. –   Ken and Carl
1.   Directionality linkage. - CJ
2.   Power Pins. - Heiko
3.   Pairing power pins with functional I/O - CJ
4.   Sample / Capture. – Carol (Freescale) & Roland
5.   TRST included in PCB level diagram. – Adam L.
6.   Slow to Fall/Rise signaling issue – CJ
7.   "No Connect" – Ken and Francisco.
8.   Device ID – Still needs work
9.   Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:
- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.