IEEE 1149.1 Boundary Scan Working Group Minutes

Date – 9/21/2010

Attendees: CJ Clark, Bill Tuthill, Brian Turmelle, Ken Parker, Craig Stephan, Carl Barnhart, Dave Dubberke, Francisco Russi, Adam Ley, Roland Latvala, Heiko Ehrenberg,

Missing with pre-excuse: Carol Pyron,

Missing: Neil Jacobson, Ted Eaton, Bill Eklow, Adam Cron, Wim Driessen,

Agenda:

1) 11-11:15   Register Attributes

   [<register mnemonic description>] (see B.8.17, page 46

    [<register fields description>] (see B.8.18, page 46)

   [<register fields association description>]   (see B.8.19, page 46)

2) 11:15 – 11:40   SAMPLE – Any conclusion?

3) 11:40 -12:00   Reset and (StickyClamp?)

Meeting Called to order at 11:13 am EST

Minutes:

CJ - How often can you have register mnemonic and register field attributes
        If we have mnemonics we don't want to have collisions. Allowed to have
        PASS/FAIL/DONE/ etc . you can use it multiple times in the package files.
        But to allow checking across multiple register attributes is not where we want to
go.
        Correct approach would be to bring in mnemonic into package file from BSDL.
        Should be [ ] so it can be optional

Adam L. Semantically there is no difference between having multiple declared attributes
and have a string concatenated with the &
        Doesn't have an opinion either way.
        Already have to deal with multiples due to strings in the packages. Seems like an
arbitrary constraint
CJ – Correct. But not user friendly. Agree that we can have multiple register attributes
and can parse them the same way as strings.   But in terms of human, when you allow

multiple attributes, it promotes grabbing data from one BSDL to another and could cause problems.

CJ - By using a single register mnemonic and not allowing cut and paste and it has to be put into the package file, now the mnemonic is isolated in the package and checking is only in the package.

Adam L. – if the user doesn't understand that mnemonics have to be unique in the BSDL scope they won't understand to use package files.

CJ – good point .. sure

Ken – The person who is doing the cutting and pasting is probably at the IC vendor. So it is descriptive guidance issue??

CJ – Not sure we are guaranteed that it is the IC vendor.

Ken – Someone is cutting and pasting is the problem. Syntax errors that don't understand or correct syntax and wrong semantics. This will lead to mayhem.

CJ – hope it doesn't get that far. The compiler should flag that.
         Would rather just seem them in the package file to avoid the mayhem.

Adam L- arguments for dropping the multiplicity of attributes are not strong, but would be happy to propose the multiplicity for consistency with who they appear in legacy.

CJ – not cast in concrete . wanted to bring it up, and if it doesn't work than we can change it.

Adam L- no objection to have them single.

Carl – Push for multiplicity originally due to looking at package files as includes. This was already a multiplicity. One in BSDL and one in package. No strong reason to have multiples

Will withdraw suggestion as well. Happy to have singletons in the BSDLs and Package.

SAMPLE

CJ – 3 & 4 were possible things that could be managed.
         Bothered by having Cell on single ended side of receiver is optional in Dot6.

If you remove sample requirement, you take away any possible method of seeing simple things like seeing data at the chip.
         Functional resources may not be there.
         Makes for difficult area to test and understand if sample is removed. If you have sample you can have a method to see if the data is coming in.

Roland – when we went to dot6, the test receiver was fully sufficient to do jtag testing, for EXTEST and other requirements.
         It was an optional requirement for dot6 and the sample was not included. This has caused a little problem.

Carl – intend to bring if the sample is optional up in Dot6. The one time that cell that doesn't make sense is if you have on chip bypass/coupling capacitors and can't be bypassed. Nothing of worth can be sampled.

Roland – if you are just looking at toggle at mission rates, you can use the cell for sample. Not for EXTEST.

CJ – to do Dot6 you need a special driver that does Dot6.   Doesn't matter if it is on chip or off chip, but Extest makes no sense in this mode, but sample should still be there. Roland – that was their position was to sample from mission mode and Extest from Dot6 transceiver.

Ken –B7-B11. Table of legal capture source in 2001 spec
        Can we add new L's for sample.
        B7 – sample is only allowed to describe PI for bidir or clock. If we added L for
CJ – on observe cells you can sample x,1,0, but not on required cells.

Roland – Can you deprecate EXTEST on the mission receiver?
Carl – looked at that in Dot6

CJ – when you can bypass the on chip caps,
Carl – then you need to support EXTEST in mission receiver. And that would be the recommendation.
CJ – not in standard yet.
Carl – needs to be revisited by Dot6 team. Biggest area to look at .
CJ – bypass the caps on receiver for on chip AC coupling and setting common mode voltage for transmitter 0, you can go back to DC type test.
Carl – Dot1 needs to set a stake in the ground and thinks that the cell should be required for dot1
Roland in reality the caps are external or in series internal. More than likely an external caps. Can't just bypass caps.
Roland – could have external and internal caps.
CJ- why is that. Not large enough. Internal values.
Roland- not sure will have to look
CJ – mistake to remove the Sample Cell from

Reset

Ken – Bring back the question if we need a "RESTORE" instruction. TAP based mechanism to restore reset condition.
        State of board is ok for testing but not ok for resuming boot process.
        Restore would start up process as if it saw a reset.
        If you don't have a reset pin to access or a nail than a tap based way to implement it. Such as a reserved Opcode.
Wants to remember that we brought this up and maybe we need to revisit
Should it be mandated it ex
Adam l - would support it. Should it be a mandatory instruction?
Ken – that is the question
CJ – is there a target register? Do we want to support multiple reset?
        All for it.
Ken – allow leeway with the designers to define how many resets.

CJ- hard to know where the reset should be used. Definitely with INIT. LogicBIST and BISR, would want to use instruction to cause a reset. Feels it should go beyond INIT. Just doing EXTEST, there are values going into Core logic what disturbs functionality. Would serve many purposes.

Ken - maybe give it a prefix to tie it to INIT family. Not married to any of these naming ideas
        Call it INIT-RESET?
CJ – can you use the status register.
Ken – maybe. Doesn't need to be unique.

CJ – feels it goes beyond the INIT procedure.
Ken – maybe break up RESETS. And do all resets would be general reboot?
        Bottom line is not to jump through too many hoops to reset the chip.

CJ – make a place for it in INIT area and Ken can help make semantics. Sees it as a must have.
CJ – need Sticky Clamp as well.
Roland – target register fro RESTORE be resettable as well?
        Can't effect normal mission operation.
Ken – goal is that it should start you towards normal operation and no affect after wards.
Carl – has some objections and would move them to email

Sticky clamp. Persistent. So you can access other things while clamp remains.
Hand in hand with reset.
Holds IO in a permanent state while you load other tests or instructions. And then use RESET instruction to take it out of sticky clamp.
Now CLAMP goes away after you load another instruction.

Maybe new instructions have a CLAMP like behavior.
INIT RUN has clamp like behavior.
How do we get out of the Clamp Like behavior is the key.

Meeting adjourned: 12:12EST.

Next Meeting: 9/28/2010 11:00 AM EST

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.
1   Observe only. –   Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:
- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.