

Date – 11/30/2010

Attendees: CJ Clark, Bill Tuthill, Carl Barnhart, Adam Cron, Ken Parker, Francisco Russi, Craig Stephan, Heiko Ehrenberg, Mike Richettie, Adam Ley, Dave Dubberke, Carol Pyron, Wim Driessen ,

Missing with pre-excuse Brian Turmelle,

Missing : Roland Latvala, Lee Whetsel, Ted Eaton, Neil Jacobson, Bill Eklow

Agenda:

- 1) Required Patent Disclosure Slides
- 2) Wrap up of clamp_hold/clamp_release
- 3) New Business, if any

Meeting Called to order at 11:00 am EST

Minutes:

Reviewed Patent Disclosure Slide

Wrap up of Clamp_hold/Clamp_release

Francisco brings up his comments which he had sent out in email prior to the meeting

Francisco : Document was hard to read. Descriptions should be put up front rather than at the end. This would help the readability of document.

State diagrams X.1 should show transitions

Carl: text shows transitions conditions.. there is more than just a single signal going from 0 to 1 or 1 to 0. It is a full instruction decode.

CJ: only can show the 1 and 0 when you have a single signal. Here we are showing instructions becoming valid changing the states.

Francisco: picture depicting this or state diagram? Concerned maybe we should show picture to describe the implementation

CJ: will be different implementations of instructions registers.

Need to show the FlipFlop.

Carl: didn't add the FF into the DOC. Did not have time to add this figure.

CJ: can do it many ways. Don't want to restrict anyone to a single implementation

KPP: don't have a figure yet. We do show some possible implementations.. and want to complete this Annex to contain that

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CJ: x.1 section is normally description section.

Need description of instructions in instruction section.

Carl: why would you put the circuit prior to rules. Doesn't make sense.

KPP: Is CJ or Carl adding text to draft from ClampHold/ClampRelease doc?

CJ: is happy to do it. Would like some help with the figure that needs to be added.

Carol: will work with CJ to get figure into draft.

CJ: will put figure in description before the rules.

KPP: Is CJ or Carl tweaking info that comes in

CJ: is tweaking.

Carl: at this point changes go to CJ rather to Carl.

KPP: can comment on new draft?

CJ: hopefully have edited version out before Friday.

Carol: doesn't have Visio.

Carl: will volunteer to make figure in Visio if Carol sends something

CJ: has created a merged document of the draft in word. No longer a document hierarchy because it doesn't work in Microsoft correctly. Don't know of any other standard using sub documents.

Document is also in the latest version of Word. (docx)

Carl: question on INIT. Has there been any progress on BNF and PDL?

CJ: progress is that we would like to keep register assembly separate. To make it complete hierarchy puts a burden on the parsing and forces everyone to support it.

Will send document over for everyone.. Idea is to not mix both modes together.

When putting the bits together you have to have it pre-declared in the package file. Can't call it out in the middle of the assembly.

One other change would be to have as many attributes in the BSDL file. They just end up getting concatenated in the file. Will remove that restriction in the BNF. This Reverses CJ's earlier decision to not do it this way.

CJ: haven't done anything with the PDL yet. PDL needs the ability to add an instruction. Will need a "-ir" added to allow people to load different instructions.

Carol: any drive to push our PDL back into 1687 group to make it into their PDL.

CJ: will do this but too early. Need to define it more first.

KPP: what are we going to do with the IC_RESET? Still an open topic

CJ: need to get the rules down and incorporate it into the doc

Carl: don't have a consensus on what it is yet?

Carol: writing it down will help that

KPP: Where do we think we are? Originally proposed it as a tap based way to press the reset button.. Also through it would change the persistent as well. If it was an annex it would have to mention that the persistence diagram would have another arch in it.

CJ: one thing we didn't converge on yet is that it is a ClampRelease aspect to IC_RESET. Clamp persistence would stay on after IC_RESET

KPP: IC would be something that would remove all the clamping and start the Reset processes.

CJ: to get that affect would be a ClampRelease and then an IC_RESET.

KPP: two modes.. IC_RESET by itself would keep it in ClampHold state. And then ClampRelease and then IC_RESET would bring it back to a normal state.

Would have to write it up that way.

CJ: Sees it as 2 modes - IC_RESET with release. IC_RESET without.

Carl: one suggestion to take care of this was to have IC_RESET have a TDR that would select what would get reset. The TDR could include a bit for persistence.

CJ: right I can see the bit. Or do we want one way to guarantee that everything gets reset.

Carol: our reset sequences are complicated. Depends on your definition of Reset.

Freescall has reset state-machine with 36 states in one of the chips.

CJ: all we want to do is to mimic the yanking of main reset pin.

Carol : Our doesn't doesn't have a single reset pin that resets all of logic

CJ: If we are mimicking external reset pin might be too complicated to have a multibit TDR

Carol: a multibit TDR will give more freedom to reset. Include documentation on TDR an it would be ok.

CJ: what do I get as a benefit to have mutlibit TDR? Would need to understand resets from one on-chip test to another . Not sure we have the ability to describe that.

Carol: isn't really advocating either way. But sees it more as a tradeoff between flexibility and complexity.

Mike: AMD has complex reset. AMD's chips have private instructions that do something like this. Doesn't do hard or cold reset. That is accomplished by yanking pins. We have instructions that do partial resets. May just do jtag reset or functional reset. This is done to save time.

Sees value in a having a mutibit TDR. Could have one bit that is a hard reset.

KPP: could you explain what some of the more complicated resets are?

Mike: just partially resetting things instead of going through full reset.

KPP: this is useful for internal chip testing?

Mike: yes. This functionality is not for the outside world to use.

CJ: thinks the test engineer would be confused as to knowing which bits in the TDR to use to clear the chip. The test engineer doesn't know the layout of the chip and which bit needs to be set for

Adam C: feels that if the issue comes down to documentation and 100 bits that do 100 different things than it will be too hard for the user to know what it does.

In favor for an IC RESET command, but if there is a whole lot of documentation that goes along with it, it will be useless as no one will want to deal with the documentation.

Carol: thinks a multibit tdr with a minimum of 1 bit would be a good compromise. First bit is all reset. Other bits for partial resets

Carl: like the idea of mutibit TDR. Sees a case where you wouldn't want to fool around with PLL,

Sees this discussion comes to be the same as Init_data Bits. Test engineer shouldn't have to know about all this, but would have to be provided procs that would guide him to the right resets.

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CJ: feels that the general consensus for IC_RESET is for a multibit TDR where one bit is a HardReset and other bits are user defined.

KPP: Wants the hard Reset to be the LSB of the TDR.

Meeting adjourned: 12:00 EST.

Next Meeting: 12/7/2010 11:00 AM EST

NOTES:

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.

1. Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.

Weekly 1149.1 Meeting coordinates

1. Please join my meeting.

<https://www1.gotomeeting.com/join/172495048>

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United States: +1 516 453 0012
Meeting ID: 172-495-048
Audio PIN: Shown after joining the meeting

2. Other call in numbers

Australia: +61 (0) 8 6365 4094
Canada: +1 416 800 9290
Germany: +49 (0) 898 7806 6462
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