

**Date – 02/01/2011**

**Attendees:** CJ Clark, Bill Tuthill, Adam Cron, Craig Stephan, , Ken Parker, Carl Barnhart, Dave Dubberke, Wim Driessen, Brian Turmelle, Heiko Ehrenberg, Carol Pyron, Ted Eaton, Francisco Russi, Roland Latvala, John Braden, Adam Ley,

**Missing with pre-excuse** Mike Richetti

**Missing:** Lee Whetsel, Neil Jacobson, Bill Eklow,

**Agenda:**

- 1) Required Patent Disclosure Slides
- 2) Editor Status
  - a.) Update on web
  - b.) Input on new draft
- 3) IC\_RESET – new figures/strawman
  1. Updated figure (sent prior to meeting)
  2. Where is updated strawman doc (members have given feedback which hasn't been shared)
  3. Adam Ley – report on 1149.7 use of reset
- 4) New Business

**Meeting Called to order at 11:00 am EST**

**Minutes:**

Patent Slides shown and reviewed

Editor status essentially unchanged. Carl has generated and will post the clean and Dec-Jan diff documents. Will start email review process by section as soon as IC\_RESET can be added to the document.

**IC\_RESET**

- CJ presented and explained the revised figures.
- Ted objected to dropping the second bit of the Clamp/Test Persistence controller (TPC/CPC) providing separate control of blocking Test-Logic-Reset signal to TDRs without forcing CLAMP.
- CJ asserted that the same thing could be achieved by using a “local” TDR bit as shown in PRBC example. The “local” TDR bit could override the mode signal for any and all ports, if desired. Other people don't want functional pins active.
- Ted: If we build the TPC/CPC with two TDR bits, we get the added flexibility.
- CJ: We are trying to get to universal or even mandatory CLAMP for various users.
- Ted: Nothing is lost by changing the “sticky” bit to a TDR and providing for the two functions (blocking TLR resets and holding CLAMP mode) separately.
- CJ: That approach ruins Clamp\_Hold for everyone else.
- Ted: Making the Clamp\_Hold bit a TDR bit doesn't ruin or change anything.

- Adam: Separating control of TLR and CLAMP mode has advantages.
- CJ: Separating the functions ruins Clamp\_Hold.
- Ted: Why? I don't believe it does.
- CJ: I don't want Clamp\_Hold without TLR reset blocking.
- Ted: Agreed; that can be handled by a rule. the two bits only allow three states: no test persistence in effect, TLR resets are blocked but Clamp\_Hold mode is not asserted, and both TLR resets are blocked and Clamp\_Hold mode is held.
- Carl: The two functions are orthogonal.
- CJ: With the current definition of Clamp\_Hold, a user is forced to implement a local control to override the Clamp\_Hold for particular pins if needed. By separating the functions, you eliminate this need and user will not implement local controls.
- Ken: I'm confused. Allowing a local control to affect all bits destroys Clamp\_Hold.
- Carol: TLR would remove (reset, clear) the local control bit.
- CJ: Well, TLR could reset all bits in the example PRBS TDR.
- Adam: TLR is not mandated for user TDRs. It is the instruction decode that provides the override and would prevent the local TDR bit from having any effect when the user instruction is not. I still assert that it makes sense to block TLR separately from Clamp\_Hold.
- CJ: Local control is what is important.
- John: We do not need to define local control in the rules because it only applies to user instructions.
- CJ: Yes, this PRBS drawing is just an example of what a user could do.
- Ken: So private instructions can override Clamp\_Hold, but we need ot make sure this is just an example.
- John: For standard instructions, all pins remain clamped.
- Ken: Also, loading a standard instruction restores clamp behavior if it was broken by a user instruction.
- Ted: Wat is the argument against separate control of TLR reset and CLAMP behavior?

**Meeting adjourned: 12:10 EST.**

**Next Meeting:** 2/8/2011 11:00 AM EST

NOTES:

**Current Issues listed and who will champion that issue.**

1. Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ

## IEEE 1149.1- 2011 Boundary Scan Working Group Minutes

4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

### Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.

### Weekly 1149.1 Meeting coordinates

1. Please join my meeting.

<https://www1.gotomeeting.com/join/172495048>

United States: +1 516 453 0012

Meeting ID: 172-495-048

Audio PIN: Shown after joining the meeting

2. Other call in numbers

Australia: +61 (0) 8 6365 4094

Canada: +1 416 800 9290

Germany: +49 (0) 898 7806 6462

Netherlands: +31 (0) 208 080 380

Sweden: +46 (0) 852 503 470

United Kingdom: +44 (0) 203 051 4835