Date – 03/15/2011

Attendees: CJ Clark, Bill Tuthill, Adam Ley, Carl Barnhart, Craig Stephan, Carol Pyron, Roland Latvala, Brian Turmelle, John Braden, Bill Eklow,

Missing with pre-excuse Ken Parker, Adam Cron, Wim Driessen,

Missing: Lee Whetsel, Neil Jacobson, Ted Eaton, Mike Richetti, Dave Dubberke, Heiko Ehrenberg, Francisco Russi, Ted Cleggett,

Agenda:

1) Patent slides
2) Further review of Clause 6, 7 and 8

Meeting Called to order at 11:00 am EST
Minutes:

Review Patent Slide

8.19 and 8.20 still are being reviewed
Carol would like change to add
Carl makes a motion to adopt for changes to date for clause 8.1-8.18 with option to change later

Carol raises the question if we are at a quorum.
The count shows we are

Motion to adopt changes made to date to Clause 8 sections 1-18 into draft without prejudice to future discussion or future changes.

Carol seconds
No one opposed
Motion passes

John: Does PDL get maintained in 1149.1 or 1687?
CJ: Both will have to as there are some differences in 11.49.1
John: concerned in keeping them in sync
Bill E: are there going to be extensions to the PDL for 1149.1?
CJ:
John: 1687 is still a P standard?
CJ: yes.. CJ is on the 1687 group and will keep them synced up
CJ goes through some of the differences
iReset: 1687 no discussion about passing parameters into iReset. Would be useful for 1149.1

iApply. No instruction loading in 1687. All iAppy s are targeting a test data register. 1149.1 have built in tdrs for instructions
option toallow a parameter to be passed to load an instruction
iEndState: was in 1687 but now missing. Might be useful for us to adopt to be able to end in a certain state.
iClock/iClockOverride: might not care about them in 1149.1 and might not want to carry them
iProc: wrapper around a procedure. Works with iCall and iTarget
Carol : is the pdl a proper subset of 1687 PDL or is it a subset with a few extensions.
CJ: suggests that it is the same as 1687. Would support all commands. Add-ons (support for parameters) might be added to 1687.
Carol: the PDL has multiple levels?
iRead/iWrite of boundary registries with PreLoad or Extest and was not a concept in 1687. Is that here in this list.
CJ: Addressed in comment about iApply with parameter. In 1687 instructions are loaded based on TDR. The tool will figure it out. But it assumes that there is only one instruction per data register. Not the case with Sample/Preload/Extest on Boundary Register. Has added instruction parameter <IR> to iApply
CJ: Levels – We would only support level 0 PDL. 1687 has PDL – Level 0 and PDL – Level 1 (TCL)
Carol: Just curious because only mentioned Level 0 before and was wondering if we were going to add Level 1
CJ: Only showing Level 0 and only plan on using Level 0
CJ: iPDLLevel Key word may not want to be carried in 1149.1
Carol: Keep keyword but fix level parameter to be 0
CJ: agrees with that
Carl: fix 1149.1 as version as well
Bill E: would anticipate that the .1 standard will go to ballot before 1687. Not sure you want to tie references to 1687 in 1149.1 as 1687 isn't a standard yet.
CJ: goal will be not to have any references to 1687
Bill E: Thinks that after 1687 gets approved there should be some addendum to 1149.1 standard to link the PDL to 1687 standard

CJ walks through PDL section to describe the changes and additions that he made.
Carl: One of the big issues of InitSetup and InitRun that we had to be careful about was that we were able to identify that something applied to a specific instances to a specific chip to a specific board. Not sure how I target the correct path here with PDL
CJ: it is the iTarget command used to do that. Tells the tool the scope of a particular PROC.
CJ feels that the use model is easer in 1149.1 and will work on making one.
CJ: points out that 1687 allows iRead/iWrite to be a register or pin. In 1149.1 sees the targets being registers and not pins.
Carl: in InitSetup we did have rules that allowed InitData register to read pins so that the software could verify that the pins were set correctly before moving to Extest.
CJ: so do you think we need to keep the ability to have both registers and pins

Carl: port is translated to a bit of a TDR. So the iRead is reading the TDR but some of the bits are defined as ports.
Carl: talks himself of needing pins for iRead/iWrite and withdraws the comment.
CJ will take another week to clean up PDL section before sending it out.
Carl asks CJ if register extensions are done?
CJ still have a ways to go and working on PDL first then get the BSDL straightened out

Meeting adjourned: 12:00 EST.

Next Meeting: 3/22/2011 11:00 AM EST

Motions Made and Seconded

- **To adopt changes made to date to Clause 8 sections 1-18 into draft without prejudice to future discussion or future changes.**
  - **Seconded**
  - **Motion passes unopposed**

NOTES:

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Current Issues listed and who will champion that issue.

1 Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.