IEEE 1149.1- 2011 Boundary Scan Working Group Minutes

Date – 04/05/2011

Attendees: CJ Clark, Bill Tuthill, Brian Turmelle, Carl Barnhart, Adam Cron, Roland Latvala, Mike Richetti, Carol Pyron, Wim Driessen, Ken Parker, Dave Dubberke, Craig Stephan, Ted Cleggett, Heiko Ehrenberg, Francisco Russi

Missing with pre-excuse Adam Ley,

Missing: Lee Whetsel, Neil Jacobson, John Braden, Bill Eklow, Ted Eaton,

Agenda:

1) Patent Slides and Rules of Etiquette
2) Clause 13, 14, 15 wrap-up
3) 16 & 17
   a. Reset-select issues
4) PDL Annex C   - Review Discussion

Meeting Called to order at 11:00am EST
Minutes:

Review Patent Slide – Reminder sent out over email during the last week.
Review of Working Group Meeting Guidelines

Carl gives an update on Clauses 13, 14, 15
        Incorporated feedback. Friday's discussion has not yet be incorporated into draft
        Changes in Clauses 8,9,11 were sent out in email

Carl Ask for groups permission to accept changes to date in 13, 14, 15. Changes from Friday's discussion will show up as track changes.

CJ and Ken want to see changes made to Clause 13, 14

Ken makes a Motion to accept the changes in Clause 13, 14, and 15 made to date without prejudice to changes made at a later date.
        Seconded by John
No discussion required.
Point of information from CJ – New chapters so these clauses will not have any problems diff-ing against 2001 version
Motion passes unanimously

Group will review tweaks made to these clauses next week and finalize sections

Carl – Clause 16 is reset select register

Reset Select register defined a lot of rules (functions) to it. Will need to go over carefully

Figure 16-2 updated

Got rid of capture capability which got rid of one layer of control and muxes.

Will need to redo figure to swap TDO and TDI in figure.

CJ wants to know if people will take this figure and hold the design as written in stone and can't be altered. Thinks the observe ability is worth the capture logic

Carol – suggestions adding text around the figure to describe options

Carl – add a recommendation so that final value of reset signal to logic should be captured to allow observation of reset.

CJ- should be very clear in figure

Carl – can add another picture of that one bit and add extra gates to show it.

Ken – likes the idea of a recommendation and is a useful thing to suggest.

Ken – why do we give permission to do this? It is just another wire and multiplexor. Should make them monitor the resulting state of the reset. Is this too much of a requirement?

CJ- agrees with the idea and doesn't think that it would be too burdensome

Carol – could add a top level wiring

Ken –will this result in a wiring objection?

Carol – yes

Adam C – easy to change "may" to "must".

Ken – not the word you should use but gets the idea.

Adam C – contingent to someone taking the permission

Ken – thinks k) should be a rule.

CJ – thing we are going after are optional reset. Pin level reset that is required we have observation through Boundary Register. What we are talking about here are the optional internal resets that occurring

Carl – if you look at the figure and the mux. If the mux is far away from the select register there are 2 wires. If it is close to the select register it are 2 wires. Doesn't see the difference

Carol – for internal resets Carol disagrees.

Internal resets will be scattered around. Will have master reset but will also have local reset. The local reset will need to be brought back across the chip.

Carl - simply capturing output of the mux.

Carol – only need that on the master and not internal

Carl – depends if there are another pair of reset and enable there is another mux controlling that.

Decided that Carol should go off and make a drawing to help understand where the problem is.

CJ – there is some objection to requiring the observe capability.

Carol – doesn't have an objection to observing the pins.

Adam C- do you object to observing the reset* signals
Carol – yes. Objects to the wire on the mux
Will take this offline with some drawings to get on the same page to understand Carol's
objections

Carol – do we need a rule saying if k) is implemented do we put it in the BSDL?
CJ – no construct to say where we are updating from
Carol – will need to develop a BSDL structure for that .

Clause 17
Conformance and documentation requirements
Small changes in this section

Clause 9
Updated section 9.2.3
Updated figure 9-4
Added coded snippets in VHDL and Verilog for capture-update TDR cell
Added figure 9-7
Updated figure after 9-7 about need to de-gate
Added table 9-1 Design Specific TDR interface

Clause 6
Updated figure 6-8 to de-gate clock. Gives ClockBSR and UpdateBSR (gated signals) to
boundary register
Updated clauses 8 and 11 to use the ClockBSR and UpdateBSR signals

Adam C: prefers the older method of gating clock. Might be a large deviation from what
is currently in spec and may need more explanation

Adam C – will look into the new text and see if it meets his expectations

Clause 11
Updated figures for BC Cells
Added "deprecated" to the BC 6 cell

Carl will post new draft with updates accepted from motion.
Carl posted draft for updates of 9,11,6 (04/04 draft)

Meeting adjourned: 12:00 EST.

Next Meeting: 4/12/2011 11:00 AM EST

1 Motions Made

Motion to accept the changes in Clause 13, 14, and 15 made to date without prejudice to changes made at a later date.
Seconded
Motion passed unanimously

NOTES:

New Teleconference information. Now using Live Meeting.

Join the meeting

Meeting time: Tuesdays 11:00 AM (EST)   (Recurring)

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Current Issues listed and who will champion that issue.
1   Observe only. –   Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko

3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:
*   CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
*   Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
*   Comment #8 CJ will make changes to draft for observe only
*   Comment #7 CJ will get in touch with Doug to get input regarding Comments
*   Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
*   Comment #4 Adam L to add comment about TRST. Update figure 6.8
*   Comment #3 Adam L will update language for any proposed change for this section.