Date – 08/23/2011

Attendees: CJ Clark, Bill Tuthill, Brian Turmelle, Ken Parker, Carol Pyron, Carl Barnhart, , Dharma Konda, Roger Sowada, Wim Driessen, Craig Stephan, Josh Ferry Francisco Russi,, John Braden,

Missing with pre-excuse Adam Cron, Adam Ley, Heiko Ehrenberg, Ted Eaton,

Missing: Lee Whetsel, Neil Jacobson, Mike Richetti, Ted Cleggett, Matthias Kamm , Peter Elias, John Seibold, Bill Eklow, Roland Latvala, Dave Dubberke,

Agenda:

1. ***11:00*** Patent Slides and Rules of Etiquette
2. B.8.14.3.8 <input spec>
    a. ***Motion Needed: Motion to accept B.8.14.3.8 in current draft subject to any wording improvements***
3. Further discussion on
    a. mixed R_F/R_A
    b. ***PPA and RPA***
4. Homework assignments

Meeting Called to order at 11:07 am EST
Minutes:

Review Patent Slide – Reminder sent out over email.
Review of Working Group Meeting Guidelines

Discussion on <Input Spec>
Question on if we had spent enough time on it.

Carl -did we end up with an Open X?
CJ – no
Carol – either open1 open0 pull1 pull0 . If the IO doesn't fit one of those descriptions than it is optional and leave it off?
CJ – yes that is fine but need to discuss with group about not having that ability.
CJ – no guarantee what the pin will do due such things as cross talk
CJ – is concerned about "optional". If you don't include the documentation for it that it is non compliant
Carl – BSDLs are created often before tap out
Francisco – has seen people planning BSDL at pre-silicon
CJ – has seen many revisions of BSDL after silicon as well
Carol – order of IO is dependent on floor plan placement around the die. Verify that the BSDL and RTL agree. Can have minor revisions after tape out. Doesn't have a verilog model for a Z. This Translates to a logic 1 so it can't be verified in simulation

Would be willing to do Open1 Open0 if spice designers could model the IO so that the Z could be modeled correctly

Ken – if the pad designer was to engineer the open behavior, no outside influences, seems like it would be reasonable to include in the BSDL. If it was an accident and not engineered than it would not be coded as an Open in BSDL. The IC designer is responsible for the Spec so if he has engineered the Open than put it in there and if it is not than it should not be in the BSDL
Carol – not so sure if it is a conscious decision, but feels that the IO needs to be simulated and then report on the IO. Functional behavior has priority over the open behavior.
Ken – describes consciously engineering- they can choose the feature and engineer it into their system.
Carol – agrees that there will be more attempts to build it that way, but will be lower priority in high speed IO
CJ – in LVDS we are required to drive a 1 when the inputs are open.
The BS cell can observe the 1 and coding would be Open1
CJ – open1 and open0 doesn't work will with Differentials and only 1 leg is open. This more for both pins shorted or open.
Carl – proposes keywords Weak1 and Weak0. ATPG can look at netlist and look for pull ups
Ken – what if it is 1meg pullup
Carl- have to assume designers have some competence.
Ken - concerned that the "pull-up" might actually be a logic 0 and will cause a problem.
CJ – a positive power supply will give it a pull up
Carl – need to not
Josh- as a user, you are just talking about how risky you want to be in your test generation. Doesn't mind the definition of weak, but as a user I would like to be given the choice to use it or not. For a standard weak is fine. And people can use it as they want.
Carol – feels this is a valid point
Carl – thinks it can be included and has value.
Carol – when BSDL does have weak0 weak1 do you do ATPG that does on that information or a switch to allow it to be ignored and treated as a Z or X
CJ – have always treated it as weak0/weak1, but do have switches.
Problem is that we are heading into an area that doesn't have test engineers that examine each pin. Would like the normal mode be aggressive. And then look at failures and mask out if necessary.
CJ – construct doesn't need to be used for ATPG if causing a flakey test.
Carol – willing to allow some companies to spec a weak0. Not sure she would. Sees that there is value to this, but wants to be realistic to what IOs can support and be spec.
Willing to add open0/open1/weak0/weak1/ and make it optional. Feels that it is realistic
CJ – optional if you don't have a description/description doesn't fit.
Carol- when it is optional than it means either I don't know what my IOs do or it doesn't fit one of the descriptions.

CJ – if you code weak1 in BSDL but internally you have Pull1. Is this an error or is this an optional.
Ken – if it is not labeled correctly than it is wrong.
CJ – so if the input has a pull 1 on the input and then they leave it out is that an error or optional.
Carl – would have to be a violation
Dharma – agrees it is a violation

Carl- needs more text and description in the section so he is reluctant to vote on the section. The concept is eligible for a vote.
Francisco – this may be minor for BSDL but major for library designers to add or change existing libraries.
CJ – how so.?
Francisco – open1/open0 is the concern not so much weak0/weak1
CJ – Agrees,
once we do specify these attributes than this information would fill into the libraries.
Some elements would be already categorized and just need to add the attribute.
CJ – what is Francisco's' position
Francisco – no problems with weak0/weak1. Open1/open0 will require changes in the libraries and wonder if having a weak1/weak0 or new idea (dc parameter attribute) would be good.

CJ – weak1 and weak0 might confuse people and might be difficult to generate
Carol – will have chips that want to support new standard and will be using old libraries. No one wants to go back and spice anything.

- **Meeting adjourned: 12:04** EST.

Next Meeting: 8/30/2011 11:00 AM EST

No motions made.
First order of business at next meeting is to settle the input spec

HomeWork Status
John has passed his examples in to the working group. CJ is running them through the parser.

Carol – is still working on examples
Heiko is still working on examples.
CJ is still working on port assignments

Homework assignments.

Heiko and Carol's assignments are outstanding and will be done for next week's meeting

CJ will have examples of port assignments

Bill E – work on more concrete example and definition of the ESSID register

NOTES:

1149.1 working group website - http://grouper.ieee.org/groups/1149/1/

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JOIN the meeting as GUEST – will have to ask to present

Meeting time: Tuesdays 11:00 AM (EST) (Recurring)

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