

Date – 10/18/2011

Attendees: CJ Clark, Bill Tuthill, Brian Turmelle, Craig Stephan, Adam Ley, Carl Barnhart, Jeff Halnon, Sankaran Menon, Josh Ferry, John Braden, Adam Cron, Ken Parker, Dave Dubberke, John Seibold, Dharma Konda, Carol Pyron, Roland Latvala, Bill Eklow, Heiko Ehrenberg, Roger Sowada, Francisco Russi, Brian Erickson*

*new member

Missing with pre-excuse

Missing: Lee Whetsel, Neil Jacobson, Mike Richetti, Ted Cleggett, Matthias Kamm , Ted Eaton, Peter Elias, Bill Bruce, Wim Driessen,

Agenda:

- 1) Patent Slides and Rules of Etiquette
- 2) *Review of Carl's draft changes*
- 3) Review of Mon and Pulse1/Pulse0 cells
 - a) Looking for BSDL token
 - b) <type assignment>::= **NOPI | NOPO | NOUPD | MON | PULSE1 | PULSE0** | <user type keyword>
 - i) Little change for the tool reader of BSDL. A method for IP providers, PDL writers to communicate the capability of the cell. Tools know how to handle in GUI and PDL (Cell resets automatically). Both cells add testability and PULSEMON reduces scans and enables an edge after UPDATEDR
- 4) *Switch Mux* & Boundary_Scan_Segment
 - a) Enables INIT_DATA to traverse multiple power domains
 - i) Controls and senses power before mux is on
 - ii) Mux enable allows scanning through power domain
 - iii) Use with Boundary Scan register
- 5) PDL Level 1
- 6) mixed R_F/R_A
- 7) Homework assignments

Meeting Called to order at 10:30am EST (new starting time)

Minutes:

- Carl reviewed additions to Clause 9 that he sent out earlier
- Documentation for self monitor and self reset cells
 - Allows the switching out of registers
 - Addition for the ECID
 - Design and Construction of test registers

- Rule C – now you can define fixed lengths segments or a fixed length register
- Note is modified to allow data registers may vary in length by switching fixed length segments into and out of the register

Ken – Does this imply that the ID code register can be made up of segments?

Carl – no it is still fixed length

Bypass register

Bypass escape

IDCODE

These 3 are all fixed lengths.

CJ – would prefer to see ECID as a single length register

Jeff – if you put in segments you need to do it the way we describe.

Carl – add to the note to add about switching

CJ – yes we want to be specific on this

Adam C- at power up do we know what the length is?

Carl/CJ – Yes.. That is a requirement

2 new types of cells

- a) Self monitoring TDR cell with update state and non gated clocks

Carol – asks about the construction of the diagram

Carl – this is made to be a clean diagram and can be made with different structures.

CJ – we would like to get the VHDL for these cells

Asks if we should show the VHDL for all the

Are people comfortable with what we have now?

We want consistently and people to use the illustrated cells in the standard. And should include the code.

Carl – can we put in the active code or do they have to be the full code.

Carol – just for illustration purposes. Since these are short snippets we should leave them in and be consistent and add for these 2 cells.

CJ – do we want to illustrate

Ken – do we understand the usage here of Self-monitoring?

Carl – how about Self-Capturing?

Ken – Self-monitor has meant something for 10-15 years and maybe changing the meaning would confuse those outside to the working group?

No output buffer on pin being monitored. No Line from the outside

CJ – if we go to Self-Capturing, we will need a new key word in place of MON

Ken – not the MON that is the problem it's the Self

CJ – this is capturing the PO

Ken – what is the difference between update and PO

Carl – there is a mux between update and PO

CJ – thinks this definition is sufficient enough

Ken – concerned someone will implement a boundary cell where the tap is outside the buffer and not inside the buffer

Adam L- agrees with Ken. Intent is to capture Update

CJ – Ken and Adam should come up with an alternative name.

Adam L – concern is that people are not reading every word and think it is a self monitoring cell and drop it in on a boundary and have less than desirable results.

CJ - Carl can make it clear that these cells are not for the boundary register cells.

Adam C- does this cell go into the boundary register

Carl – no

Adam C- can't be a register to control a switch mux.

CJ – no not with the changes Carl made.

Carl – might be used to turn power on or off in the boundary register. Would not be in a classical sense.

CJ – can we make it clear that it is not for use with pins?

Carl – yes.. Will fit that in

Dharma – if there is no reset will this be tied

Carl – would be tied to a 1 - the dash line is optional reset.

b) Self Resetting and self-monitoring TDR cell with non-gated clock

A timing diagram was also added.

Ken – so it is monitoring the fact that the PO was high?

Carl – it is monitoring if the PO was high or low during the update sequence

Ken – would be helpful if there was a state in the diagram for the tap

Carl – reset is not option in the cell

Carl – monitoring is to show if a defect in Cell keeps you from writing out what you wanted to write out. Doesn't have to be done every time. Once you prove the cell working correctly

CJ – another place it is used is to give you a sense you are scanning in the place you except to.

Ken – would request that the tap state be added to the Figure 9-12

CJ – how does the group feel about the rules stating this is what we expect for behavior

Carl- the monitor behaves the way a traditional update cell behaves.

CJ – would also like to show the inverted PO.. to get back to the negative going edge

Carl- can put an inverter and PO* on it.

Ken – should be 5 or so rules that express the behavior of the cell

Carl – there are rules that define basic behavior but no additional rules about capturing the update or doing the pulse business. Any Suggestions?

CJ – offline will take a stab at some of the rules about how/when the pulse occurs.

CJ – a complete consistent approach will bring value to the industry.

Carol – BC cell types have benefited industry with their consistency.

Are there going to be legality tables setup for this.

CJ- if you can get your PO to pulse with a rising edge on the falling of TCK and UPDATE than you are in good shape.

Carol – this is an internal TDR do you actually care that it happened on that edge or had an impact the next time you come around.

Should be rules defined that you care about.

CJ – The PO would have to change on the Edge of TCK

Carol – what if you had to double clock the signal to cross clock domains.

CJ – that would be bad.

Carol – why is that bad?

CJ – you can make your own cells, but this cell has its own special behavior.

CJ – we are not preventing you from having the flexibility that you like. What we are saying here is that we want one cell type that does one function.

CJ – will put the rules together and will gather feedback.

New section 9.4

Test data register segment controls

Carl reviewed the new rules that were added

Adam C- does this architecture demand longer wires ?

Carl – possibly.

CJ – you can have the mux close to the cell but the output of the excluded segment would be longer. Where would you

Adam C- mux stays where it is but the cell goes close to the control cell

Carl – if control cell is downstream of the break you can't load it to correct the situation, if it is up stream you can scan in a 0 and cause the bypass to exclude it and restore the scan chain.

Adam C – is this a suggestion or a need?

CJ - creating rules for that.

Dharma – shouldn't be a problem if you can take care of timing. Or move layout to help. In the real world this may not be linear like in the diagram.

Sankaran – why would you say the length isn't too long

Dharama- many things you can do inside the chip. Move clocks around. Or added flops.

CJ – are we ok with this section?

Ken – in the case of the boundary register, the only reason we exclude segment is because of power

Carl – yes as far as what we talk about in the standard, but there is no intention to having a rule to that

Adam C- power turning on and off and segments added are orthogonal.

Ken – reason for segmenting was justified with power domains.

Carol – also for useful for multichip packages. Even in the same package there are reasons to do it.

CJ – primary reason is Power. But there are probably some other things that are there.

Carol – no reason to exclude other reasons for it.

Ken – what happens to data if the segment was included and the excluded?

Carl – it is held. It is a recommendation to hold data when not selected on scanning.

Ken – because of the recommendation I can't couldn't on that so when I include it I must assume that it is full of garbage. I can't predict what is on the chain. So for a boundary register I don't know what it could be doing to the IOs when you add the chain.

CJ – going to have to do preload with power on

Ken – so there is a period of time between power and scan of new section where the new section is doing random stuff?

Carl – you will not be in EXTEST or clamp when you are doing that. You would be in your normal non-invasive mode.

CJ – no plan on turning segments on or off while you are in EXTEST.

Ken – some segments might be included/excluded per board setup.

Carl – you can power up the segment

Adam L – basically the bit that is controlling power doesn't have a mux in front of it for normal mode or not.. Once you scan that bit that you are driving.

CJ – if you are turning the power on for an IO segment, you won't typically fry a board. In most cases you can't turn the power on.. Power controlled at the board level.

Figure 9-15 Scan Switch Cell with ungated clocks reviewed

CJ – doesn't have any benefit in the boundary register

Carl – doesn't hurt and makes it one way of doing things.

CJ – adds extra delay but it is fine

Carol – likes the design

Carol – once you are in TLR you are back in mission mode.

Carl – with persistence on we are still in test mode controlling the IP

Carl – TRST will always collapse them

Carl – makes a suggestion to take a quick poll to move on with the changes

Wants an informal poll

CJ – anybody opposed with moving forward with the changes Carl has made?

No one objected

No abstentions

Ken – the question isn't are we approving or is it ok for Carl to proceed.

Noted and is cleared.

Ken – Does the definition of the segment mean that it is indivisible. Can't have nesting

CJ – correct.

Carl – thinks there is a rule.

Ken – segments are basic atoms and we can only build a linear chain.

Carl – yes

CJ – coordinating with 1801. We will get a copy of the draft. Also tried to contact Ron Aiken to get feedback

Introduction new member

Brian Erickson - Apps Eng with JTAG technology has joined the group.

Next week we will make an attempt to vote on this section.

• **Meeting adjourned: 12:00EST.**

Next Meeting: 10/25/2011 11:00 AM EST

0 Motions Made

HomeWork Status

IEEE 1149.1- 2011 Boundary Scan Working Group Minutes

John has passed his examples in to the working group. CJ is running them through the parser.

Carol – is still working on examples
Heiko is still working on examples.
CJ is still working on port assignments

Homework assignments.

Heiko and Carol's assignments are outstanding and will be done for next week's meeting

CJ will have examples of port assignments
Bill E – work on more concrete example and definition of the ESSID register

NOTES:

1149.1 working group website - <http://grouper.ieee.org/groups/1149/1/>

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JOIN the meeting as GUEST – will have to ask to present

Meeting time: Tuesdays 11:00 AM (EST) (Recurring)

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