

Date – 10/25/2011

Attendees: CJ Clark, Bill Tuthill, Brian Turmelle, Adam Ley, Carl Barnhart, Craig Stephan, Dave Dubberke, John Seibold, Sankaran Menon, Wim Driessen, Josh Ferry, John Braden, Bill Eklow, Adam Cron, Francisco Russi, Heiko Ehrenberg, Carol Pyron, Jeff Halnon,

Missing with pre-excuse Roland Latvala,

Missing: Lee Whetsel, Neil Jacobson, Mike Richetti, Ted Cleggett, Matthias Kamm , Ted Eaton, Peter Elias, Ken Parker, Dharma Konda, Roger Sowada, Brian Erickson, Bill Bruce,

Agenda:

1. Patent Slides and Rules of Etiquette
2. *Review of Carl's draft changes Clause 9 and Clause 11*
 - a. Motion to accept changes in Clause 9 and Clause 11
 - i. Subject to further refinement of cell names
 - ii. Subject to new discovery of any 1801 conflicts/problems
 - iii. Subject to working out b-s register segments which are off
3. Boundary_Scan_Segment
 - a. Is the b-s segment in test mode or mission mode when it is not included?
 - i. In test mode – allows for short b-s register and non-active segments to 'clamp'
 1. Why not make a private instruction for a short b-s register?
 2. Requires preload of all segments even if you're not using them
 3. If EXTEST allows off segment to be in mission mode and CHMODE (TMP controller)
 - a. Forces it to test mode, then two signals routed for each segment and not one.
 - ii. In mission mode -
 1. No need to preload segments which are not going to be used or are unknown to user
 2. Single CHMODE/MODE signal routing
 3. Behaves like IC b-s registers on board that are not in EXTEST
 4. SERDES and other factors limit use/effectiveness of 'holding pins' going forward
 5. PCB can be designed to manage I/O of non-1149.1 devices
 6. User defined IP blocks are the way to communicate to non-1149.1 devices while entire b-s segment is in clamp_hold (enables at-speed testing) so b-s register is not in path at all.
4. Review of Mon and Pulse1/Pulse0 cells

- a. Looking for BSDL token
 - b. <type assignment> ::= **NOPI | NOPO | NOUPD | MON | PULSE1 | PULSE0** | <user type keyword>
 - i. Little change for the tool reader of BSDL. A method for IP providers, PDL writers to communicate the capability of the cell. Tools know how to handle in GUI and PDL (Cell resets automatically). Both cells add testability and PULSEMON reduces scans and enables an edge after UPDATEDR
5. PDL Level 1
 6. mixed R_F/R_A
 7. Homework assignments

Meeting Called to order at 10:30am EST (new starting time)

Minutes:

Review Patent Slide – Reminder sent out over email.

Solicited input from anybody who is aware of patents that might read on our standard.

No responses.

Review of Working Group Meeting Guidelines

Review of Test Data Register segments

Discussion of added rules

When excluded , test data register segments shall not respond to the

Update_DR Tap state

When segment is returned the value of register is assumed to be unknown

Updated figure 9-14

CJ: segment enable cell is really a power enable cell??

Carl: wasn't sure if this was the case or not. Will update the figure

CJ: Craig will simulate figure 9-15 to make sure it works the way it

should.

Clause 11

Power up cell now requires a PO only cell (control-only cell)

CJ: feels someone might object to the word “control”

Control cells are special cells. But if it is clear for everyone than no problem

Modified length verbiage to include segments.

Can not vary the length of a register or a segment itself.

Can have either a descript of full boundary scan register using attributes or you can have 1 or more boundary scan register segment descriptions but can't have both.

Rule h) says that it is fixed while running.

permissions

CJ: control-only cell should be called power-enable.

CJ: likes power-enable and segment-enable for names of new cells.

CJ looks for a motion to be made on clause 9 and 11 being accepted with subject to refine cell names, subject to 1801 conflicts, and subject to working out b-s register segments which are off

Motion made by Carl to accept changes for clause 9 (only) subject to further refinement.
Seconded by John Braden

No further discussion

1 no Adam Ley

2 abs Wim Driessen, Heiko Ehrenberg

14 yes

Adam Cron, Bill Tuthill, Brian Turmelle, Bill Eklow, Carl Barnhart, Craig Stephan,
Dave Dubberke, Francisco Russi, Jeff Halnon, John Braden, Jhn Seibold, Josh Ferry,
Sankaran Menon,

Motion passes

Boundary Scan Segments.

In test mode allow for short boundary scan register and non active segments to
“clamp”

Why not make private instruction for short b-s register?

Requires preload of all segments even if you're not using them

If Extest allows excluded segment to be in mission mode and CHMODE (TMP controller) forces it to test mode, then you will need two signals routed for each segment and not one.

In Mission mode

No need to preload segments which are not going to be used or are
unknown to user

Single CHMODE/Mode signal routing

Behaves like IC b-s registers on board that are not in EXTEST

SERDES and other factors limit use/effectiveness of holding pins going
forward

PCB can be designed to manage IO of non-1149.1 devices

User define IP blocks are the way to communicate to non-1149.1 devices

while entire

b-s segments is in CLAMP_HOLD

Adam C: seems inconsistent in test mode

CJ: need to refine what TMP means. Only useful for boundary register.

Carol: don't require preload if you have control-r

Adam C: TMP bit would be kind of a way to guard from letting the boundary go wild.

CJ: need to preload every segment even if you are going to turn them off. Otherwise
more danger where people will go into clamp or EXTEST and not preloading all
segments.

Carl: in test mode. You can do most with private instructions. Shorting the b-s register
doesn't have much value.

TMP controller if off you don't need to do the preload.

In mission mode.

Carl: in test mode controller we have a rule d now 6.2.??d

Change rule says that when a segment is excluded the TMP controller doesn't control it. Already have a mechanism to place pins in mission mode..

Either allow this mechanism to stand so when a segment is not selected it is the same as when a TDR is not selected and between TDI and TDO. Which means that it would obey clamp and the TMP controller.

This is a rule how to exempt pins from the TMP control.er

Can adopt CJ's position by altering the rule in the TMP controller.

Not ideal but would be consistent

CJ:

Jeff Halnon: deals with many "non-compliant" chips

Most of the SOC and IP that deals with are "odd".

CJ: that is why we are trying to define more in the standard to reduce the odd

CJ: can enable the segment and give it static values easily. The question is how it works when it is excluded.

Dave: any testing on a board looking as a flat. Where everything is on. If I excluded it, I wouldn't care what was the contents of the cell. So if it wasn't included it wouldn't have control.

Carl: if I issued a clamp instruction what would it do

Dave: would not care. Wouldn't want clamp to have any effect on it.

Sankaran: can we make it sticky?

CJ: Clamp_Hold has that capability.. Says will hold the pins in the boundary register after changing the instruction.

Carol: agrees with what we are saying for the Boundary Register.

For other TDR's it is up to the designer to define what it is doing.

CJ: No TMP on user defined registers.

Jeff H: are we talking about having the cells in a segment inherit the test mode persistent

CJ: in the boundary register and gets a mode that controls the mux (test mode or mission mode) The cell that switches would be gated with the mode (CHMOD) clamp hold)

Jeff: there is only one?

Carl: Mode signals all take the same value as the clamp instruction

CJ: b-s cells would have pins in mission mode when the segment is in mission mode.

That is the question.

In test mode that would require preloading segments that are you are not interested in using.

Carl:

Jeff H: what if we had another flip-flop that latched the status of the mode and latched at the time the segment was bypassed. And that mode would be latched. To unstuck it you have to put it back in the chain and let it reacquire the TMP bit again.

Carl: maybe missing is when you power up all segments are excluded.

Jeff H: if it is excluded it stays that way. On power up the flip-flop is set for mission mode.

CJ: what capability are you not getting? If you don't care about segment you turn it off. If you want to put it in EXTEST you turn it on.

CJ: what we have will do what you need.

CJ: so far we haven't seen a way to turn all the segments on before preloading it. Now you need to sense power before you turn the segments on.

CJ: Heard more today than Friday that the mode should be Mission Mode.

Carl: have scenarios where you have pins in test mode and you want to take those pins out of test mode. Sometimes the test engineer wants to hold the entire chip quiesce other than what he is working on.

CJ: what to make sure we are getting behavior for the board test engineer.

Should consider the routing of CHMOD /Mode not to make 2 signals to route.

Wim: One problem. Doesn't want bits in the scan path to be both control and data.

CJ: focused on mission mode or test mode for the segment when it is off. Look at control off line

CJ looks to take a Straw Poll .

When the segment is not included in the scan chain are the boundary registers are in test mode?

Heiko (depends)

Carl

Francisco

Wim

2 others

Adam Ley: Yes (would like to add more info to his yes vote - 2 bits of information for control. Why can't we have both modes. Bit that selects if the chain is included and another bit saying it is active (powered on) if it is not active and powered it would be mission mode.

Jeff Hanlan: likes the 2 bits. Would be more like adding a 3rd bit)

CJ: can always have a third bit to set as control. Would prefer that instead of a monitor bit that latches the state as was suggested earlier in the meeting

CJ: do we want to add another bit? How much of a burden would that be ?

Adam does That bit is the override even with TMP controller is present?

Adam L: TMP should be the superior function

CJ: than we are stuck, and still need to have everything preload

Adam L: Yes additional bit segment active bit would be the one that says do we expect the segment to participate in the test. Would be like the override already described for the TMP controller.

Mode cell would have to be overriding factor. Would have to override CHMODE or mode. Would have complete flexibility at the cost of the bit. If that bit isn't too much it would be a good compromise.

• **Meeting adjourned: 12:05 EST.**

Next Meeting: 11/1/2011 11:00 AM EST

1 Motions Made

Motion made by Carl to accept changes for clause 9 subject to further refinement.

Motion passed

HomeWork Status

John has passed his examples in to the working group. CJ is running them through the parser.

Carol – is still working on examples
Heiko is still working on examples.
CJ is still working on port assignments

Homework assignments.

Heiko and Carol's assignments are outstanding and will be done for next week's meeting

CJ will have examples of port assignments
Bill E – work on more concrete example and definition of the ESSID register

NOTES:

1149.1 working group website - <http://grouper.ieee.org/groups/1149/1/>

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[ppppp11491p*pp03820#](tel:ppppp11491p*pp03820#)

JOIN the meeting as GUEST – will have to ask to present

Meeting time: Tuesdays 11:00 AM (EST) (Recurring)

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