

Date – 1/3/2012

Attendees: CJ Clark, Bill Tuthill, Brian Turmelle, Peter Elias, Ted Eaton, Wim Driessen, Carol Pyron, Adam Cron, Ken Parker, Craig Stephan, Dharma Konda, Adam Ley, Josh Ferry, Dave Dubberke, Jeff Halnon, Roland Latvala, Carl Barnhart, Francisco Russi, Kent NG, Heiko Ehrenberg

Missing with pre-excuse:

Missing: Neil Jacobson, Mike Richetti, Ted Cleggett, Matthias Kamm , Roger Sowada, Sankaran Menon, Bill Bruce, Brian Erickson, Kent NG, John Braden, Bill Eklow, , John Seibold, Lee Whetsel,

Agenda:

- 1) Welcome Back
- 2) Patent Slides and Rules of Etiquette
- 3) Annex C Discussion.
 1. Annex C PDF of clean and diff to be on website private area.
 2. passing originals to Carl.

Meeting Called to order at 10:30am EST (new starting time)

Minutes:

Review Patent Slide – Slide Presented to the Group.

Solicited input from anybody who is aware of patents that might read on our standard.

Wim: There is a patent pending on pulsing from Cell dated back from 1996. Will Send CJ the details

CJ will work with Wim offline to make sure there are no issues.

Ken asks for a definition of “Essential”

Adam: it is defined in IEEE patent Policy. Will find the specific reference and forward it to the group.

Review of Working Group Meeting Guidelines

No Objections

Discussion on Annex C

Changes have been posted to the website.

Changes are not complete and more work needs to be done but wants to get information up to start discussion.

This is not a tutorial so it might make it a little difficult to understand the big picture of PDL

CJ notes that nothing has been voted on so these keywords and descriptions haven't been set in concrete.

CJ: Proc for ECID has been added

Level 0 PDL commands.

Fix ups

Changes from 1687

iTarget – separated to have 2 commands

For targeting

For specifying the proc

Adam C: changes from 1687 or changes due to 1687

CJ: Changes due to.

iProcTarget

To avoid collisions of PROC names. Creates instance or type based PROCS. Tools will use to create unique instances.

Ted: you can do the hieratical calls in 1687

If you have a reusable set of PDL you don't want to have to change every iProc call to retarget to a different reference designator. Simplifies retargeting.

IProcTarget - turns targeting for iProc off. Tools don't know when to turn off targeting and this is a way to avoid having to keep changing target

CJ points out that 1687 has not solidified all the PDL details and had gone ahead and deviated from 1687 in the interests of cleaning up the Loose ends that CJ sees with 1687's PDL

Ted would like to see differences highlighted between 1687 and what CJ has added.

CJ points out that there is not a finalized document to show 1687 PDL

Carl: why isn't the iProcTarget before the source.

CJ: need to source all the objects you might have .

CJ: to target something at the board level. You use iTarget

iTarget was broken out to iTarget and iProcTarget

What is the proper way to get the full hieratical register name available.

Adam C: at the board level how do you target the board? To get to the very top.

CJ: You can target the different chips with a iTarget command to have chips talk to each other at the board level.

Adam: how to call the top level.

CJ: a blank iTarget will assume top level

Ted: find that outside the scope of a chip standard.

Ted: type association is supported in 1687. You have always been able to assign a procedure to a type.

CJ: rules haven't been defined. So how the full register path is created is not defined well in 1687. 1687 seems to be more instance based and not type based.

Ted: would disagree with that.

Ken: how does this work in a serial environment if the parts are on the same chain

CJ: in a PRBS example, you would setup the receiver first than transmitter and then read the receiver. That is how you would do it sequentially

Ken: if you U3 and U2 in the same chain, what do you do on U2 while focused on U3

CJ: you scan in the test data registers

Carl: you could put the other chip in Bypass

Ken: so you aren't parallelizing the sequences? The chip out of focus is doing the last instruction?

CJ: if it was written that way. You can write it to not work that way.

CJ: showing a scan frame for 2 devices would help clear it up

CJ: iMerge will tell the tool to line up the iApplies and call both routines at the same time so that the scan is optimized.

Just a method to optimize so it doesn't need to be done but needs to parse it.

Ken: concerned about how the tool would know what should and shouldn't be done concurrently. Not seeing the hints to the tool to know how to do it.

CJ: without the iMerge command it will be done sequential. With the iMerge command the tool will have to know. There are some other keywords that help.

iTake, iRelease

Wim: each function should tell the tool if it can be merged or not, with a keyword perhaps.

CJ: is open to suggestions to help solve the problem.

CJ will work on more material for Friday's meeting to help clear up some of the merging issues.

CJ goes through example of how Hierarchical code is converted to a Flat interpretation.

Ken is concerned of where files come from and how many files that will be needed to be called in.

These are Short examples. But would have all procedures in one file.

Could put all code in one file if wanted .

Wim: how does INIT be done using PDL. Example like this is outside scope of 1149.1

Carol: Agrees. PDL was started for INIT and should have some examples to show it.

Wim: Thinks that the PDL should be a separate standard

CJ: would do the industry a disservice if 1149.1 couldn't run chip tests.

Ken: would like to see examples for PDL

Carl: thinks it is necessary that the Procedural language so that people can use it for things that are not in the standard. We should try and make our examples in the Standard to be dealing with explicit instructions that require PDL.

Carol: last set of examples should be illustrating advanced constructions

CJ: there is a community out there already that have done things with 1149.1 in an ad hoc way, and we should provide a mechanism to ease the work load in the industry. Have an opportunity to provide an ability. EXTEST is limited.

Carol: Agrees. As a chip vendor, we use JTAG extensively to access BIST engines and write to registers at will.

Carl: there is a value in having a standard way. But we shouldn't have to add an extensive tutorial to the Standard. Should be able to show everything with the standard instructions.

Meeting adjourned: 12:06 EST.

Motion Summary

0 Motion Made

Next Meeting: 1/10/2011 11:00 AM EST

HomeWork Status

John has passed his examples in to the working group. CJ is running them through the parser.

Carol – is still working on examples
Heiko is still working on examples.
CJ is still working on port assignments

Homework assignments.

Heiko and Carol's assignments are outstanding and will be done for next week's meeting

CJ will have examples of port assignments
Bill E – work on more concrete example and definition of the ESSID register

NOTES:

1149.1 working group website - <http://grouper.ieee.org/groups/1149/1/>

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JOIN the meeting as GUEST – will have to ask to present

Meeting time: Tuesdays 11:00 AM (EST) (Recurring)

AUDIO INFORMATION

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