

Date – 04/10/2012

Attendees: CJ Clark, Adam Ley, Bill Bruce, Bill Eklow, Bill Tuthill, Brian Turmelle, Carl Barnhart, Carol Pyron, Craig Stephan, Dave Dubberke, Francisco Russi, Hugh Wallace , Jeff Halnon, John Braden, John Seibold, Ken Parker, Kent NG , Peter Elias, Rich Cornejo, Roland Latvala, Wim Driessen, Dharma Konda,

Missing with pre-excuse: Roger Sowada,

Missing: Lee Whetsel, Matthias Kamm , Mike Richetti, Neil Jacobson, Ted Cleggett, Sankaran Menon, Brian Erickson, Heiko Ehrenberg, Adam Cron , Ted Eaton, Josh Ferry,

Meeting on 4/3/2012 was canceled

Id you Agenda:

- 1) Patent Slides and Rules of Etiquette
- 2) Use LiveMeeting “Raised Hand” to be recognized and take the floor
- 3) Editor’s comments on draft
- 4) IC_RESET homework wrap-up
- 5) INIT_SETUP/INIT_RUN homework wrap-up
- 6) Finalizing for Ballot

Meeting Called to order at 10:40am EST

Minutes:

Review Patent Slide – Slide Presented to the Group.

Solicited input from anybody who is aware of patents that might read on our standard.

No responses

Review of Working Group Meeting Guidelines

No Objections

Carl to get new draft out later this week for review.

Homework assignment from last week was to review init_setup and init_run

Carl has some questions that need to be resolved.

Carl – what is the polarity of the reset inactive value of bits in the reset select register?

Hugh – Abstract language. At least provide them with the ability if it is inversed or not

Carl – need to define what happens then you hit TRST.

PDL assumption is if you have not applied a field it will be set to 0’s

This could be dangerous

Ken – agrees

Dharma -

Carl – rules are that TRST will set the register to all 1's . PDL will assume it is all zeros

CJ – PDL doesn't have an assumption. We can define when a register is not defined we can define all 0's go into a register. In this case we have defined a register. We are defining the default values of the register in the standard. We can have the control value change but the actual reset would be preferred bring the bit low.

Carl – Async resets tend to be low. Sync resets tend to be high active. Not always reset = low. Asking for trouble to create this one register where things are negative active.

Jeff H – if there is a way we can get it changed so it is consistent by changing the name of the function so the active high vs. low would be consistent we should investigate that option before we give up on it.

CJ – pin based reset (which is what this register is describing) have been active low.

Granted there are exceptions. But commonly there are more active low resets.

Jeff – old school resets. New school resets are not a single even. Reset is a process that requires a clock and multiple states. It's not just a pin anymore.

CJ – this reset is only it mimic the pin being toggled through a bit in the TDR.

We are not trying to design a POR.

Roland – new libraries are active high async reset. What is traditionally low may not be the case in the future.

Carol – chip pin is active low

CJ – just trying to mimic the function of the pin. There is some value in having the PDL written so that when you are talking to the reset control bit having it similar to the reset pin. If the pin needs to go from low to high. The test engineer would be more comfortable in setting the bit in the reset control register the same way that the pin is being set. Just trying to map the pin functionality to that one bit functionality.

CJ – do we allow the flexibility to have these registers come up in any state. Or do we nail down the polarity of the register.

Carl – suggestion is to change the default polarity from negative active to positive active.

Carl – not hearing a consensus. And leaving it the way it is.

CJ – continue discussion over the reflector.

CJ – Reset Control is the bit that follows the bit.

Ken – name it Reset Function?

CJ – reset hold and reset enable are also functions.

CJ- Reset Control bit is the one that needs to be defined. So if you want the flexibility than the standard should say that the reset value should match what the active state is for the pin

Ken – struggling for a better phrase for reset control bit. Should it be reset assert bit.

That is he bit that you play with.

Carl – reset enable selects ether the control bits

CJ – not seeing a problem reset_hold and reset_enable with their default state.

CJ – we will move this to reflector and continue

INIT RUN and INIT SETUP

Rule C –

Init_Run

Rule e- INIT_RUN and ESSID only absolute time was allowed. PDL supports absolute time, tck, sysclock . We need to decide if INIT_RUN and ESSID code should support system clock.

Carol – half and half. INIT RUN should not allow system clocks but ESSID should .

INIT RUN is using its own TDR to program what is going to happen to the analog controls. All in the TCK domain. For ESSID you are actually having to do a partial POR to read non volatile memories.

ESSID will get greater acceptance and more usage if you allow system clocks.

CJ – like BIST. Need the system clock to run the process.

Jeff H – init should be left for more primitive things. ESSID is more advanced.

No system clock for INIT. ESSID can have system clock .

Init needs to be reserved for fundamental functions.

Dave D – in favor in having system clocks for INIT and INIT RUN. There is a complication in the crossing of test and system clock domains. Typically the IO functions are configured using system clocks.

Francisco – preamble for ESSID? Do we need to specify how to get the ESSID

CJ – we won't specify how we will get ESSID.

Ken – 2 domains. Gross manufacturing errors. Analog and digital testing. And get the board as quiet as possible. Turn clocks off. So if I need the clocks on to make init setup and init run work. Can I turn the clocks off after they are setup? How hard is that to do? Would be good if INIT_SETUP and INIT_RUN are clock free (only TCK)

ESSID is advanced and part of the testing that you would want to do with the clocks on . This is a whole different kind of test.

No system clock for Init Setup and Init Run

Bill E – a lot of the stuff that relies on the System Clock for ESSID is transparent. Data Loaded when you do a POR. Before you would get a chance to turn the clocks off.

Thinks it is more to describe if we need to do any waiting for this stuff to happen.

CJ – the question is do we allow for system clocks.

Bill E – Take the not having the system clock out of the clause. Don't say you can't use the system clocks. Just take that part out and it works.

CJ – for both INIT_RUN and INIT_SETUP and ESSID?

Bill E – for ESSID.

CJ – do we allow system clocks for init run and init setup and ESSID?

Carl – only limiting for Init run. Not rule for init setup. Not time dependant

Carol – should be able to do init run without system clocks.

Bill E – either allow a system clock or don't do ESSID. Don't see how to do this with just TCK. Remove part about external clocks

Ken – Init Run should not be using system clocks. The other scenario you get into when doing extest testing you might not even have a system clock available. If you get into a situation where you can't do INIT_RUN and put into EXTEST we are pretty much hosed.

Ken – ESSID code has legitimate reasons to have system clocks.

John S – a vendor that does it the way Bill described. The ESSID is loaded behind the scene with system clock. Does provide a way to do with TCK though. Prefers the system clock allowed for ESSID.

Carol – when you say behind the scene you mean that you are doing a POR too.

John S – yes.

Carl – consensus that INIT Run should exclude system clocks and ESSID should allow system clocks.

CJ – did hear 2 people not in favor for TCK only for INIT Run.

Carl – heard consensus for changing the rule in ESSID code. But no consensus for changing the rule in INIT_RUN.

CJ – majority now is for INIT RUN to be used with TCK only.

John B – agrees with Carol on the EXTEST. Flexibility allowing other clocks, not just TCK, would make it easier for people to implement the standard.

Carl – init setup and init run was written as the initialization of EXTEST. Init Setup and Init Run may be rerun later to set up the chip for a different test. May want to restrict that during interconnect test you do not allow system clocks.

Ken – I see that as a permission.

CJ – can't use INIT Run for any functional mission mode. Because it puts it in a non mission mode.

Wim – Agrees with Ken.

CJ – from a test perspective would like to see it only with TCK. But from a design perspective it may be restrictive .

Meeting adjourned: 12:00pm EST.

Summary of Motions Voted on
0 Motions voted on

Next Meeting: 4/17/2012 11:00 AM EST

NOTES:

1149.1 working group website - <http://grouper.ieee.org/groups/1149/1/>

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Meeting time: Tuesdays 10:30 AM (EST) (Recurring)

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