Date – 05/15/2012

Attendees: CJ Clark, Adam Ley, Bill Eklow,Bill Tuthill, Brian Turmelle, Carl Barnhart, Carol Pyron, Craig Stephan, Dave Dubberke, Dharma Konda, Francisco Russi, Heiko Ehrenberg, Hugh Wallace, Jeff Halnon, John Braden, John Seibold, Josh Ferry, Ken Parker, Kent NG , Peter Elias, Rich Cornejo, Roland Latvala, Sankaran Menon, Wim Driessen,

Missing with pre-excuse:

Missing: Lee Whetsel, Matthias Kamm , Mike Richetti, Neil Jacobson, Ted Cleggett, Brian Erickson,
Adam Cron , Bill Bruce, Ted Eaton, Roger Sowada,

Agenda:

1) Patent Slides and Rules of Etiquette
2) Use LiveMeeting "Raised Hand" to be recognized and take the floor
3) Brief update on draft
    a. INIT_SETUP with mandatory test/mission mode bit
4) Motion to specify a system clock attribute needed for INIT_SETUP/INIT_RUN. (This motion says two things, 1) system clocks are allowed for INIT_SETUP/INIT_RUN state machines 2) an attribute will specify the names of the ports required
    a. Details to be specified later. Based on John Seibold's example

```
attribute SYSCLK_COMPLIANCE of xyz : entity is
"("&
"(XUAI_REFCLK, 156.0e+6, OFF),"&
"(PCIX_REFCLK,100.0e+6, ON)"&
")";
```

    However, don't want dataclocks as shown. (FPGA one data clock per pair). Don't need additional pinmap.

5) REGISTER_CONSTRAINTS

```
Mnemonic_Identifier [A-Za-z0-9\@\&\*\_\-\+\|\:\'\.]*
```

    - No unary operators allowed in an M_I

<binary expr> ::= <check expression> <white space> <binary operator><white space> <check expression>

    a. CJ to get with Carl, Bill, Hugh and anyone else for wrap-up

6) Finalizing for Ballot - Go to ballot before end of month

Meeting Called to order at 10:35 am EST

Minutes:

Review Patent Slide – Slide Presented to the Group.

Solicited input from anybody who is aware of patents that might read on our standard.

No responses

Review of Working Group Meeting Guidelines

No Objections

Ken – sees a problem with test/mission mode bit
Carl – including it as a safety bit for the test engineer. Engineer would have to decide what to bring in test mode.
Ken – trying to mask init-setup invasiveness
Carl – believe that the vast majority of cases invasiveness would be benign. Only turn bit on if it caused a problem if a chip was mushy before going into test mode.
Ken – have 2 init-setup instructions. Can coordinate behaviors better
CJ – expected behavior from Test Engineer side 2 instructions might be more palatable than the bit.
Ken – bit being set in a long string could take 1k's of bits before it is set
CJ – dealing with these problems today. Don't see how we can get around it. Not sure we need to be super concerned.
Carol – 2 different init-setups ? same TDR or different TDRs?
CJ – same TDRs. Decode of instruction would set test or mission
Carol – if you do one do you need to do both?
Carl – yes. If you have init-setup you have both.
Carol – agree it's low cost. If they use the non test mode version they could be intrusive.
Ken – can do the wrong thing but this gives a way out.
CJ – adds more to standard since we can't determine if init-setup should be test mode or mission mode.
CJ – need more time to develop this if we prefer 2 instructions over the bit.
Carl – agrees a little more discussion before we vote on it.
Adam L-
Carol – views it as tools in a tool kit
Hugh - any possibility we give a default state and use PDL to turn the other mode on
Jeff H – why are spending a lot of time to do what looks like test mode functions before we go into test mode.
Carl – test mode is defined in a particular way. Taking control of the IO with boundary register. We are not doing that. We are doing things that people label "invasive". So getting from mission mode to test mode was simple in 2001. Now there are many things to get the internals of the chip to a safe and cool state that is no longer simple process. It is now more involved to get board ready for test. Not clear that we can just "drop the hammer" anymore.
Jeff h- if you have the power turned off, how can you do anything. You would have to turn on a part of the chip that isn't under mission mode control. Is it really being

controlled? No it is artificially forced to go on. We are making a lot of Mush. Is it feasible to manage the mush completely in test mode? Instead of out of test mode?
CJ – the mush includes setting analog parameters and modified in mission mode.
WE do have segments that are powered off. The reasons they are powered off is not as safety critical measure but as power saving measure. We need some how to turn those segments on for full test. Could leave them off with less test coverage.
Jeff H – if you have an excludable segment, before you preload it, in mission mode you have to turn it on. So you have a segment that is turned on, and those pins on that boundary register are not under control yet.
CJ – will always be the case. Pins that aren't controlled after they are powered on, they are in mission mode. Then we go into test mode with the pins.
CJ – not much way around it. Don't have a way of scanning a register with power off. Power needs to come on, artificially before we can scan it.
Jeff H – we would be better off if the test engineers were in total control or not. This half way state is troublesome.
CJ – no half way state. Not injecting a halfway state into the standard. Trying to make tools that have a testmode, mission mode and something in between
Jeff h- as soon as we start turning things on and off, the 2 modes need to coexist. Concerned about what the test engineer process is trying to do and the mission mode process is trying to do and they step on each other.
Carl – I think we have the same problem in the industry today and the test engineer is on his own. Trying to give the test engineer some better handles. Worried about what glitches are created during setup. Just trying to give the test engineers the tools to provide themselves with ability to look at problems when they see them.
CJ – catch 22. Need to turn on the segment to increase coverage. Need to have it in test mode when you turn it on. Can't preload the segment if it is powered off. No magic bullet. Just providing a tool to allow the test engineer to control the init-setup to be in test mode or mission mode.
CJ – have complex systems today with no tools. So the standard is reacting to these complex systems.
Hugh- You switch the chip on and not touch the JTAG tap. No test until send something to JTAG tap. The designer has full control over the chip before we touch the tap. Arguing about touching things in the middle of the chip and not the boundary register.
Hugh – it is a formal handover
Ken – Note that Bill Bruce proposed a protocol called ShutDown that is similar to this
The amount of mush goes down with these 2 instructions. The only mush left is the pins that we have to play with with Preload
CJ – This is a form of ShutDown.
Ken – shutdown concept could be as simple as the IR generates a shutdown signal to the processor which executes some code to put the board in a quiescent state.
CJ – gets complex when code is involved.

System clocks.
Discussion is not "how to define the system clocks", but "do we allow system clocks to be part of the init-setup?"

If you require system clocks you have a catch22 on the PLL. You need to enable them to get the system clocks but then need to shut off PLLs off to put part in safe/cool state.

Carl makes a motion for system clocks to be allowed for init-setup and init-run
Dave Seconds motion

Ken – questions the plural on clocks. Can we put an upper limit on how many clocks. Can you say 1 or 5. How do we solve that issue?
Carl – RUNBIST instructions allow an unfettered number of system clocks.
CJ – issue is if you only say you care allowed 1 system clocks that presents a problem for the IC designers. Almost the same as saying you have to drive your system clock from TCK.

If you have 100 system clocks that doesn't help for board interconnect.
Don't think there is a case where you can say a specific number.

Ken – may add a recommendation to minimize the number of system clocks.
CJ – if voted in would ask the editor to recommend this.
Carol – Agrees having a restriction of 1 clock is like using TCK.
Ken – when I have done init-setup and init-run with clocks on. Can I turn clocks off when I am done so I can run tests or does this imply that the system clock needs to run all the time.
Carl – no it does not imply that.. but the clock may not be able to be turned off. May be free running.
Ken – class of tests where you need a quiet board. So I would want to shut off clocks to run these tests.
CJ – that might need to be a requirement.
Carl – PDL will give ability to state that the clocks should be shut off if system can
CJ – ok... It should be recommendation. Requirement is overboard.
CJ – once we get to init-run. We can go back to init-setup and turn clocks off. So you could shut clocks off and perform other testing with clocks off.
CJ – any hardships?
No one spoke up
Question Called.

Yes (13)

Bill E.	Bill T.	Brian T.	Carl B.
Carol P.	Craig S.	Dave D.	Dharma K
John B.	John S.	Josh F.	Rich C.
Wim D.			

No (1)
Adam L.

Abstain(8)

Francisco R.	Heiko E.	Hugh W.	Jeff H.
Ken P.	Peter E.	Roland L.	Sankaran M*

*was not available at time of vote.

Motion passes
13/1/8

Recommendations are to be added.
Minimize the number of system clocks.
System Clocks should be able to be disabled

Register _ Constraints
No unary operators allowed in an M_I
CJ – leaves only the binary operators in the M_I. if we allow spacing on the binary operator
Hugh- either get rid of the constraints or put the identifier back to VHDL_identifier
White space is a parsing non starter as far as Agilent is concerned.
Reason we don't do this is because parsing is done up front. It screws up everyone's tools that are not using TCL
CJ – nothing to do with TCL here.
Hugh – TCL handles everything as strings. So that is why spaces work here.
Mnemonic_Identifer was great until you put in constraints.
CJ – The Mnemonic_Identifer is parsable with the whitespaces.
Hugh – disagrees.
Bill B – what we should be talking about is prefix_identifier not mnemonic_identifier. Mnemonic_identifer is a beauty contest.
CJ – prefix identifier doesn't have + and – in it.
Bill B- hasn't seen what it "should be". Thought Prefix_Identifier was same in the standard
CJ – that would be a mistake
Carl – had just copied Mnemonic_Identifier for Prefix_Identifier.
CJ –doesn't think that adding whitespace to someone's grammar is a burden.
Hugh – disagrees.
CJ – the thing that it brings you is the separation that is necessary for parsing.
Hugh – not that important. Just makes it look pretty.
Hugh – says that he can parse this but it creates an identifier that can't be used.

Meeting adjourned: 12:07 pm EST.

Summary of Motions Voted on
1 Motion voted on
System clocks should be allowed in Init-Setup and Init-Run
Motion passed 13 yes 1 no 8 abstain

Next Meeting: 5/22/2012 10:30 AM EST

NOTES:

1149.1 working group website - http://grouper.ieee.org/groups/1149/1/

To Join the meeting
https://www.livemeeting.com/cc/intellitech/join?id=2CQ2PQ&role=attend&pw=n%26d%5DNqX%284

Meeting time: Tuesdays 10:30 AM (EST) (Recurring)

AUDIO INFORMATION

-Computer Audio(Recommended)
To use computer audio, you need speakers and microphone, or a headset.
-Telephone conferencing
Use the information below to connect:
Toll: +1 (218) 862-1526
Participant code: 11491

FIRST-TIME USERS

To save time before the meeting, check your system to make sure it is ready to use Office Live Meeting.

TROUBLESHOOTING

Unable to join the meeting? Follow these steps:

1. Copy this address and paste it into your web browser:
   https://www.livemeeting.com/cc/intellitech/join
2. Copy and paste the required information:
   Meeting ID: F9R6S6
   Entry Code: k/d6<@M6j
   Location: https://www.livemeeting.com/cc/intellitech

If you still cannot enter the meeting, contact support.

NOTICE

Microsoft Office Live Meeting can be used to record meetings. By participating in this meeting, you agree that your communications may be monitored or recorded at any time during the meeting.