Date – 10/30/2012
Attendees: CJ Clark, Bill Eklow, Bill Tuthill, Brian Turmelle, Carl Barnhart, Craig Stephan, Dave Dubberke, Dharma Konda, Francisco Russi, Hugh Wallace, Jeff Halnon, John Braden, Ken Parker, Peter Elias, Wim Driessen,

Missing with pre-excuse: Adam Cron , John Seibold,

Missing: Lee Whetsel, Matthias Kamm , Mike Richetti, Neil Jacobson, Ted Cleggett, Brian Erickson, Scott Wilkinson, Jason Chodora , Roger Sowada,
Kent NG, Sam McMillan, Sankaran Menon, Ted Eaton,
Heiko Ehrenberg, Rich Cornejo,
Adam Ley, Bill Bruce, Carol Pyron, Josh Ferry, Roland Latvala,

Agenda:

1) Patent Slides and Rules of Etiquette
2) Use LiveMeeting "Raised Hand" to be recognized and take the flo**o**r
3) Review of ballot comments, if any.

Meeting Called to order at 10:33 am EST

Minutes:
Review Patent Slide – Slide Presented to the Group.
Solicited input from anybody who is aware of patents that might read on our standard.
No Response
Review of Working Group Meeting Guidelines
No Objections

Review of Ballot Comments
Walk through of the 10-28-2012 comment spreadsheet that CJ had sent out to the reflector.

Add Permission
Carl – objection that it is a general provisioning rule and should go into a clause other than the clause for compliance enable pins.

CJ – it is require to have an Observe Only now.

CJ - j permission is not in the right place. This is covered by other rules that are already present
Carl – the fact that it is covered elsewhere is not important to me. That it is in the wrong place is important.
Would like it at B14.1

CJ – ok at dd
Carl – or rewrite cc to cover all 3 classes and linkage or vref it should have an expect value of 1 or 0
CJ – thinks cc already covers it
Not sure what the [ ] means around port ID.
Carl – it's just a bookmark.
CJ – leave cc as it is. This is more general permission. Only referring to linkage power and vref.
Carl – right. In group port id there is a permission for the associated port and in compliance enable there is a permission for a compliance pin.
CJ – so we just need to drop j really.
Carl – yes.

ID number 209 from comments
CJ – the other change is in u1 and u2
The change that was submitted is not what is in the document
Carl – you were excluding the associated port. that is part of rule S
You were not
CJ – 1,2,3,4 are function types. Rule has been around for a long time and described the function type. Input, output, buffer, inout
Carl – what about compliance enable. Do you need an exception for that?
For port id, linkage, vref,
Used rule s so that it would be there for all
Understood why you put the associated port as an exemption but realized that we needed exemptions for those excluded by rule s.
CJ – rule S is not telling me the port ID's need to be input or clock. And if it is a certain type than it needs to be observer only.
CJ – you should provide the list
Carl - think if you go look at subsections of s you can infer it.
CJ – not obvious how to do it
CJ – say on U rather than referencing another rule can we list the 3 types.

#218 from Wim on PDL
CJ – PDL is able to be parameterize. Feels that there are a lot of conclusions being made in this comment.
Peter – Parameterized could be a bad choice of words.
Worried about that crucial information must be changed is not addressed through parameter list. PDL designer might not give all information through parameter list. Because of this you would have to instantiate several different blocks.
Carl – when we define a field you are allowed to specify that the value of that field is deferred. There is a mechanism setup to do what you are looking for.
CJ – there is a BSDL construct for deferred (*) so the tool knows that the value has not been set. So the tool can ask for that value.
There will be some difficulty configuring an IC as a complete novice. Someplace someone has to have an understanding how the IO to be set. That needs to come from a system level

CJ – look at the deferred section on the BSDL and come back to see if that gives you any additional information. That would flag the novice to fill in a value.
Peter – will look at that again.
CJ – shows an example of having deferred values in BSDL
#219 from Wim. Pre and Post conditions
Wim – doesn't want the test engineer to go into a piece of code to know if something is disabled. Wants the tool to be able to do it.
CJ – thinks the use model here is incomplete.
Doesn't think there is a need for the test engineer to change the iproc
Wim – test should say what you should set before you can run the test.
CJ – if we have made an ip block going to a memory(flash). One of the bits in the test register will be a chip set. One of the first lines in the iproc will be drive the CS low.
Wim – what if memory is controlled by a source that you don't have control over.
CJ – possible. Can't address every flawed process.. if I am providing IP then I provide a register with the Chip Select in it. If the IC designer doesn't do something with that then it would be a whole different problem.
CJ – action item for Wim, explain to us in detail what a pre and post procedure looks like and how it provides an advantage and what problem it is solving.
Wim – will try.

#220 – no clear specification how iApply must be implemented if selectable segments are possible in the TDR
CJ – thought we had a normative section that address this better for Wim.
Wim – couldn't find it. Came up during the 1500 support being added.
CJ - execution shouldn't be different. Common goal that we want to achieve.
The issue was the ordering of reads and writes
CJ – what is it that would satisfy you?
CJ – when I write the PDL code not sure what the ic designer is going to do with it.
If I have a group of TDRs than you can write PDL code without knowing the IC topology. IC designer gives you IO that you can hook up. Not forced to put all the test data registers into one TDR. The PDL can be written to allow that flexibility.
Wim – two selectable segments in the same TDR. Concern is how to execute the PDL so that there is no confusion in the PDL engine how to execute the PDL.
CJ – if you write PDL poorly than you can get different output from different tools.
WIM – who says what is right
CJ – when you get the wrong value back
Wim – is completely wrong. Someone can make mistakes and can't have different schemes to execute PDL from different tools. PDL needs to be strict in how it executes
Hugh - Disagrees that PDL needs to be strict. But if you put together strange hierarchy than the tools need to deal with it.
Need to make rule that when you integrate hierarchy there aren't two differentways of doing it.
Wim – doesn't think it would be too difficult. One iApply defines a state and when you do an iRead you want to read that state of your board. iWrite will move the system to the next state.
Hugh – once we put in the segment enables, this opens up the problem with iApply.

Carl – understands what Wim is askig for in this comment
CJ – there is nothing to write into the standard to eliminate people from running bad code. Would have to validate IP/PDL before delivering to customers.
Carl – the way the standard is written now it allows someone to write many iReads and iWrites and one iApply.
CJ – if we force everything to be predetermined we loose flexibility for the IC vendor.
Carl – not saying that at all. If the IC or IP designer creates a dependency the tools under the cover could do all the iReads first before it does an iWrite.
CJ – would like to see the original figure to understand the problem better.

Meeting adjourned: 12:14pm EST.

Summary of Motions Voted on
0 Motions voted on

Next Meeting: 11/6/2012 10:30 AM EST

NOTES:

1149.1 working group website - http://grouper.ieee.org/groups/1149/1/

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