IEEE 1149.1- 2012 JTAG Working Group Minutes

Date – 1/10/2012

Attendees(17): Adam Cron, Adam Ley, Bill Eklow, Brian Turmelle, Carol Pyron, CJ Clark, Craig Stephan, Dave Dubberke, Dharma Konda, Francisco Russi, Heiko Ehrenberg, Jeff Halnon, Josh Ferry, Ken Parker, Peter Elias, Roland Latvala, Wim Driessen

Missing with pre-excuse(2): Bill Tuthill, Carl Barnhart
Missing(12): Bill Buce, Lee Whetsel, Neil Jacobson, Mike Richetti, Ted Cleggett, Matthias Kamm, John Braden, Brian Erickson, Roger Sowada, John Seibold, Sankaran Menon, Ted Eaton

Agenda:
1) Patent Slides and Rules of Etiquette
2) A word about the IEEE
3) Annex C presentation & discussion

Meeting Called to order at 10:30am EST
Minutes:
1)
Review of Working Group Meeting Guidelines
Review Patent Slide
    Solicited input from anybody who is aware of patents that might tread on our standard.
    No new responses.
CJ: Asked Wim to supply the patent number of the patent mentioned in the previous week.
Wim: Forwarded to the reflector European patent # EP 0 768 538 B1.
    Method and tester for applying a pulse trigger to a unit to be triggered.
CJ: Forwarded to the reflector US Patent # 5983378.

2)
    CJ: Has asked the IEEE about rules regarding boundaries of IEEE WG. The notion that 1149.1 can't proceed down certain paths because P1687 exists is pre-empting discussion.

3)
    CJ: Requested feedback on how much of AnnexC has been read by the working group.
    CJ: Reminder that PDL was decided by consensus of the INIT sub-group almost 2 years ago (April 2010). That's why all examples have been in PDL.
    CJ: More than one iApply may be necessary and we must look at what design constraints we are creating.
    CJ: Operation could be as simple as RUNBIST but not likely in today's ICs.
    Wim: Mentioned that INIT became more complicated due to power domain control being added.
    CJ: Power domains were voted on and that's why it is being addressed in INIT.
    Wim: Clarified that Peter and Wim are not opposed to power domains.

CJ: Asked that Wim and Peter come up with an alternate proposal to address power domains, INIT and PDL.

CJ: Wants to make sure we're on the same page.

CJ: PDL was added as an extension (side-file) to BSDL to provide additional configuration and setup information.

Adam C: Believes that INIT_SETUP doesn't need PDL1, that PDL0 is sufficient.

Ken: Hugh Wallace is having trouble attending the meeting. Asked if he was being blocked somehow.

Brian: Of course not. Forwarded Livemeeting info to Hugh.

Ken: INIT is being bifurcated into 2 separate constructs. INIT_SETUP for EXTEST and INIT_SETUP for other interconnect test.

Ken: How simple can we make setting up the EXTEST vs. other test capabilities?

CJ: It does come down to that dividing line. How much work has to be done to get EXTEST vs. other board test.

CJ: If there is 1149.6 support the AC coupling may need to be turned off.

Roland: If we're not interested in error checking, we could use just PDL0 and proceed with basic test.

CJ: PDL0 is a bare minimum yes, but how will any knowledge of the chip be transferred.

Bill Eklow: Has not read the latest draft but asked if PDL0/PDL1 are the same as P1687.

CJ: They are primarily the same but not exactly due to 1149.1 specific test issues.

Wim: All kinds of needs for 1149.1 test are needed with PDL1 but it should be another standard.

Heiko: Neither for or against PDL1. Added that PDL1 would certainly be nice for more advanced test.

Adam C: Asked for clarification of what more advanced test means.

Heiko: Finds that some test will be straighter forward with 1149.1 architecture vs. P1687 architecture.

CJ: Interconnects like a SPI device can be done with register fields and PDL1.

Josh: We do need a procedural way to talk to the TAP, and it should be in 1149.1. I don't see a structural reason to go to P1687 for my designs.

Adam: What's needed from PDL1 for your designs?

Josh: It's the feedback loop. More information needed than just a PASS/FAIL. When it fails diagnostics is needed. PDL0 doesn't provide that.

CJ: Serdes example from John discussed.

Jeff: PDL0 to initialize everything but how much beyond (just do the EXTEST interconnect test) do we need in 1149.1? PDL0 works well for most things but not ideal for all situations. Some pins can't run EXTEST without more setup.

Carol: PDL0 should satisfy INIT_SETUP for most chips, but not all chips. Sees the need for PDL1.

CJ: PDL1 provides a language for more complex setup that would at least be available without going to ad-hoc approaches.

New topics:
None

Action Items: Informal poll of the WG via reflector regarding PDL0/PDL1 requirements due to time running out.

Meeting adjourned: 12:02pm EST.

NOTES:
1149.1 working group website - http://grouper.ieee.org/groups/1149/1/

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Meeting time: Tuesdays 11:00 AM (EST)   (Recurring)

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