1149.1 Working Group Meeting Minutes. November 17, 2009

Attendees :
> Adam Cron
> Adam W Ley
> Bill Tuthill
> Carol Pyron
> Francisco Russi
> Dave Dubberke
> CJ Clark

Agenda:
> Old Business
>> Review Action Items
>> Revisit Pull1/Pull0 – slow rise/fall times
>> Review of INIT Tiger Team
> New Business
>> Self Monitoring

Meeting Called to order at 11:03am EST

1. Old Business
   a. CJ has been in touch with IEEE to get the 1149.1 draft. Currently trying to get the correct format worked out
   b. CJ is working on getting access to 1149.1 website
   c. CJ got in touch with Doug Way and Tom Langford to review their comments on the ballot. Doug and Tom are not available to work with the group on the comments they made.
   d. Figures that need to be update are still outstanding

   e. Pull1/Pull0 – state of pins at UPDATE DR should be valid but on some pins this is not the case do to their slow rise/fall times. CJ would like an indication that the pin is not going to be ready. This would give the tools the ability to wait a period of time before sensing the pin.

> Adam feels that just tagging certain pins slow to rise/fall does not seem complete.   Sees no value in a partial solution. Seems too vague. How do you know what the rise/fall time is?
> CJ – a slow to rise/fall indication just shows that the pin is not ready to observe in x number of TCK signals.
> Carol – Spec says that it should achieve the pull state by next TCK cycle. Are people extending their TCK period to make the pulled pin be correct by the time a capture is done?.
> CJ – yes.. There is evidence of this.

CJ would like to see pull1/pull0 pins tied to the specified TCK frequency. If not ready by 2.5/3.5 TCK cycles give it this attribute, allow pattern generator to define a better gauge as to when to observe pins.

Carol - is it a verification question or silicon question.

CJ – multiple things. Verification of compliance, we would like to validate the chip with a set of patterns of compliance. Would like to observe the output at a specific point in time. After falling edge of tck out of update dr state. Would like to know that the pin responded to update dr. Some pins would not be at that state

Carol feels it is a verilog or modeling problem.

CJ – more of a problem predicting patterns. Not a verilog problem.
Tag certain pins in defined way that are not going to be ready after update + 2.5tck . we can wait until they are ready. Simulation environment would help us in board level environment as well.

Carol – suggest adding a field in the BSDL that would add number of tcks to wait for that pin to be valid.

CJ – would like to add a BSDL extension

Carol – add key word like "slow pull1" that gets a defined amount of time.

Dave – does this make more patterns? What is the net gain? More patterns would mean more money.

CJ – not more patterns but adding how much to delay to wait

Dave – sees this as running slower. Either slower TCK or delay to wait for pins. Test would be running at slowest pin.

Adam sees it not as a thru-put issue but as giving ability to make sure that UPDATE DR is working correctly and setting different class for pull1/pull0 as only these pins are allowed to be slow

CJ – would allow optimization on patterns. Fast when slow pin is not changing in patterns. Also allows simulation to check compliance

Francisco - .6 uses time attributes. Maybe we can use something similar to that.

Adam – proposal sounds like it needs to be more flushed out.

CJ – agreed. But there seems to be some support and a few suggestions that should be considered.

Adam – group should focus on requirements and impacts on current 1149.1 before coding up BSDL.

Adam – mention of rules that outputs should be valid ½ tck or full tck period. If these rules exist than they need to be modified or added to give output timing characteristics or behavior

f. Update on INIT Tiger Team Meeting
Meeting on held Friday 11/13/09
Reviewed discussions from ITC and Last week concerning the INIT state to bring everyone up to speed
Team needs to work on gaining participation from wider audience.
Carol will send out an email to the reflector to ask for more participants

Carol will provide with minutes of meeting

Discussed what to use for a side file for init data

Adam suggested using SVF as a model of what information needs to be conveyed in init data and not use SVF as the syntax.

Francisco suggested using STIL as a model of content.

2. Call for new business (11:47am)

a. Self Monitoring cells

Dave –Self monitoring captures back what it is driving if the pin's voltage is sitting at the half way threshold between a high and low. This is seen when a pin is shorted to another pin and the pins are driving opposite values. When this occurs no failure is detected. A Failure is seen when pin is tired directly to power or ground.

Dave asks the question Is this 1149.1 or driver design issue?

CJ – self monitoring cell doesn't define how the driver works.

Reasons for having self monitoring is to allow us to tell the difference between an open and a stuck at 1/0. Also enhancing testability on pins going out to non BS chips.

Receiver should respond to mid state.

Standard define the capture point not the driver/receiver design

Dave – some guidance or a note, to indicate this problem.

CJ – mid state can't resolve to value you are trying to drive.

Dave – does this fit in with the init state that Carol is looking at?

Carol – drive strength would be addressed by INIT state.

Carol – init would help when going to a open connector and allow you to bias drivers.

CJ – extest receiver could receive a logic 1 or 0 in midstate.

Carol - midstate is programmable but difficult to find correct range

Dave – with adjusted drive strength he can detect failures.

CJ – receiver on mid state would be guaranteed to have inverse of what the drive is driving.

Adam – JJ and Ken who brought up this problem are not present at meeting. We should turn it back to them and get firm proposal from them as to the problem and possible resolutions.

b. Definition of No Connect in standard

Francisco –section B.8.3. Allow the use of "No Connects" to describe actual no connects when using the same die in multiple packages. There is no reference to using no connects this way in the standard.

Decided to not have a meeting next week 11/23/09 due to thanksgiving holiday. Meetings are scheduled to reconvene on 12/1/09

Meeting officially adjourned 12:12pm EST

Next Meeting: Tuesday, December 1,2009 11:00 am EST

Action Items:
- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam to add comment about TRST. Update figure 6.8
- Comment #3 Adam will update language for any proposed change for this section.