1149.1 Working Group Meeting Minutes. January 5th, 2010

Attendees:
> CJ Clark
> Adam Cron
> Bill Tuthill
> Adam Ley
> Francisco Russi
> Carl Barnhart
> Carol Pyron
> Dave Dubberke
> Wim Driessen
> Roland Latvala
> Ken Parker
> Heiko Ehrenberg

Agenda:
1) Roll Call
2) Updates and Q&A on the task lists
3) New Business

Minutes:
> Meeting Called to order at 11:09am EST

1. Update on Task List
> CJ is still working on Directionality Linkage diagram.
> Roland and Carol have submitted their SAMPLE submission over email.
> Adam C. has made progress with Website. Minutes have been added to website.
>
> Sample permission
>> Information from 1149.6
>> Sample more of a .1 issue.
>> Static capture on sample on high speed inputs/outputs
>> High speed serial I/O's not synchronized to TCK.
> Carl – why is this not left at .6 why does it need to be .1
> Roland – committee's point of view it would be .1
> Carol – feedback was that it should be .1 topic.
> Carl – nothing in write-up that says why it should be a .1 issue.
> Carol – will change write up to be inclusive to all I/O and update submission to include info as to why add to .1
> Ken - .1 issue TCK and data rates can be large skew. Sample could be meaningless because of the clocking skew.
> CJ – should we offer guidance as to where this is allowed such as differential pair?

Carol – allowed on any pin. Maybe add different BC types

Carl – Agrees. Intent of .1 would be SAMPLE would actually sample the pin unless sample value may be misleading and meaningless. Recommendation to be supported on any pin that where meaningful data can't be sampled.

CJ – Concern that if it is left in the designers camp to determine it is analog and not digital pin, due to time or functional constraints they make take a shortcut and label the pin as a Linkage Pin.

Tie rule into new INIT section

Want to avoid designers dropping SAMPLE across all pins

Ken – All BC definitions define sample as capturing primary input to cells. Maybe define BC as capturing X's. do we need a new cell.

Carl – Capturing X's does not require a new cell

If we are capturing static values need new cell.

If we use the current cell and have it capture X than we shouldn't need a new cell design.

Ken – just need to be aware of the question.

Roland – JTAG cell doesn't need to chang. There is just different data being fed to it.

Carol – After initialization SAMPLE could work then. Or a mode that would enable SAMPLE with something that you define with INIT.

Carl – INIT command should be written as such no functionality is available until after INIT

CJ – in package files sample is on PI on BC_1. Want a cell with an X/1/0

New Cell that would have allowed X in the Sample position

Carl – Add additional cell entry

CJ – either make new cell as part of standard or allow people to make their own package files.

CJ – INIT and Sample. Want to preserve SAMPLE capability after INIT. Especially in the FPGA space.

Carl – Agrees that if SAMPLE is defined in BSDL than it is not valid until after INIT. None of the boundary scan commands are valid until after INIT is completed. And work as defined in Cell Info BC type

Carl – should differentiate in capturing 1/0 and X's

Carol – INIT is invasive. Not in mission mode.

CJ – there is a difference between 1/0 and X's. Constant value doesn't give too much help. Don't know what it will capture.

Carl – if it reports X than you may be able to gather some information. If it is a constant value returned than you can't get any more data. Stuck doesn't tell me anything.. Toggling tells me something. Making suggestion that 0/1 isn't a good idea.. But X has value.

Carol – times not monitoring PI and expecting X.

CJ – PO.X / PI.X can provide something information. At least SAMPLE is looking at the pin.

PI is already telling what is at the pin

Carl – Stay with original Sample. Some situations where Sample doesn't work. Just saying not compliant is not enough. Need to be allowed to report back X on the pin.

Seeing the pin toggle without knowing what the value should be can aid in debug.

CJ – May just text with explanation is enough. Can allow sample on high speed signal

Carl – need to add normative text and recommendation

Carol – is there support of concept of making SAMPLE an optional instruction? Or do we want to simply modify the current SAMPLE

CJ – want to modify the current SAMPLE. Change restriction on Sample

CJ – if not in mission mode no need to Sample what is on the pins. But when in mission mode we should be sampling.

CJ – Could allow Sample on the single ended side of the differential pair.

Carl – recommendation in .6 if a differential put a sample on the output of the test receiver.

CJ – Observe Only's on the receiver side. Is this where the difficulty are?

Carol – Still an X due to power level mismatch. If initialized this is not a problem. In mission mode can we have an X?

Carl – until mission mode or test mode initialization sample doesn't work.

Once the board is working after initialization SAMPLE should capture something

CJ – Bottom line you need INIT before SAMPLE. If you do it before it doesn't do anything for you. Once INIT is finished I/O is conditioned and you should be able to SAMPLE.

Carl – state normatively or descriptively that SAMPLE is not available until after INIT is done. Can not SAMPLE until there is a system to SAMPLE.

CJ - .1 will be able to setup system without software. Can run INIT

Carol – INIT is intrusive. Normal Mission mode can not be guaranteed to run after it. Will run in normal JTAG realm.

Ken – should SAMPLE be mandatory given all these problems.

Different views on value on SAMPLE. What is value and cost of SAMPLE.

Carol – until test receiver for .6 SAMPLE has been most problematic. Most non compliant occurrences.   SAMPLE is trouble!

Ken – does any one care?

Carol – rare people complain about it. Will call pin Linkage if it is not working so they don't get call.

Carl – decreases coverage of board test.

Carol – shouldn't get used in test

Carl – should only be used in Lab Debug

If you don't have functional SAMPLE it will cost more to debug board.

CJ –Don't have 100% devices with boundary scan. Need to see what pins connected to non boundary scan are doing

Carol – can't you see pins toggling while in extest

CJ – can't put part into extest because it would stop the chip from working. The whole chip goes into extest

Carol – SAMPLE is not part of board level production tests.

Ken – in production board tests SAMPLE is not work horse. In R&D SAMPLE is used.

CJ – feels there is high quantity of small board tests that use SAMPLE rather than ATPG. Customers never generated patterns they just use SAMPLE.

Ken – Cost and Benefit. Carol says cost is bigger than can imagine. CJ says Benefit is bigger. Does anyone care?

Dave – Intel doesn't put much emphasis on SAMPLE. EXTEST is the primary goal of that function.

Dave – cost going into test features and verifications that go into Silicon as well.

Ken – what we are discovering is all the issues going on with Sample. Does the changes and efforts warrant the benefits?

Carl – SAMPLE should be done on a pin by pin basis

Francisco – easier to identify the pin to generate X?

CJ – is for this path. Seems to be the middle ground for what to do with SAMPLE.

Carol – in last revision where sample and preload split there was a strong camp to make SAMPLE optional.

Ken – correct that is why we divorced them. Standard voted down making SAMPLE optional

CJ – Correct.

CJ – good to hear from FPGA people because they have a lot of IO

CJ – thinking at terms of capturing at pin. Maybe should think about SAMPLING at the core and may resolve some issues.

Carol – no sampling point outside the analog shell.

Roland – designers have issues implementing SAMPLE. Not sure of details why.

Carl –making SAMPLE optional on a pin by pin basis is a valid way to go. PI.X would warn anyone using SAMPLE instruction that you can't count on it. Need to look at what is going on.

Carl – If voted on SAMPLE being optional it would not pass.

CJ – Agrees.

Ken – doesn't want to spend a lot of time on a non-issue.

Carl – if Freescale has problems with SAMPLE (IBM had difficulty as well) just say it captures X. Don't force someone to be non compliant because of a business decision.

CJ – no need to remove SAMPLE all together.   Want to relax restrictions on difficult pins. Just cautioning on wording in standard so people can't take advantage to make all pins SAMPLE X. Want to help where difficult and keep SAMPLE where it is not difficult.

Carol – will update document with Feed back.

Meeting adjourned at 12:30 EST.
Next Meeting: Tuesday, Jan 12 11:00 am EST

Current Issues listed and who will champion that issue.
1   Observe only. –   Ken
2. Directionality linkage. - CJ

3. Power Pins. - Heiko
4. Pairing power pins with functional I/O - CJ
5. Sample / Capture. – Carol (Freescale)
6. TRST included in PCB level diagram. – Adam L.
7. Slow to Fall/Rise signaling issue – CJ
8. "No Connect" – CJ and Francisco.
9. Device ID – Still needs work
10. Low-Voltage self observe shorts coverage problem – JJ & Intel
11. Init – Carol & Carl

Action Items:
- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.