1149.1 Working Group Meeting Minutes. January 26th, 2010

Attendees:

CJ Clark, Bill Tuthill, Carl Barnhart, Carol Pyron, Heiko Ehrenberg, Wim Driessen, Adam Cron, Ken Parker, Dave Dubberke, Adam Ley, Francisco Russi, Roland Latvala

Agenda:

11:00AM

1) Adam Ley – TRST

11:12AM

2) Ken -- OO on I/O pins

11:35AM

3) Heiko – power/gnd pins called out in port list instead of linkage

11:45AM

4) Francisco – No Connects in packages

Minutes:

Meeting Called to order at 11:04am EST

Review of individual tasks

TRST – Adam L / CJ

Adam L was not ready to discuss TRST at this meeting and will present more information at next meeting

CJ provided a diagram. Needs updating

Ken – should we modify the other 2 examples? CJ has modified the most used example.

CJ – not necessary to update other examples. Not much value.

Ken – agrees

Adam – did we agree to add as addition diagram?

CJ – was believed to be a replacement.

Carl – with correction that Heiko

Carl – motion to adopt the addition of the new TRST figure that CJ provided with TRST* being the label. (fix proposed by Heiko)

Carol 2nds motion.

Adam Ley opposed

10 yes and 1 no.

INIT status

(slides from Carol)

Rules are at 85%

Discussion text content at 50%, actual text 10%

Actual incorporation into the dot1 text at 0%

Plan to add into chapter 8

New section 8.16 and up that describe the new INIT instructions.

Insert new chapter between the existing chapters 12 and 13 to cover all the theory and reasoning of INIT.

In Annex B describe new BSDL attributes needed to support INIT

Carl- need modified text of dot1 and will fold in INIT changes into that document.

CJ – a lot of work that needs to be done. May need to have 2 balloting for INIT and updates to DOT1. May be too much work to meet schedule.

Carol – biggest open issue is side file definition.

Ken – 1532 standard has a side file problem and was able to deal with it. May be a good place to look to see how they did it. May be able to lift some ideas from there.

CJ- time line- would be looking at draft at spring time and balloting in summer and in august we would be submitting. And meet REVCOM in September (http://en.wikipedia.org/wiki/IEEE_Standards_Association)

Heiko – Power/ Grounds in Port List

Heiko provided Email that describes problem and solution that he proposed.

CJ – real problem that the people in the trenches need to deal with

Software guesses what the power nets are. Not always a perfect process.

No feed back mechanism to show that the process was correct.

Carol – wants to maintain the usage of Linkage pins. Leans towards not putting power pins in ports.

CJ – more work to parse BSDL extension. Already changing parsers to add * might as well change for adding power to port.

CJ – problem has been known. How do you identify the topology and what is connected to power and grounds.

Ken – Linkage has been hiding information – a catch all. How do we get more information in such a way that the people who want it can get it and those who don't want it don't have to get it. How do you get the info in such a way to write a ATPG program to get it right.

Ken – Looking for CJ's slides.

CJ – will send them in email

Ken – is concerned that we pick a way that is a true contribution to the standard and not a "backassward" way

Francisco – No Connect

Ken proposed a motion – sent email with proposed syntax

Motion – change syntax description in B.8.7.1 (of 1149.1-2001) per the syntax addition shown above and amend the semantic check B.8.7.2d) as shown in Email from Ken. The description text in B.8.7.2 is to be modified to sync up with the above changes.
// email from Ken added here

B.8.7.1 Syntax

<device package pin mappings>::= <pin map statement> <pin mappings>

<pin map statement>::= **attribute PIN_MAP of** <component name>**: entity is PHYSICAL_PIN_MAP;**

<pin mappings>::= <pin mapping> {<pin mapping>}

<pin mapping>::= **constant** <pin mapping name>**: PIN_MAP_STRING:=** <map string>**;**

<pin mapping name>::= <VHDL identifier>

<map string>::= " <port map> {, <port map>} "
<port map>::= <port name>**:** <pin list>
<pin list>::= <pin ID> | **(**<pin ID> {, <pin ID>}**)**
<pin ID>::= <VHDL identifier> | <integer>

Proposed is a modified syntax (mods are in red):

B.8.7.1 Syntax
<device package pin mappings>::= <pin map statement> <pin mappings>
<pin map statement>::= **attribute PIN_MAP of** <component name>**: entity is PHYSICAL_PIN_MAP;**
<pin mappings>::= <pin mapping> {<pin mapping>}
<pin mapping>::= **constant** <pin mapping name>**: PIN_MAP_STRING:=** <map string>**;**
<pin mapping name>::= <VHDL identifier>
<map string>::= " <port map> {, <port map>} "
<port map>::= <port name>**:** <pin list>)
<pin list>::= <pin desc> | **(**<pin desc> {, <pin desc>}**)**
<pin desc> ::= <pin ID> | ***
<pin ID>::= <VHDL identifier> | <integer>

Semantic check (rule) B.8.7.2 d) today says:

d) The <port map> for a <port name> defined as **bit** in the <logical port description> shall be defined
using a single <pin ID> without a subscript. The <port map> for a <port name> defined as a **bit_vector** in the <logical port description> shall be defined using one or more <pin ID> elements within parentheses.

Proposed is a modified rule:

d) The <port map> for a <port name> defined as **bit** in the <logical port description> shall be defined
using a single <pin desc> without a subscript. The <port map> for a <port name> defined as a **bit_vector** in the <logical port description> shall be defined using one or more <pin desc> elements
within parentheses.

Motion: Change syntax description in B.8.7.1 (of 1149.1-2001) per the syntax addition shown above, and amend the semantic check B.8.7.2d) as shown above; moreover, the descriptive text in B.8.7.2 is to be modified to sync up with the above changes.

//

Carl – does this imply that the BSDL that conforms to this will not work in a BSDL in a previous parser

If we adopt this we are dropping backwards compatibility

Ken – yes we would drop backwards compatibility

Carl – likes change but wants to understand that we are voting on dropping backwards compatibility.

CJ – we over emphasize backwards compatibility. Other software such as packages from Microsoft are not backwards compatible with previous versions. Earlier VHDL parsers can not parse code from newer standard updates.

Ken – legacy parser will see a conformance statement see and give a warning then and not give an obscure parsing error when reaches the *.
Carl – was 2001 backwards compatible
Ken – no it was not.
Carl likes change
Carol likes it too
Adam L – point of information : Matter for the year extension that is on the package not conformance statement. Conforming devices could choose to adopt the new syntax.
Syntax for 2001 is backwards compatible. New semantic rules but believes the syntax is backwards compatible.
Carol – should wait til next week to vote. To do this in the same BSDL with 2 different packages, both packages would have to share id code.
Adam L – no provision to share ID codes in different packages.

Carl – take this as first item for next week.
Ken – agree to allow people to look.
Carl – first item of business next week.
CJ – motion will be put it on agenda for next meeting. Not necessarily at the start of business
CJ – group will adopt that voting will not occur outside the scheduled meeting time to be fair for people that need to leave at the designated end time.

Carol – motion to adjourn. Seconded

Meeting adjourned at 12:07 EST.
Next Meeting: February 2nd 2010 11:00am EST

Motions made

1. to adopt the addition of the new TRST figure that CJ provided with TRST* being the label. (fix proposed by Heiko)
    a. 10 yes
    b. 1 no

Current Issues listed and who will champion that issue.

1 Observe only. – Ken
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale)
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – CJ and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.