

1149.1 Working Group Meeting Minutes. March 16th, 2010

Attendees: CJ Clark, Bill Tuthill, Adam Cron, Dave Dubberke, Heiko Ehrenberg, Carol Pyron, Francisco Russi,

Missing with pre-excuse: Adam Ley, Ken Parker , Wim Driessen

Missing: Roland Latvala, , Bill Eklow, Carl Barnhart,

Agenda:

11:00 Review any further input on the draft?

11:15 Linkage_in, linkage_out, linkage_bidir, linkage_buffer, linkage_package

Power_1, Power_0, Power_neg, Power_ref, Power_other

Could we live with these choices?

11:40 INIT

Minutes:

Power/Linkage

Carol is unsure about the use of Linkage_BIDIR and what ATPG tools will do with it.

CJ - ATPG tool sees it , it will not touch net.

Carol - What do you do with linkage_in,

CJ - Would feel free to drive pin from a boundary scan device (separate or same device)

CJ – need models in place to make heads or tails out of topology. Would help make tools more push button. Tools can check power and linkage pins to

CJ – linkage bidir is active analog bidirection and don't know what direction it is going in.

Carol – many times pins can be functionally be one direction but given the randomness of power up the pin might need to be a bidir because of powering up in an unknown state.

Discussion on BC_6 cells. BC_6 cells make testing a single device on a board difficult. This discussion will be taken offline with CJ and Carol.

CJ – Can we live with current choices? Or do we need to tweak it.

Dave – Heiko's choices are different that what is listed?

CJ – haven't listed what Heiko had listed.

CJ – Can live with POER_POS, POWER_NEG, Ground, POWER_REF, POWER_OTHER.

CJ – Analog_in Analog_out, Analog_buffer, Analog_package, Analog_

Carol – Freescale devices have a power pin that is used to blow electrical efuses.

Francisco – is it a power pin?

Carol – yes. it is a true power pin. Certain VDD must be set to blow fuses. Not sure how to document this with the new power attributes.

CJ- what do you do at board level

Carol – has to be connected to a power

CJ – the nit would just be a POWER_POS or POWER_REF. Would most likely be POWER_REF because it is a reference voltage.

Heiko – With programmable devices such as Actel specific programming voltages are needed that are different than the supply power.

CJ – ok with leaving Power Other.

CJ – purpose is not to have modeling language for power. Purpose is for during ATPG identifying what is at the board level. Classify that it is a power pin and not linkage pin. Identify pull up and pull downs construct by knowing the POWER_POS, POWER_NEG or GROUND attribute

CJ – these attributes not trying to model all power pins.

Carol – VDD pin identified as POWER_POS and goes to net that has sink on chip. From an ATPG point of view what would you do with that information.

CJ – Power_POS would tell you a lot about the constructs of pin

Dave – net would tell you that one end is shown to be a power net and if the other end is a resistor than the tools would know how to drive that pin

CJ – this is what we showed. Knowing if the net is a power rail it helps improve the ATPG. FPGAs have many power pins. If we can identify if it is a power rail or reference voltage we can determine if it is a pull up resistor or pull down resistor. Also added checks for tools

CJ – in complex devices you won't have a way to narrowly define power pins. Just want to understand where resistors go and knowing they are connected to a power rail will make life easier for the tools to determine the resistors functions.

Francisco – what do you expect to be POWER_OTHER?

CJ – not sure. Maybe a catch all for programming pin like Carol is defining.

CJ – POWER_POS, POWER_NEG, and GROUND covers most everything.

.POWER_REG will pick up some left outs for the IO voltage.

CJ removed POWER_OTHER from list

CJ –Rule of thumb for POWER_POS - do they have a potential greater than 0. Than that pin would be POWER_POS.

Carol – Do we want to distinguish between power to IOs and Power to core?

CJ – no. not at this time.

CJ – first step is to understand the difference between analog and boundary scan pins and power pins. Next stage is to map the power pins to IO to narrow down faults to reference voltage pins.

CJ – Jacobson and Parker ITC paper. BSDL extensions for mapping IO signals to power rails. Area we would like to go.

Francisco – highlighted some power domains for an ASIC in email. If you had different power domains and want to identify each would you call them all POWER_POS. if you put POWER_POS and POWER_NEG all positives are +0 all the negatives are -0. Do we need this to figure out the power nets?

CJ – tools will identify power domains from topology. Nets will be separate.

Francisco – we won't make distinction in BSDL.

CJ – right not at this point.

Francisco doesn't feel all possibilities are being explored for options for POWER_ attributes

CJ comments that he can't incorporate all suggestions into the standard

Adam - don't want to have something that is going to be voted on every year as something is changed to accommodate changing technology

Carol would not like to vote on the standard every year either.

CJ is for having the standard change along with the technology. Voting for standard change every 2 years would not be that crazy of an idea.

Adam - we are dealing with a volunteer force of workers. Don't understand why we have to finish by April to get it out by May and leave things on the table to get left out by this date.

CJ - Have to have a cut off date to avoid feature creep. Need to make a release even if there are some issues. Seems silly to hold back on all the improvements we have to get everything out

CJ - there are improvements that I want but know there isn't enough time to get everything in

Adam - should have at least a little discussion on different point of views.

CJ - list could be endless

Francisco - power is such a hot issue today. Lots of chips are designed with multiple power domains. Would help users if we can identify the different domains. Possibly with different attributes

CJ - how will it help?

Francisco - POWER_POS will have an expected value of a power pin rather than dealing with entire spectrum could hone in on a power pin with attribute. Helps the end user if the pin fails that is the information up front that the user gets to start with. Pointing the user in the right direction

CJ - Not enough time in a call to develop ideas on the phone. Would like to understand issue better and would need more information to do that.. This idea needs to be fleshed out more.

INIT

Carol - init is making good progress

Carol - would like to see init make next round of balloting.

Carol - stated goals at ITC was to ballot INIT.

Carol - last meeting.. how to get it in the standard.

Integrate it through the standard

New annex. Self contained with few references to it in the main body.

Carol - 2 new instructions in the instruction section. Impact could be own annex.

Carol - need feedback from CJ.

CJ - easiest way is as a separate supplement.

Carol - hadn't considered.

CJ - trying to be practical. Lots of syntax in attributes. Might be into summer time to October working out grammar.

Francisco - hire a technical writer?

CJ - don't understand

CJ – difficulty not in capturing information. Difficulty is agreeing on syntax. Technical Write will not make those decisions for us.

CJ – Hierarchical example is troublesome.

Carol – knew there would be controversy there.

Carol – pink is controversy , green is a comment. Blue is syntax.

CJ – Wants to change the syntax. Sent changes in email to carol and group

Carol - Can live with changes that were made in CJ 's example email

Carol – might be useful to have text associated with a mnemonic so the tools could relate to the user. (“toolhelp” or “INFO” - comment passed forward to the tool)

Carol – BSDL uses brackets?

CJ – it does but not parentheses are better. In TCL you use ()

Carol – Can change Brackets to Parentheses

CJ – would need to work these out during the week in email. And not in the standard meeting.

CJ will send out mail regarding the changes to Carol's example of INIT.

Carol can not find the Paper from Neil Jacobson and Ken Parker on power pins. Will track down and send to her.

Meeting adjourned at 12:17 EST.

Next Meeting: March 23rd 2010 11:00am EST

Current Issues listed and who will champion that issue.

1. Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1

- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.