

December 3, 2010

Minutes of IEEE 1149.1 - Initialize Sub-Group Meeting

Attendees:

Carl Barnhart
John Braden
C J Clark
Dave Debberke
Heiko Ehrenberg
Roland Latvala
Ken Parker
Carol Pyron
Francisco Russi

Minutes:

Today's meeting was dominated by a discussion of IC_Reset

- Carol: we have not discussed when (what TAP state) the reset would take effect
- Carol: the consensus seems to be that we will have a TDR to allow selecting among possible resets (no disagreement.)
- Ken: Least Significant Bit (LSB) of TDR should be master or global reset, and any other bits providing finer control.
- Ken: consensus was that reset would not release Clamp Persistence.
- Carol: keeping the operations atomic (independent) makes life easier for chip designers.
- Carol: what is the intersection of IC_Reset and INIT?
- Carl: there is a lot of overlap; both are preparing the chip to perform a specific test or system function.
- Carol: differences in the details; they probably end up at different states.
- Dave(?): why are we preserving clamp-persistence across reset?
- Carol: having them independent makes life easier without burden on test programmers.
- Ken: test flexibility, can prepare the chip internals while still holding th I/O in clamp.
- Roland: is IC_Reset a test instructions?
- CJ: no, it is a non-interfering instruction; clamp-persistence determines if the I/O are clamped.
- CJ: Lots of tests (besides interconnect) are kicked off by 1149.1 and may need specific resets in between.
- Roland: this seems to be very chip specific and difficult to standardize.
- Carol: when does it execute?
- CJ: when we load the TDR using a "run" bit in the TDR.
- Ken: use the RTI TAP state after TDR load.
- Carol: if we use RTI, we need to clear TDR at Update-IR because some controllers always go through RTI.
- Roland: This leads to a lot of design tradeoffs.
- Carol: on complex chips, these tradeoffs are already being done, and this is all optional so does not force any new tradeoffs.
- Ken: How does reset assertion/de-assertion normally work?
- Carol: Assertion of reset pin (or entry to RTI) generates assync reset to a lot of flops, de-assertion (exit of RTI) is synchronized and used to start boot state machines and possibly other logic.
- Ken: how is time in RTI specified, TCK only or wall clock time?
- Carol: TCK only for INIT, maybe the same for IC_Reset?
- CJ: we may need to revisit that due to the high frequency TCK allowed on some chips which would lead to very high TCK counts even if the tester could not support that high

- frequency TCK.
- Carol: Summarizing where we are at:
 - Required TDR, minimum 1 bit.
 - TDR cleared by Update-IR.
 - LSB of TDR is master reset.
 - Time in RTI is equivalent to assertion time of reset pin.
 - Use field/mnemonic to document TDR bits.
- CJ: IC_Reset overrides at least some of INIT results.
- Carol: would like a BSDL parm that specifies whether INIT results are preserved or not.
- Ken: I think any boot sequence overrides INIT results.
- CJ: In Altera FPGAs, the I/O characteristics are independent of programming the function. For Xilinx, they are not. We have to assume that the I/O are changed by IC_Reset.
- Roland: should we have TDR bits to protect the I/O?
- Carl: Users have had user instructions for INIT and reset for a long time. We standardized INIT because it needed to be included in the ATPG test automation. There is no similar need for IC_Reset, so why are we attempting to standardize it?
- CJ: for teaching and instruction on how to do this, as well as making it easier for chip designers to include the function, and easier for chip consumers to request such a function.
- Ken: There is value in having standard instructions and procedures for common functions, even if not automated.

We then had a discussion about the integration of the Clamp-Persistence text. CJ thinks it would read better if the two instructions (normative and descriptive text of C.3) was moved to the end of Clause 8, but C.2 and C.4 would remain an Annex. Ken and Carl argued for keeping it all in one place, making it easier for experienced engineers to find it all, and Carl argued that he is concerned that once some part of it ends in the Standard Body, there will be ripple effects requiring changes all through the document. Of major concern to everyone is to not create new clauses (chapters), as would be needed if the controller or TDR were moved to the body, which would mess up the clause numbering known by users and referenced by other Standards. Carl suggested talking to someone with strong knowledge of Standard structure about this problem.

The meeting adjourned abruptly on time.

Current Status:

Formalize Rules – In progress.

BSDL Constructs - – BNF coding in progress, semantic checks in progress.

Formalize PDL constructs – In Progress.

Incorporate INIT and Clamp-Persistence into 1149.1 Std.

Actions:

- Carol to provide custom bidir IO example diagram.

Next meeting date:

Same time, Friday, December 10th.

We are currently planning a meeting on December 17th as well, then no more for the year.