Date – 05/06/2011

Minutes of the IEEE-1149.1 Working Group Friday meeting

Attendees:
Adam Ley,
Brian Turmelle,
Carol Pyron,
Dave Dubberke,
Craig Stephan,
Roland Latvala,
John Braden,
Carl Barnhart,
Francisco Russi
Ken Parker

Meeting called to order at 8:33 am MST

Current Draft: P1149 1 Draft 20110502.pdf (_clean.pdf)

Agenda:

- Status from the editor
- Discussion of Francisco's proposal on boundary register segment rules (Sub-clause 9.2)
- New business from Ken (On-chip silicon ID)

Today's Minutes:

Status from the editor:

Annex B:

- Waiting for mnemonics and register fields definitions
- Ken reworking 'shall' statements within Annex B
- Adam will look at the changes Ken is making
- Ken – I took a first cut and what is there is not complete.

Annex C:

- Also in progress

Discussion of Francisco's proposal:

We discussed Francisco's proposal to standardize rules for a side file that defines marketing pin names and physical pin mapping and order of boundary register segments. This is in reference to permission 9.2.1.e. The concern is that there are currently no rules which define the boundary register cell ordering within this file and this impacts synthesis and stitching and the resulting design and BSDL file.

- Carol displayed Francisco's email from this week showing all the possible combinations of boundary segment ordering within a 'physical pin map' side file for a given boundary segment.

- Francisco explained his concerns about control, output, and input cell placement of segmented boundary chains and was in favor of defining rules for the EDA vendors to follow to standardize the work/effort to define the order for placement optimization and boundary cell ordering. Today this file has physical pin and marketing pin information but little/no information on the boundary register definition
- The group discussed how this is not an industry wide issue. Companies each have their own solutions.
- Ken mentioned that BSDL only describes the finished design, and is not concerned about how the EDA tools arrive at a finished BSDL.
- Carol understood the issues Francisco is presenting but thought other EDA forums may be better for addressing these issues since these issues don't affect board test.
- Carl mentioned that optimized chain order is based on physical placement and this issue is not an industry wide issue. This is an in-house issue.
- Francisco reemphasized that he brought this up as an issue for this Standard since this information is missing. The physical pin map order in BSDL doesn't explain how it came to be. In this side file we have pin and bsr segments, but depending if you are on east or west side of the die you need to know the order.
- Carol thought that if we were to standardize this others will ignore it anyway and use their own tools and methods.
- Francisco asked for a motion to discuss further. Carl said there is no voting on Friday but we can take an informal poll.
- Carol defined the motion (poll) as "Formalize a side file format for input to EDA tools to drive the order of the BSDL boundary stitching."
- Poll Results:
    - Adam – no
    - Brian – no
    - Carl – no
    - Craig – no
    - Dave – no
    - Francisco – yes
    - John – no
    - Ken – no
    - Roland – no
- Carol reemphasized that this topic is be better suited for an EDA forum.

New business from Ken (On-chip ID)

Ken brought up new business. At the VTS Symposium he met with Matias Cam (sp?) and discussed a topic raised before by Bill Eklow about the On chip silicon IDs. Matias wanted to know how to kick start this again. Ken told him we don't have time for side shows, and that he needs to put together a presentation for the Tues meeting and in a 15 minute proposal the WG would have to be a ready to vote on this proposal. The concept

is like another User Code instruction. It has to be straight forward and he must justify why it is important.
We had some short dialog on this topic:

- Carl - asked is this a digital serial number?
- Ken mentioned it would be an optional standardized instruction
- Ken – We may specify the lsb. 0=bypass 1=silicon ID
- Carol – Was he coding meaning into the bit fields?
- Ken – I haven't seen his proposal. Maybe 30bits or 20bits
- Carl – After it fails you want to track it back to a lot
- Francisco – Ken why not aks to increase the 32bit device ID field?
- Carl – The serial number is only if it fails in the field
- Carol – It should probably be a separate instruction

Ken said Matias will go offline and present us something we can vote on in 15minutes, so that this doesn't delay the standard with feature creep.

Meeting adjourned: 9:17am MST

Action Items:

- WG to continue review of Annex B

Next Friday Meeting:

- Next week Friday May 13, 2011