

Date – 13/Jan/2012

Minutes of the IEEE-1149.1 Working Group Friday meeting

Attendees:

Adam Cron
Adam Ley
Brian Turmelle
Francisco Russi
Carl Barnhart
Craig Stephan
CJ Clark
Ken Parker
Roland Latvala
Carol Pyron
Dave Dubberke
Jeff Halnon
Josh Ferry
Ted Eaton
Heiko Ehrenberg
John Braden
Peter Elias
Roger Sowada
Bill Eklow
Bill Bruce
Sankaran Menon

Excused:

Meeting called to order at 9:35 am MST

Current Draft: See private area for latest draft

The agenda for the meeting today:

- Continued CJ's presentation and discussion of PDL

Meeting

Ted opened with request to continue to define the minimum requirements, and leave the procedural aspects to another standard.

CJ commented that 'minimum' means different things to different people.

Ted suggested we could to show a P1687 tutorial .

CJ agreed Ted could do that.

Carol added that there are different audiences of 1149.1. Different consumers, and she asked CJ to go through his presentation in a simple manor.

CJ's Presentation Highlights:

Slide 1:

- BSDL
 - Reg fields/mnemonics
- Package Files(s)
 - Reg fields/mnemonics
- PDL0 file(s) IP blocks
 - procs (predefined)
- PDL0 file(s) IC level
 - procs (predefined)
- Database

CJ discussed the initial scan frame was setting up iRead(expected values)

Carl asked about RESETVALS

CJ clarified the DEFAULT and SAFE values are used

Ken asked if SAFE value has its historical BSDL meaning

CJ Yes it is similar to the safe value of the boundary register. It's the value which leaves things in a 'off/safe state when there is nothing chosen to be scanned in.

Deleted: thought so, but thought the Std didn't have to be explicit on this.

Slide 2:

- iWrite
- iRead (expected)
- TDO XX
- Using Mnemonics

Slide 3:

- iGet example:
- IN, EXPECT, OUT fields get populated by this command

Group discussion points:

Board level Tools would have DATABASES and PDLs from each IC vendor in their tool memory space

Adam C asked about the definitions of PDL0 and PDL1 now, there seems to be some merging of these commands in 1149.1

Note: there has not been any merging of PDL0 commands with PDL1
IfMatch and IfMatchloop are PDL0 commands

CJ asked to hold off that thought for now

CJ pointed out that the tools will process PDLs sequentially for each IC since this is prior to test execution, before the iAPPLY(s) so this does not impact test time.

All of this is building the scan frame. The iAPPLY records this in the proprietary binary tester formats.

Deleted: proprietary

By default PDL scan frame data is not merged between ICs/ However he mentioned for INIT_SETUP the iMerge may need to be the default.

Carol/Ken added discussion about aligning (parallelizing) all this between ICs and this is where it gets more interesting.

CJ added that while ICs with INIT_SETUP are being setup, the other non-init ICs are loading bypass or device-id or SAMPLE

CJ added that INIT_SETUP proc has to be done for all ICs on a board before going to INIT_RUN.

CJ added for other procs you are not required to do them additional IR scans, so IR scans are sticky as long as you don't touch them.

Ken asked if one PDL ends before the others (proc), but the others have more data to process, then you repeat the scan data. Extra dr-scans. OK if data is always the same or 'no-op' equivalent. However if a one of the new 'pulsing cells' the extra scans could be an issue. The perhaps Adam's idea of managing frames bottom to top may be good idea.

CJ added that pulse zero and pulse one only fire once each. If you have a pulse one circuit, you get a 'one shot', and the tool is responsible for putting the cell back to zero in the next scan frame. The tool is responsible for this such that pulsing does not occur,

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CJ confirmed Ken's question is valid. There are push and pull concepts of moving the data into the functional domain. (eg: Go bits, Update-DR). Designers need to preserve the INIT_SETUP data, so cannot load over this with SAFE or DEFAULT data, SOMETHING has to be scanned, so it makes sense to reload the same INIT_SETUP frame again when needed.

Adam Ley asked if the init-data register was the only register that INIT_SETUP could target. Is that correct?

CJ said that was the current understanding, but that could be changed perhaps. Issues like power control maybe, but he cannot think of one at the moment.

Adam added that in general the merging process would get extremely more complex if that were the case. CJ agreed.

Carl added that there was no current rule against this in the draft.

CJ added we may want to vote on this, but init-data should be the only register allowed during INIT_SETUP.

Adam concurred that this should be a rule.

Jeff added that IC1 and IC2 procs are not linked in your prior comments to Ken. If there are power issues, a power domain bit in IC1 could control a domain in IC2. This is not uncommon. Power controls can be standard gpio off of a processor core. If power sequencing is part of the INIT process then you cannot say IC1 and IC2 are independent of each other.

CJ responded that this is a misunderstanding. The scan frames are independent of each other for each IC. You are bringing up board level constraints and init setup that have these dependencies. This discussion is for IC level only, since some had issues with board level issues managed by this Chip Level Std.

CJ added that PDL1 could be used to help this board level type issue. Maybe INIT_SETUP or some other instruction needed to get power out of the one IC to power up the other.

Jeff wants to defer the PDL0 and PDL1 discussion for now.

CJ said we won't be able to solve all the board level issues.

Carol asked if Adam or others had other questions. None at this time.

CJ asked if the INIT_SETUP should always be merged? It's not on by default, so to address Ken's concerns we may want to think about this.

CJ added that one use model for PDL0, including the match loop constructs, can be used across industry for ATE vectors, jtag testers, and so on. For production PDL0 may be what is needed for tester hardware use.

CJ asked Bill Eklow about the use models. His views on PDL0 only for INIT_SETUP

Bill commented that the tool vendors have the most stake in this discussion. From his standpoint we may have enough to deal with for PDL0 only, but as technology evolves, this may not be enough in the future. The progression of the boundary register and its initialization was passed over last time. If we allow both, how do we guide on use of

PDL0 and PDL1 going forward? If you allow both, this will let the market decide the direction we are going.

CJ brought up that if INIT_SETUP cannot be fully done in PDL0, how do we create a rule/permission for the iProc init_setup. Recommend it is done in PDL0?

Ted brought up that we can describe the INIT hardware in BSDL and punt on the procedural aspects of this. Even though CJ thinks we are almost done, he feels there are other aspects of PDL that the WG does not fully understand, and we may have quite a bit more work to do.

CJ: The technical content is done, there are tweaks to be made, arrangements of commands to suit the WG. We do in fact have semantic rules for PDL0 and the two commands in PDL1

Bill added that for the 10 year issue, you must work on a Std within each 10 year window time frame. For Ted's position, you could reopen the Std a year after it was releases, although that may not be the best approach.

CJ agrees we need to have something final and operational, before we close the door on this Std, so that could be a problem.

CJ has a couple more slides, and perhaps discuss on the reflector. PDL1 has just two proposed commands plus the TCL.

Ken asked, CJ you said branching can resolve into an iApply. How do you manage this?

CJ added that if then else can be operating on the database, not on the data coming back. iGet on a register with IN or EXP only operates on the database itself.

Ken asked for this distinction to be clarified.

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CJ said iGet OUT is not merge-able and not desirable on the INIT_SETUP

CJ added that the 3 fields that iGet processes, 2 are from the database to set up the scan frame, and the 3rd is the TDO value. The third form of iGet is non-mergable.

Carol said Adam has another question.

Adam Ley will ask his question on the reflector, since we are out of time.

CJ concluded with some closing thoughts on INIT_SETUP. Two procs provided by IC vendor to turn off PLL and ac-coupling for example. Need to follow up offline this coming week.

Meeting adjourned: 11:02am MST

Action Items:

- Continue PDL discussions over the reflector this week.

Next Friday Meeting:

- Next Friday meeting is on 20-Jan-12