Date – 04/15/2011

Minutes of the IEEE-1149.1 Working Group Friday meeting

Attendees:
Adam Ley,
Wim Driessen,
Brian Turmelle,
Carol Pyron,
Craig Stephan,
Roland Latvala,
John Braden,
CJ Clark,
Carl Barnhart,
Francisco Russi

Meeting called to order at 8:35 am MST

Current Draft: P1149 1 Draft 20110404.pdf (-clean.pdf)

Agenda:
Continued review of PDL

Minutes:

General
1.A short discussion of Fig 11.1, whether or not it should be updated based on Ken's feedback to Carl this past week. The WG felt since this is an original figure and only introductory in nature it can be left as is.

2. Note from Carl that the wording of '4 or more signals' for BC cells restored to the text based on email discussions this past week.

Review of PDL

3.First we had lengthy discussion lead between CJ and Wim about the scope of PDL and whether or not it should be component level only, or extended to the board level:
- Wim has issues with the WG taking on PDL definition for board level test. Since BSDL and PDL will be supplied by component (chip) vendors he felt we should focus on component level examples and PDL definition. He would prefer that the group sticks to component level BSDL and PDL, and keep the board level discussions/work for the objective of another standard.
- CJ is of the position that we need to define enough board level PDL to allow access to component level test features once they are placed on a board.
- Carol added that component vendors will supply templates for certain cases such as IRESET or invoking MemoryBist,

- Franscisco brought up the question of 3D chips and chips with multiple TAPs. To date 1149.1 does not deal with this.
- CJ brought up that we want to be compatible with other standards, but leave multi-taps to those other Stds. We are in the board test business so we need to know how to assemble all this BSDL/PDL from chip to chip at the board/system level. Tests may need sequencing by a test engineer who does not soley rely on the board test software tool vendor to assemble all this per their own routines.
- Wim raised objections to developing a board standard and felt it was up to tool vendors to read BSDL and PDL for each chip and manage this one level above.
- CJ emphasized that tool vendors can still have their own proprietary languages, but we want to allow PDL to support hierarchy.
- Francisco raised the question of 1687 compatibility, and whether they face similar issues with board hierarchy? CJ answered by stating that 1687 is a chip level Std and they don't address the boundary register at all. We want to stay compatible with 1687and they can reuse our work here.
- This discussion tabled for now. CJ asked to note Wim's objections. So noted.

4. CJ then continued PDL discussions:
- Based on feedback from Adam it was decided that iWrite –IR should be sticky, and that subsequent writes to the same register do not need the –IR if the user intends to use the same instruction to access the register again.
- There was much discussion today whether the –IR should be on the iWrite/iRead or on the iApply. Based on today's discussions the WG group favors putting –IR in the iWrite and iRead to be explicit about which register it pertains to.
- There was discussion about also allowing the prior syntax like: iWrite.U1.instruction.CLAMP, where there is ambiguity, as in this case where the bypass register then become the active register.
- Discussions about whether and how a PDL sequence should be controlled. Many iWrites followed by iApply will be handled under the covers of the tools and the order may not be handled the same from tool to tool. CJ asked if we need to help the users avoid ambiguity and bad results? It was discussed that the component vendors should build in the correct sequences into their PDLs if it is important.
- CJ noted there are the same number of scans whether we allow a single iApply or execute it after every iWrite iRead. He was asking if we want to allow the single iApply at all?
- There was a short discussion about whether iWrite –IR SAMPLE should be an error or not? CJ thought it should be illegal, others thought it should not be an error, but is meaningless.
- CJ asked the group to think about how the DR scans are executed and said he would highlight our discussions to 1687 group.

Meeting adjourned: 10:00am MST

Action Items:
- WG members to continue homework review Clauses 9 &11 by next Tues.

Next Friday Meeting:
- Next week Friday April 22, 2011