September 17, 2010

Minutes of IEEE 1149.1 - Initialize Sub-Group Meeting

Attendees:

Carl Barnhart
Marty Bayer
John Braden
CJ Clark
Dave Dubberke
Roland Latvala
Adam Ley
Ken Parker
Francisco Russi
Brian Turmelle

Minutes:

Freescale (Roland and Marty) presented some concerns about Sample. leading to a wide ranging discussion.

- Want permission to not SAMPLE w/ Test Receiver cell (CJ: originally a dot-6 issue, now covered by new permissions for ROO to not SAMPLE.)
- Want the mission receiver boundary cell to be optional (CFB: this is now a conflict between dot-1 and dot-6; there is some desire to restore this cell to dot-6 because of the EXTEST problems with the Test Receiver; take up with dot-6 WG.)
- Sample on mission receiver is meaningless because of difference in clock speeds and because open receiver will toggle due to noise.
- CJ presented a slide with a Serial-In-Parallel-Out (SIPO) on the output of the mission receiver. This SIPO could be considered part of the analog receiving logic or not, but there are issues with both EXTEST and SAMPLE. Normally, a single bit of the output is monitored (assuming no INTEST support), with a bypass of the extra logic in EXTEST. Is this enough from a Black Box point of view?
- Should SAMPLE be allowed to be ignored on a per-pin bases, and if so under what circumstances?
- Adam: The meaning of SAMPLE data (usually NOT part of board test) has always been subject to interpretation (by someone familiar with the circuit.)
- Adam: Originally, SAMPLE was a simple way to take advantage of the existing connections already in place for EXTEST.
- CJ: would it be better for SAMPLE to capture the “Link Up” or equivalent signal from the SIPO instead of data? If so, how do we specify that?
- CJ: do we need to re-visit the “no logic” rule (11.4.1e)? Ken: No. Carl & CJ: we may need to for the “fault-cell” ROO, anyway.
- CJ: Some vendors currently support SAMPLE up to 10GHz others do not. Why?

There were no firm conclusions reached or changes to the Standard proposed, much less voted on, at this time. Roland sent out a separate list of options.

The meeting ended more or less on time.

Current Status:

Formalize Rules – In progress.

BSDL Constructs - – BNF coding in progress, semantic checks in progress.

Formalize PDL constructs – We need to start on this.

Actions:

- Carol to provide custom bidir IO example diagram.
- CJ to distribute his Board Test Workshop slides.

Work still to be done:

Formalize side-file language.
Incorporate INIT into 1149.1 Std.

Next meeting date:
Same time next Friday September 24th.