Date – 23/Sep/2011

Minutes of the IEEE-1149.1 Working Group Friday meeting

Attendees:
Carol Pyron
John Braden
Dave Dubberke
Roland Latvala
Dharma Konda
Peter Elias

Meeting called to order at 8:30 am MST

Current Draft: P1149 1 Draft 20110820.pdf (_clean.pdf)

Agenda/Overview:
Carol gave an overview of ITC and summarized 2012 Std remaining tasks
We also continued some discussion of ECID

Minutes:

ITC Overview from Carol:

CJ gave a 45 minute overview of 1149.1 2012
Ken gave a presentation on board 'labotomy' problem: clamp hold/release/icreset/safe&coo
Conference was well attended, last day 3 tracks (fewer sessions)
1149.8 in judges hands getting ready for ballot.

- (Like dot6, using ac pulses to test capacitive opens to connectors)
- Chips drive a net to from a scan part to a non-scan part

3D-IC presentation
LBIST (Intel presentation)
Mentor/Logic Vision LBIST has good technology too.
Common thread was voltage droop and power for voltage regions:

- Invidia talked about how computer architectures are changing.
- Multi-core, Performance per Watt
- For test we'll have to be aware of how much power we are adding to these chips. May need more partial scan, since overhead of scan flops is not acceptable anymore.
- Compilers made interface between sram and 1st flop scannable

Carl received an award for a paper he did 10 years ago

2012 Std, remaining tasks:

For our 2012 Std release we need to finish up:

- Power muxing
- Sample relaxation
- Boundary register segments
- PDL needs some standard subroutines
- P1687 (IJTAG) is targeting a Q1 2012 submission also
- Q1 Feb, or Q2 May submissions allowed, both will allow us to complete within 2012
- Discussion – Hard IP with BSR segment in it. How do they communicate this from IP to the chip
    - For hardend IP you can have a fixed TAP available

Dharma - Do 1149.1 and 1687 complete with each other?
Carol – Our PDLs need to match
John/Peter – P1687 builds on 1149.1 tap to access instruments inside a chip.
Carol – P1687 can access ICReset and Init_Data and run Serdes tests.

ECID Discussion:

Carol – ECID from PDL will need subroutines. ECID from TCK only (not a system clock)
Dave Currently a power up sequence is needed for reading fuses.
Carol – We are same today. Could possibly change to be TCK based.
Dave – What is the use model for ECID?
Carol – One use model is to prevent 'pirating' a board. ECIDs would be wrong for a copy cat board.
Dave – Also for field ECO changes
Carol – We also have a core version and processor version id registers.
Dave – The ECID will tell you about lot contamination.
Dave – They are driving for a simple way to determine device tracking.
Carol – They only have control of the TAP pins. P1687 assumes you have other pins available to them. ECID can be accessed that way. If we want to support ECID on partial assembled boards then TAP access should be required.
Carol – Tool vendors like TAP only access.
Dave – Security and privacy related questions are a concern
Carol – Yes. Today ecid's are private.
Dave – We are talking about ECID becoming public and accessible to all.
Carol – In mid 90's lawyers said do not like making ecid software accessible.
Peter – Yields and costs could be extracted and affect pricing.
Dave – That could be managed, but security is also an issue.
Carol – Today ecid reading is a complex process.
Dharma – We don't have access to all this information. For security do they mask the private stuff and only release the public stuff?
Carol – The spec says to invoke the instruction, and wait #tck's in RTI. If all 1 or all 0 then ECID did not get a valid state. If your ecid 256, you can tell public it is only 32 bits.
Dharma – After power up you can access through jtag, but first time only at POR.

Dave – What is the full scope of what we are trying to manage?
Carol – Bill Eklow gave some use cases.

- Chip manufacturers
- Board manufacturers
- System manufacturers

Dave – How is that used?
Carol – Spec limit tracking, and so on. The grand vision is that there will be a lot of data, data analysis up and down the food chain for end customers. It's in suppliers interests and a win, win from their point of view.
Dave – Managing their suppliers
Carol – Roland please document ECID using TAP only access in the minutes and mention concerns about security issues.
Peter – Run Bist uses system clocks so there is precedence for allowing system clock.
Peter – Also Sample was a terrible mistake.
Carol – They got too clever with Sample/Preload. They get it for free in Extest capture-dr. So they split it from Preload. Often had to errata Sample during Preload.

Meeting adjourned: 9:30am MST

Action Items:

- Carol to present SAMPLE relaxation topic in next meeting.

Next Friday Meeting:

- Next week Friday Sep 30, 2011