

**Date – 02/25/2011**

Minutes of the IEEE-1149.1 Working Group Friday meeting

**Attendees:**

Carl Barnhart,  
Dave Dubberke,  
Ken Parker,  
John Braden,  
Brian Turmelle,  
Carol Pyron,  
Roland Latvala,  
Francisco Russi,  
Mike Ricchetti  
Heiko Ehrenberg  
CJ Clark

**Agenda:**

- 1) Carl's review of clauses 3-6 of current draft (P1149.1 Draft 20110217 clean.pdf)

**Meeting called to order at 9:35 am MST**

**Minutes:**

Overview: Carl reviewed clauses 3-6 based on feedback from the group this past week.

Today's discussion points:

Clause 3: Definitions and Acronyms

- Carl made note of edits to the definitions of the following:
- 'chip' - device, component, or integrated circuit. The word 'chip' seemed to be to vague for a global audience. The use of 'component seemed to be the most widely accepted. Carl took note to modify the definition
- 'User Instruction' = design specific instruction
- 'User TDR' - design specific Test Data register
- 'No-Connect' - only applies to silicon chip pad with no package connection. Discussion from Carol and others whether this should be expanded to include package pins that are not connected at the board level for various reasons. Carl asked that we table this discussion and Carol took action item to continue this thread over email this week.
- 'BILBO' – removed
- 'Pin' - The definition as made more generic allowing for balls, pads, landings.
- 'Test Mode' – New definition added for test mode
- 'Cmos' – New definition added for cmos technology
  - 'BIST' – New definition for built in self test added (replaced BILBO).

#### Clause 4: The Test Access Port (TAP)

- Carl brought up question from Ted to discuss pullup vs pulldown requirement on TRST\* as shown in figure 4-5
- Dave Duberke discussed whether a pulldown should be internal to the chip to allow mission mode functional operation to be unaffected by a floating TRST\* pin.
- Carol brought up the point that a pull-up is required to allow the other 4 TAP signals to function correctly during test mode if TRST\* is floating.
- Ken answered question from Ted (via Carl) about relaying pins to TRST. Ken responded with respect to fig 4-5a, that board test engineers place special constraints on pins like TRST\* to not allow it to float. eg: connect it to a pull resistor to tester resource inside the ICT fixture.
- CJ pointed out that In circuit Test (ICT) has additional/challenges for test with its shared resources/relay matrixes that dedicated per pin testers do not face.
- Roland summarized the two opposing requirements about pull up vs pull down
  - Pull down on TRST\* would meet mission mode requirements to not interfere with mission operation if pin were floating.
  - Current Pull Up rule for TRST\* allows the other 4 TAP signals to operate correctly
  - Which has the higher priority?
- Carl tabled the discussion and will follow-up via email thread this week for closing discussions in next Tues meeting.

#### Clause 5: Test logic architecture

- No detailed discussion of clause 5

#### Clause 6: The test logic controllers

- Lengthy discussion of rule 6.2.2.1.d (ie: rule D. Local override of io clamp persistence rule)
- Currently the rule is written to only allow local control of io while the design-specific instruction is active.
- Carl brought up point that Ted wanted the local control to persist beyond the design-specific instruction that invokes local control of io, to allow other operations to then be done so that a test could subsequently be run to completion. This required a sequence of instructions and tdr operations in the bigger picture.
- Ken thinks any Std instruction should remove the local persistence override.
- CJ mentioned that EXTEST won't work anyway on advanced io unless INIT\_SETUP is run.
- Ken doesn't want to rerun INIT\_SETUP many, many times.
- Carol discussed how design-specific instructions whether Public or Private are difficult for designers to verify if there are not concrete rules for their usage. This means rule D is not easily verified by chip-designers.

- CJ mentioned we are already well beyond simple BSDL verification given PDL involvement.
- Carol reiterated that designers cannot validate all possible combinations of loosely defined instruction and rules.
- Ken refined the rule-D to the effect that local control of io can supersede io persistence control for a 'group or family of related design-specific instructions'. As soon as some other Std instruction is loaded io-persistence control is restored to that established by the test persistence controller. This allows the design-specific test to perform its operations using an instructions in that family and local control will be preserved for them until a Std instruction is loaded such as Bypass, Exttest, Sample, etc.
- The group was in general agreement with this.
- Carol brought up a question on rule 4.1.1.c (dedicated TAP signals)
  - The discussion was that when not in 1149.1 compliant mode those pins are commonly reused for other test purposes, and that the rule should be rewritten to allow this.
  - The group agreed and Carl added text to rule 4.1.1.c to allow this. The addition of the phrase 'when in 1149.1 compliant mode' was added to the rule.
- Francisco asked if the figures in the draft were final or not? For example IC\_Reset discussions lead by Ted and CJ, was that finalized yet?
- Carl stated that figures can still be changed and that discussion of IC\_Reset had not yet been finalized but will be discussed in later section of the draft.
- CJ mentioned that Ted had conceded this topic unless others were for changes to current draft.

**Meeting adjourned: 10:45am MST**

**Action Items:**

- Carl to start email thread for further TRST\* pullup/pulldown discussions
- Carol to start email thread for further No-Connect pin discussions

**Next Working Group Meeting:**

- Next meeting Feb 18, 2011