Date – 9/16/2013
Attendees: (14) CJ Clark, Bill Tuthill, Brian Turmelle, Frans de Jong, Gurgen Harutyunyan, Josh Ferry, Kevin Gorman, Mike Ricchetti, Philippe Lebourg, Roger J. Sowada, Marc Hutner, Steve Sunter, Dwayne Burek, Tapan J Chakroborty,

Missing: Dave Armstrong, Kent Ng, Tom Waayers, Saman Adham, Bill Huott, Craig Stephan, Gobi, Teresa McLaurin, Dharma Konda, Ismed Hartanto

Agenda:

1) Update on PAR
2) Q&A discussion on slides
    a. Two inputs from ITC on methodology
        i. 8b/10b encoding not needed for short chip test
            1. (but perhaps still needed for system test)
        ii. Interleave at bit level to manage clock domains better

Meeting Called to order at 11:05 am EST

Minutes:

Update on Par
Sponsorship for 1149.10 was called for vote and vote had passed.
CJ received email from the sponsor so we can move forward.
Still not a working group per se until IEEE standards associations' board approves par.
CJ is not concerned about this and feels they will vote to grant the par. This will happen soon.
Can't get Website until the IEEE approval. Once that is done we will have a web site to put documents and

Q&A discussion
With a discussion CJ had with Steve Sunter, Steve had pointed out that we may not need 8b/10b encoding for the chip test.
Steve : Mentions that when they test with SERDES they control the patterns and make sure that they are compliant with 8b/10b even if it is not a 8b/10b packet
CJ – ok. Take as a data point. Using 8b/10b encoding (and 64/66) won't add too much to the logic.
CJ - Carol Pyron's input was that on the interleave we interleave by bit.
CJ – were currently going to be interleaving by wrapper/serial port. But she thought the shifting and decoding there would be problematic. Potential for some overhead doing by the bit.
Marc – would be difficult when isolating a pattern.
CJ – wasn't that it was always interleaving. Interleaving based on demand. So the patterns are interleaved on what is required. Wouldn't be forced to interleave all the scan chains.
CJ – carol's concept was wrapper serial ports per bit.

Marc – Likes editing byte wise per object and not interleaving.
CJ – agrees. Comes down to how you are going to do your decode on the parallel interface.

Steve - Seems very specific to 1500 wrappers opposed to a generic test interface. Has any consideration been given to sending an address like a TAP to talk to a specific data register?
CJ – in 1149.1 there is a convergence with 1500. It is addressable with the WrapperSerial port select. WSP Select can direct the scan.
For high volume testing we would have to shift to all the chains at the same time.
If there is nothing to interleave you are talking to one scan chain. To get the throughput you would be interleaving quite a bit.
CJ – input and output is in parallel format. Parallel interface going into the packet encoder. Overall goal in 1500 format looks like it normal does. ATPG would be generating STYLE like patterns.
How do we test the logic in the test interface? Some sort of BIST logic around the interface. Like the Scan Chain Integrity used to test the scan chains
CJ – there will be an ideal packet that tells the tester to hold off. Similar to XON/XOFF

Tapan – what is the goal of the standard? To test SERDES interfaces on chips?
CJ – 1149.10's goal is a high speed test access port.. Not for testing SERDES. For improving the bandwidth to and from the chip. Also to minimize the contact points.
This will also address power on the chip where it would allow for slower clocking but achieving the same test time.
Plus Reuse the SERDES interface already on the chip.

CJ – data would come in on the parallel side of a SERDES. Not specify how the SERDES logic works in the standard.. Don't want to standardize on one protocol. Define packet decoder and distribution.

CJ – some setup will need to be done using new features of 1149.1-2013. Can use PDL to setup the SERDES through INIT / SETUP feature in new version of 1149.1
Steve – Adaptive test mentioned on slide – can't see anything on the slide that is related to adaptive test
CJ – Adaptive test has a card and system level component to it.
Steve – able to get access to the chip in card and system level. Nothing to do with adaptive test.
CJ – test reuse is critical to adaptive test. This standard needs to work with the registers in the tap and reapplying it over the card and system level.
One of the goals is a low touch down and reuse the test
Steve – None of the capabilities of adaptive test focus on the scan test.
CJ – your point is that adaptive test is specific to parameterization.
Steve – if adaptive test is a motivation for .10 than you would need more support that shows that adaptive test needs .10
Also there is mention of not using memory on chip. There is memory. All the shift registers are memory.

CJ – from that prospective. You could shift data. Memory meant in the traditional sense of memory and memory controllers. The packet is decoded and shifted in to the scan chain on the fly.
Steve . The argument for interleaving isn't there. You can shift into the shift registers
CJ – no memory for packets in this case means shifting into buffers. The scan chain can be looked as memory yes. Data is streaming into the scan chain and not being buffered into memory.

CJ – wants to put time into decode and distribution matrix. Does not want to debate "adaptive test" as a benefit of 1149.10
Standard isn't about adaptive test or no adaptive test. Sees it as a benefit.
Steve- important to have a clear view of the benefits
CJ – we don't have to all agree with all the benefits. Lower clocking rate, high speed data, and lower touch down. are the main issues that we are looking at in our scope.
Steve – feels we all need to be on the same page for what are the major benefits. Wants to see what everybody else sees as a benefit. This will help with the decisions on what goes into the standard.
CJ - High bandwidth with low contact. This is what we have decided on prior.
Steve - Interested in understanding the benefits.
Mike R – do you see a benefit in low pin count and high speed data
Steve – sees that is a big benefit.
CJ – benefit overall is high bandwidth and low touch down with potential reusability.
Steve – Sees high bandwidth is a capability and not a benefit.

Motion to adjourn – Steve
Frans Seconds

Meeting adjourned: 12:09EST.

Action Items

Next Meeting:
September 23th, 2013 11:00am

NOTES:

1149.10 working group website - http://grouper.ieee.org/groups/1149/10/

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