Date – 10/07/2013
Attendees: CJ Clark, Adam Ley, Bill Tuthill, Brian Turmelle, Bob Gottlieb, Craig Stephan, Dwayne Burek, , Frans de Jong, Gobinathan Athimolom, Josh Ferry, Kevin Gorman, Ismed Hartanto, Roger J. Sowada, Steve Sunter, Teresa McLaurin,

Missing: Dave Armstrong, Kent Ng, Tom Waayers, Bill Huott,
Dharma Konda, Gurgen Harutyunyan, Marc Hutner, Mike Ricchetti, Philippe Lebourg, Tapan J Chakroborty, Saman Adham,

Agenda:

Continue technical discussion around figure in the PDF titled "distribution-network" This was emailed to the group

Meeting Called to order at 11:08 am EDT

Minutes:
This week RevCom will look at our Application to make our group an official IEEE Working Group

Craig Stephan is going to provide some Verilog in the next couple of weeks to give more insight into the

CJ reviewed the diagram sent out

CJ defines the Acronym CSUK – Capture Shift Update Clock
Tap is generating the signals – Capture Shift and Update TCK and instruction decode
Instruction will select test data register in 1149.1 mode
In 1149.10 mode the packets will decode and select the registers.

Added Reset'* and Mode' signals. Mode signal will have be controlled by the packet decoder too.
Mode and RESET* coming from the TAP now
Mode – 1149.1 2013 you can have mode or CLAMP_HOLD mode. This is a gated mode signal

1149.10 mode set by INIT setting. Could also have an instruction but would have to be sticky like CLAMP_HOLD so that it doesn't go away when you load another instruction.

Dwayne – wasn't thinking this was a replacement TDI/TDO data accessing all the registers. Do we think that is necessary? There are other standards like 1149.7 that have complicated things and not much adoption of that. This is more complicated. Would have to figure out arbitration between TAP and SERDES interface.

CJ – it's up to the group, but many of the test data register having access through the high speed interface is important. INIT_Data registers are quite large and a lot of data there that needs to be delivered. Would want to maintain that access so that you have a choice to come through the high speed interface or the TAP.
Dwayne – wasn't thinking there was a bandwidth problem there. Even for an IO test there is waiting. The shift time wasn't that much of a concern. The boundary register might be the one with the bandwidth needs. Device ID/ECID/Bypass are not bandwidth limited. Also we use a CPU interface to get to the 1149.1 register. This will create another interface now to deal with.
CJ – that could help you. If you are already muxing the scan chain with the CPU you should be able to add another interface.
Dwayne – we can get the CPU interface more or less going through the 1149.1 interface. Here it would interface with the 1149.10 interface. And would have to be building another interface into the TAP. This may be less modular.
CJ – There might be a some of the group who want to have a dedicated SERDES that comes up in 1149.10 mode with no 1149.1 access. We could enable that in the standard by allowing if it comes up in 1149.10. we don't preclude the 1149.1 interface to be default.
Dwayne – Don't see the need for the top registers (BYPASS/DEVICEID/ECID) to go through the HSIO interface. Will be more complicated. If there is a SERDES default that doesn't touch the tap pins, there are some arbitration issues going on.
CJ – thinking that tradition Reset would bring you back
Dwayne – The 1149.10 interface would come up as master? And 1149.1 would have to reset it and pull it back. Original vision was that 1149.1 would be master. 1149.10 would be a slave interface and just used to open up bandwidth to serial chain.
CJ – Having the dual access is useful but if there is a design challenge we should not mandate it.
Dwayne- Concurrent access of 1149.1 and 1149.10.
Steve – You would not have SERDES going to multiple chips. So it might not be practical to say coming in through SERDES and having data go to one chip and other data going to another chip.. SERDES only will go to one chip.
Dwayne – you would need a broad cast mode.
Steve – Could have SERDES going to one chip in a stacked die, but communication to other chips in that stack could be feasible.
CJ – test data registers could have voltage or temperature monitors. Someone who doesn't have access to the SERDES could still get access to the BIST registers through the TAP. Should at least enable or allow it to happen. SERDES is point to point, but can't see a reason that the output of the PISO isn't connected to another DIE.
At the board level if you wanted to daisy chain this together, that can be enabled without too much design work. Packets should be able to access all of the test data registers. Should just be muxing and gating logic.
Steve – to summarize Dwayne was saying you could use the regular tap controller to deliver the data to the smaller register. And allow regular data through the SERDES. In addition to address multiple chips. Key advantage would to have everything come through SERDES. And that simplifies writing the test as opposed to the logic.

CJ – one less thing to debug if you get your test to work through the TAP it should work through the SERDES interface. Could be useful in debugging the SERDES interface too.
Steve – Remembers that 5-10 years ago JTAG Tech received a patent where they deliver JTAG interface though a different interface. That is kind of what this is looking like. We should investigate that patent for an overlap.
CJ – Intellitech also has some prior art showing JTAG data over Ethernet which would be similar.
Dwayne – wouldn't think we would daisy chain the 40 bits. Would want to only daisy chain the serial (RX/TX) data.
CJ – Agrees, we would daisy chain the transmit and receive signals and not the 40 Bits. Diagram didn't really show that. Just showing the implementation of the SERDES is outside what we are trying to define. Not asking anyone to redesign their SERDES interface.
Dwayne – Could get complicated with addressing and could have broadcast mechanisms in that addressing.
CJ – we could have a broadcast.
CJ- Reason that you would like to have the ECID to support the ability to uniquely communicate with one of the implementation of 1149.10. Would want to wake up a specific chip with other chips ignoring data.
Bob – Regarding interleaving data types. On the way back out, how do we put the packet data header back on? Also how do we ensure packet ordering?
CJ – Packets are tagged such that we know the target test data register or WSP. Packet has fields to describe WSP Select (Scan Chain select) to show where data is going or coming from. Know the ordering of how the scan chains will look by these fields.
Bob – not only pushing into the chain but popping back off.
CJ – when you have the WSP Select the packet encoders doesn't' have to come up with a new encoding.
CJ – what isn't shown here is a packet type. Should be encoded with a different packet type to describe a packet coming back.
Frans – What is the relation between System Clock and the SERDES? Not present in this diagram.
CJ – when you go from 1149.1 to 1149.10 mode using the enable bit. Sets the mux to switch between the CSUK to CSUK serial in/out from PISO.
Frans – so that should be cycle accurate.
CJ – It is based on relation between the system clock and the data width.
CJ – timing limits on the right hand side.
Steve – system clock could be 100 MHz and it is not always equal to the serial data rate divided by the width but could be more.
CJ – clock is not based on 40 bit wide?
Steve – not always equal to serial rate / width.
Frans – We should leave out "SERDES /n" and keep it to system clock and we will see what happens.
CJ – in FPGA world we are used to see the clock rate that goes to the fabric
Steve – It is not always so tidy.
CJ – how is it not that?

Dwayne – whatever our 40 bit parallel word is. We would have to derate that to if we are going to shift the boundary register. We would have to shift that quite a bit.
CJ – would have to packets to send to the ATE to slow it down
Dwayne – 40 bit coming at 640 MHz but can only shift it at 10 MHz Would have a lot of IDLE packets
Steve – the big thing is to say that system clock and TCK are not synchronous.
Dwayne – there will be 1 packet and 100 idle packets.
CJ – depending on the operation I would agree.
Steve – if it is going to be a100/1 ration you would do everything through the TAP. Only aimed at where you have a bandwidth issue.
Dwayne – right. That was the point about the upper registers.
Steve – to have those other registers accessible through the SERDES would allow you to have all the tests accessible through the SERDES. Might be overkill but would have just one interface.

Motion to adjourn Fans
Seconded Steve

Meeting adjourned: 12:04EDT.

Action Items

Next Meeting:
October 14th, 2013 11:00am

NOTES:

1149.10 working group website - http://grouper.ieee.org/groups/1149/10/

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