Date – 10/14/2013
Attendees: CJ Clark, Adam Ley, Bill Tuthill, Bob Gottlieb, Brian Turmelle, Craig Stephan, Dharma Konda, Dwayne Burek, , Frans de Jong, Gobinathan Athimolom, Gurgen Harutyunyan, Ismed Hartanto, Josh Ferry, Philippe Lebourg, Teresa McLaurin,

Missing: Dave Armstrong, Kent Ng, Tom Waayers, Bill Huott, Marc Hutner, Mike Ricchetti, Tapan J Chakroborty, Saman Adham, Kevin Gorman, Roger J. Sowada, Steve Sunter,

Agenda:

11:00 PAR still pending. IEEE-SA meeting held on Friday.
11:05 WG P&P brief Q&A. Please read for next week, send feedback/proposed changes via reflector.
11:15 Continued architecture discussions.

Meeting Called to order at 11:12 am EDT

Minutes:
Par is still outstanding. CJ will let the group know if there is any updates.
Working group Policy and Procedures. They were sent out in email. CJ made some changes to the general policies. Next week we will review the changes as a group and vote on changes. Send suggestions to email reflector or discuss on Next Monday.

Architecture discussions.
Review of diagram from last week's meeting that was sent out in email
Why would we want to include small registers in the 1149.10 interface? Some registers will need to be interfaced by the HSIO. i.e.

Device ID and ECID registers contain important information for this interface.
Will help identify the uniqueness of the device.

Dwayne – would like to see how the architecture will pans out. Shift frequency might be bound. Shift Frequency can be derived from the system clock so each register could have its own frequency range.
CJ – Definitely need an on clock mechanism which isn't shown on the diagram. Need a mechanism through the 1149.10 interface to adjust the frequency. But it will be a smaller frequency that is required.
Dwayne- packet decode/encode. The 40 bits that are coming in are raw serial data might need some kind of synchronizing sequence. How does it know when to start decoding packets. Not clear how it will interpret these 40 bit words coming into the decoder.
CJ – part of the solution is the packet format that was shown previously.

Typically the line would have an IDLE character. The start of the packet will tell the interface that we have gone from the IDLE state to data coming in.

Dwayne. That is where I'm not sure where the 40 bit words coming into play. Is the SERDES doing the idle management and just presenting data? Was treating this format as the raw 40 bit data. So the start sequence some kind of pattern, bit, or word, or TDB

CJ – The character that is being presented is the IDLE character until you get to the start of the packet.
Dwayne – the payload could be arbitrary data. Would the packet decoder get confused if it randomly saw the idle character?
CJ – the IDLE character is an invalid 10 bit encoding so the receiver is able to detect the change of the data.
Dwayne – thought we would disable all the coding.
CJ – still need the 8b/10b encoding.
Frans – through the standard tap mechanism we put in the instruction for this high speed interface. You are in High Speed mode after update and until reset
CJ – thinks test logic reset brings it back to 1149.1 mode

The p1149.10 interface is off by default at power up and need a mechanism to turn it on. Could have a hard wired 1149.10 interface. Wouldn't require the tap to enable/disable it if there is a hard wired p1149.10 interface
Frans – would like a version number on the diagram for ease of discussion.
CJ – agrees and updates diagram with a date stamp
CJ – Inbound packets

Scan Interleave packet
Targeting Packet- select 1 of n or any P1149.10 IC to process packets or ignore
ScanR - Scan Response - ignored, forwarded to output packet.

Outbound Packets

ScanR – interleaved Scan Packet Response
TargetR – Target Packet Response
XOFF - Tell ATE to hold off on sending more packets
XON – tell ATE to resume
IDLE <n> - Tell ATE to insert IDEL Patterns. (May need not sure)

Another approach would be to add into the information of the chip a description of the TDRs and required clock speed.
Philippe – what is a typical target for this type of structure? What is a reasonable application field in terms of scan flip flop counts?
CJ – target would be IC that has a high speed SERDES on them and have a need for a significant test data
Philippe = what is significant?
CJ – 50 chains with 50 scan in and outs. The ATE will only touch down to the high speed IO and reduce the touch down. Could clock at a lower rate as well.
Philippe – compressors on the market to reduce the number of scans.
CJ – those can be continued to be used. They don't from free. And there is still a need to reduce the outside contacts. In the FPGA space, there are 10's of minutes to configure devices today. Over the next 5 years FPGAs will keep getting bigger. JTAG as a programming interface is getting limited and a high speed interface will help speed up programing.

Back to Packets
CJ - In the packet encoding, the ability to be able to adjust the clock and the scan chain and have a description of the chip.

Don't want to over the data because of need of memory to store data

Bob – We are leaving the burden to do clock control to the ATE. Not on the logic circuit
CJ – yes. Clock control would be something accessible to change the clock rate. It would be part of the test data for the chip. External the ATE will need to have enough information to tell the ATE to insert the IDLE packets. That seems external to the chip.
Theresa – are you not considering WPP (wrapper parallel port) from getting data from the HSIO
CJ – yes. Maybe a terminology problem. Maybe shouldn't be called WSP but they are parallel scan ins and parallel scan outs.
Theresa – looks like it is going to WIRs and not WPP.
CJ- We are still shifting data?
Theresa- so we are shifting several data pins to the core.
CJ – will change the diagram to reflect the idea better.
CJ – trying to avoid something adhock
Philippe- was there a addressed a need for sequential ordering of the blocks? Taken into account that the blocks that are supporting this interface being tested ahead of time. Need to test blocks without using their interface.
CJ – yes this has been brought up. We don't specify in the standard how to do that testing and what sequence. Our mission is to describe the encoder/decoder and distribution matrix. Similar to 1149.1. need to get to the tap controller to use it.
CJ – number of tests that can be done. Don't think it is in our scope to nail down the testing of the HSIO as everybody's will be different.
No one in the group has a comment about this concern.
CJ – you will have to test the structures that are there.
CJ – perhaps an annex can be added to indicate that these blocks should be tested.

Frans – makes motion to adjourn.
Second – Philippe

Meeting adjourned: 12:02EDT.

Action Items

Next Meeting:
October 21st, 2013 11:00am

NOTES:

1149.10 working group website - http://grouper.ieee.org/groups/1149/10/

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