

**Date – 12/02/2013**

**Attendees:** CJ Clark, Adam Ley, Bill Tuthill, Brian Turmelle, Bob Gottlieb, Carol Pyron, Craig Stephan, Dave\_Armstrong, Dharma Konda, Dwayne Burek, Frans de Jong, Gobinathan Athimolom, Gurgen Harutyunyan, Jon Colburn, Josh Ferry, Kevin Gorman, Marc Hutner, Mike Ricchetti, Steve Sunter, Tapan J Chakraborty, Teresa McLaurin,

**Absent with Excuse:**

**Not Present for  $\frac{3}{4}$  of meeting:**

**Missing:** Kent Ng, Tom Waayers, Bill Huott, Saman Adham, Jim Wilson, Ismed Hartanto, Zahi Abuhanmdeh, Philippe Lebourg,

**Agenda:**

- 1) Patent Slides
- 2) Affiliation record. We said we would record once, each participant's affiliation in lieu of a weekly announcement.
- 3) Further discussion on slides
- 4) 12/9 meeting cancelled. I am flying back from IEEE awards dinner on Monday morning (thank you again to many of you) and couldn't get a time slot outside of our meeting time.
- 5) New Business

**Meeting Called to order at 11:03 am EST**

**Minutes:**

Review Patent Slide – Slide Presented to the Group.

Solicited input from anybody who is aware of patents that might read on our standard.

No Response

**Affiliation Record:**

CJ sent out link for FAQ regarding Disclosures of Affiliation

We will record affiliations once and any changes will be disclosed and added to the minutes.

Adam Ley:	Asset Intertech,inc
Bill Tuthill:	Raytheon
Brian Turmell:	Intellitech
Bob Gottlieb:	Intel
CJ Clark:	Intellitech
Craig Stephan:	Intellitech
Carol Pyron:	Freescale
Dave Armstrong:	Avantest
Dharma Konda:	Did Not Respond
Frans De Jong:	NXP Semiconductor

## IEEE 1149.10 High Speed JTAG Working Group Minutes

Gobinathan Athimolom:	Did not respond
Gurgen Harutunyan:	Did not respond
Josh Ferry:	Teradyne
Jon Colburn:	Nvidia
Kevin Gorman:	IBM
Mike Ricchetti:	AMD
Marc Hunter:	Teradyne
Steve Sunter:	Mentor Graphics
Teresa McLaurin:	ARM

### Discussion of Slides.

No updated slides were sent out the past week.

#### Slide 17

Don't think we can get rid of encoding due to need for changing 1's and 0's and have robust data to recover clock.

Number of scan chains is equal to data width of the PHY.

At 25GHz rate you end up with very fast clock. This could be problematic. May need to divide down but would need a mux and descriptor to know where the scan chain data is to go.

Without Packet format you lose ability to daisy chain components together.

Packet interleave size could be added. 1/4/8 bits

Bob – Comment about matching number of chains is to not waste bandwidth? No functional problem?

CJ – correct.

Dwayne – maybe we can review some of our pattern data to validate the clock recovery.

CJ – maybe the data going into a decompressor might be random enough but you couldn't guarantee it.

CJ – as the SERDES technologies improve we could architect something that as broken. We should go along with the encoding.

Dwayne – still not sure how we would do the alignment.

Bob – one thing we would do for alignment we would take the 40 bits and have 32/36 as data and have 4 as address. And decode that way.

Dwayne – the alignment of the 40 bits is random. Would need a barrel shifter.

CJ – alignment is done with comma character (K)

Bob –

Steve – bit alignment should clean up the data

Marc- buffering data makes more sense and can limit the scope some.

CJ –

Frans – should we put a requirement of the quality of signals?

CJ – we should standardize of some of the quality. Like a CRC on the data packet.

CJ – shown 3 methods to test reliability. And the CRC32 would guarantee the integrity of the packet.

Frans – do we define the quality?

CJ – yes we would write down the 3 methods in the standard.

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Frans – do we want to write down a certain set of requirements that guarantee a test speed.

CJ – up to group but we don't want to specify the quality of the signal going into the chip and coming out.. that is a PHY and SERDES quality issue that is outside the scope of the standard.

Steve – no specification going in and out of a TAP.

CJ – as long as we provide a mechanism to validate the quality that should be sufficient.

Steve – because this is using a more complex interface than a TAP we should have more a method to check data and the 3 that CJ mentioned are good.

Steve – modem testing. Offer different points of loopback.

Bob – if we left it this way everything would have to sit off the generated clock.

Don't think that works.

CJ – yes.. Would have to shift off that clock.

Bob – couldn't have a clock crossover. You would have to distribute the clock everywhere.

Carol – would be an issue.

CJ – do we feel we need a packet protocol? Is raw data have limitations.

Bob- either way we are sending a packet?

CJ – no .. if data is managed in the PHY it is 40 bits pure data (shift data)

Bob – have to have the 8b/10b. How do you handle it without packets?

CJ – maybe Frames is a better word.

Dwayne – concerned about packet processor and buffering.

Frans – would this require a layered approach? Packetize to setup test mode

Dwayne – use TAP to initialize mode. And then pump data in.

Would be a similar approach. With the data coming in SERDES interface.

Steve – Instead of the SERDES interface, could also think of a DDR interface that is 1-n bit wide. Still have the same block to get in and out of chip. Just becomes a simpler interface. Might be simpler instead of SERDES.

CJ – potentially that could be that. Little concerned on the ATE side. Benefit of standardizing on the SERDES might be easier of the ATE.

Carol – SERDES in electronics are expensive and not on all testers.

Dwayne - Protocol aware packet buffer is small and might be for exercising interface and not for pumping data through

CJ – Next Week's meeting is canceled due to the chair's availability. (12/9)

Motion to adjourn – Frans

Seconded – Steve

**Meeting adjourned: 12:00 EST**

**Next Meeting:**

December 16<sup>th</sup>, 2013 11:00am

*Motion Summary*

*0 motions*

*Action Items*

~~*Bill Tuthill—10-21-2013—Add minutes and Attendance spreadsheet to the website.  
CJ—11-11-2013—Reach out to ATE industry and Probe Industry to get update on future of ATE equipment to see which data speeds and protocols they are heading towards.*~~

NOTES:

1149.10 working group website - <http://grouper.ieee.org/groups/1149/10/>

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