Date – 02/24/2014
Attendees: CJ Clark, Adam Ley, Bill Tuthill, Brian Turmelle, Craig Stephan, Dharma Konda, Dwayne Burek, Frans de Jong, Gobinathan Athimolom, Ismed Hartanto, Jon Colburn, Josh Ferry, Marc Hutner, Mike Ricchetti, Roger Sowada, Steve Sunter, , Tapan J Chakraborty, Teresa McLaurin,

Absent with Excuse : Philippe Lebourg, Bob Gottlieb,
Not Present for ¾ of meeting:

Missing: Bill Huott, Carol Pyron, Jim Wilson, Kent Ng, Kevin Gorman, Saman Adham, Tom Waayers, Heiko Ehrenburg, Dave Armstrong, Gurgen Harutyunyan, Zahi Abuhanmdeh,

Agenda:

1) Patent Slides
2) Dwayne's presentation
3) Review of draft 4
    a. WG input/discussion/creation of draft
4) New Business

Meeting Called to order at 11:06 am EST

Minutes:
Review Patent Slide – Slide Presented to the Group.
Solicited input from anybody who is aware of patents that might read on our standard.
No Response

Dwayne's Presentation: Slides will be posted in on Website.
Slide 3
ATPG application
20 digital pins + 1149.1 TAP used for clock, shift, and update
Concurrent block testing is supported.
Patterns must be shifted aligned (can pad patterns to align)

Slide 4
Existing Architecture
20:1 compression
Digital inputs are broadcast to core channel
Chip TAP provides control signals
Core channel outputs are routed out through digital pads.
Slide 5
Pattern Application
Tool Translates block level patterns to chip level
Channel mapping included in description file
Checks are performed to see that channel resources are available.

Slide 6
- Waveforms
  - TAP Controls ATPG compression Protocol
  - TCK provides shift clock
  - On Chip Controller provides at speed clock
  - TMS drives through protocol

Slide 7
- Mapping to 1149.10
  - Conceptually similar to earlier discussion
  - PISO/SIPO path

Slide 8
- Mapping to 1149.01
  - Channel inputs are sources from section of 40 bit word
  - 40 Bit SERDES word is fed from channel outputs
  - 3 Control sources from 40 bit SERDES words
    - Used to come from tap and now from 40 bit word

Slide 9
- Mapping to 1149.10
  - 40 bit word description
    - Control embedded
    - Channel data embedded
  - Output would need padding bits

Slide 10
- Data word Alignment
  - Break down 40 bit word into a useful word. 32 bit? Rest for overhead clock recovery padding?
  - Can gang multiple words if need more than 32

CJ – is there error checking? Current proposal has 32 bit CRC

Dwayne – wouldn't think so. More based on pseudo random test and check for bit errors.

CJ – wouldn't be able to differential result data incorrect vs. output data being incorrect.

Dwayne – could have retest? That might deal with sporadic bit errors in channel if you have a secure channel or a way of defining channel errors vs. chip failures.

Slide 11 (summary)
- Rarely use 40 channels. Usually ~32
  - Clock recovery encoding could be done within unused spare bits in40 bit word.
  - Disparity could be encoded as well?
- Often use asymmetric – more inputs and less outputs.
  - 16 in and 4 out allows 4 identical cores to be tested concurrently
- If you need more data you could gang multiple 40 bit words
- Mimics STIL patterns

Slides sent to working group and will be posted to website

Discussion will be added to agenda next week to allow members to take some time to review material. (No one had any questions today regarding the presentation. Discussion can also be on reflector if anyone has questions)

Review of draft 4

Tapan – can guys from the tester industry comment?

CJ – Marc Hunter, Josh Ferry, any comments?

Tapan – how does this fit in on the roadmap of the tester?

CJ – Current understanding is that some testers can and some can't support this type of testing.

Marc – Vector conversion path too, What Dwayne was discussion, using conversion scripts to map to hardware. ATE have serial instruments that can be used. Not sure about the 25GB/s space but the 10-12 GB/s space is covered

CJ – should I continue with what you have? Would like to know what the groups thoughts on the content are.

Frans- There is quite a few pages. We should probably go chapter by chapter. Something focused like that.

CJ – not any single chapter is complete.

Frans – We could still get together and identify what is missing or accept what is there for each chapter.

CJ – concern is that it isn't restrictive enough. Not capturing the requirements that guarantee success.

Section 7.2

Allows for common clock

Encoding changed so there is a "NONE" option

Frans – Standardization isn't always leaving in all options.

CJ - agreed. Standard shouldn't be ambiguous. This standard is more targeted towards the packets themselves (packet encoder/decoder).

Section 4 HSTAP

Rules

1149.1 TAP is not needed if 1149.10 HSTAP is enabled at power-up.

Josh – Could we institute a compliance enable instead of being brought up in an enabled state

CJ – We can do whatever we have the resolve to do. 1149.1 TAP is used as the compliance enable.

Josh – if you have a simple single pin or vector on multiple pins, it might add more flexibility for IC designers.

CJ – as long as we have a way of describing it. Concerned if they were the same pins as the compliance enables as 1149.1

No one sees any problems doing it this way (no responses)

Frans – add it as a capability. When we discuss this chapter, than we can make motions on the content.

BSDL Definitions.

Scan Port Identification section. Reuse BSDL as long as this portion is not required. A tool wanting to support 1149.10 would have to know by conformance attribute or 1149.10 package file that you were compiling a BSDL that is for 1149.10. It is an error now if you don't have a <Scan Port Identification> (TAP) if you don't have a TAP than the ScanPort Idenification section isn't required to be documented. Only thing in BSDL that forces the use of the TAP.

Frans - test register chain in the device, can be done with ICL and PDL?

CJ – if you wanted to describe the scan chains with ICL you could do that.

These attributes are packet maps. Does not have a good way to describe them in ICL

Frans – more of a conceptual question. Do you think we should we look at it?

CJ – open to the idea, just don't have the bandwidth to do both BSDL and ICL definitions.

These attributes need a real number to describe things like voltages.

Motion to Adjourn: Josh
Seconded: Frans

Meeting adjourned: 12:10 EST

Next Meeting:
March 3rd, 2014 11:00am

Motion Summary
0 motions made

Action Items
~~Bill Tuthill – 10-21-2013 -Add minutes and Attendance spreadsheet to the website.~~
~~CJ 11-11-2013 Reach out to ATE industry and Probe Industry to get update on future of ATE equipment to see which data speeds and protocols they are heading towards.~~
Philippe – Look into alternative method to create control information (pause, start, terminate, etc.) rather than using K characters in packet.
Bob – create a case study to show use of Attributes

Frans – will start some block diagrams of a simple use case to help illustrate the current architecture
Dwayne – present to the group his ideas for a simplified scheme – Direct Interface.

NOTES:

1149.10 working group website - http://grouper.ieee.org/groups/1149/10/

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