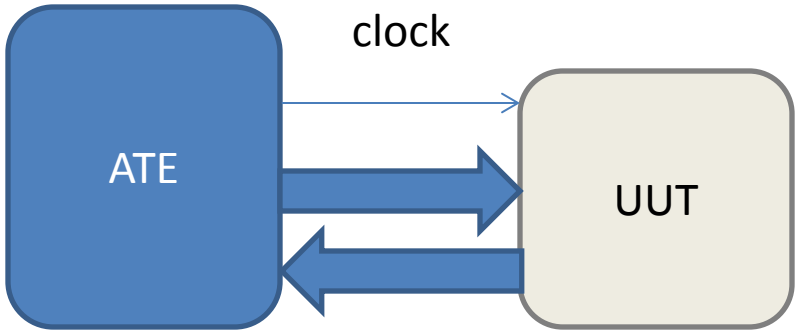
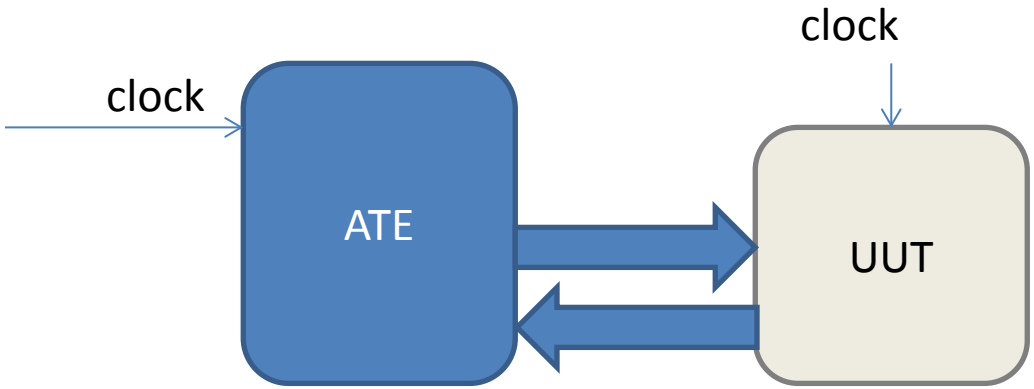
Scalability of P1149.10 versus Common Clock Test Interfaces

CJ Clark, Intellitech

Common Clock - Interface is synchronous to clock driven by ATE





Embedded Clock - Clock is embedded in the interface

- While ATE may drive the system clock needed by UUT, Clock for UUT could come from other source.

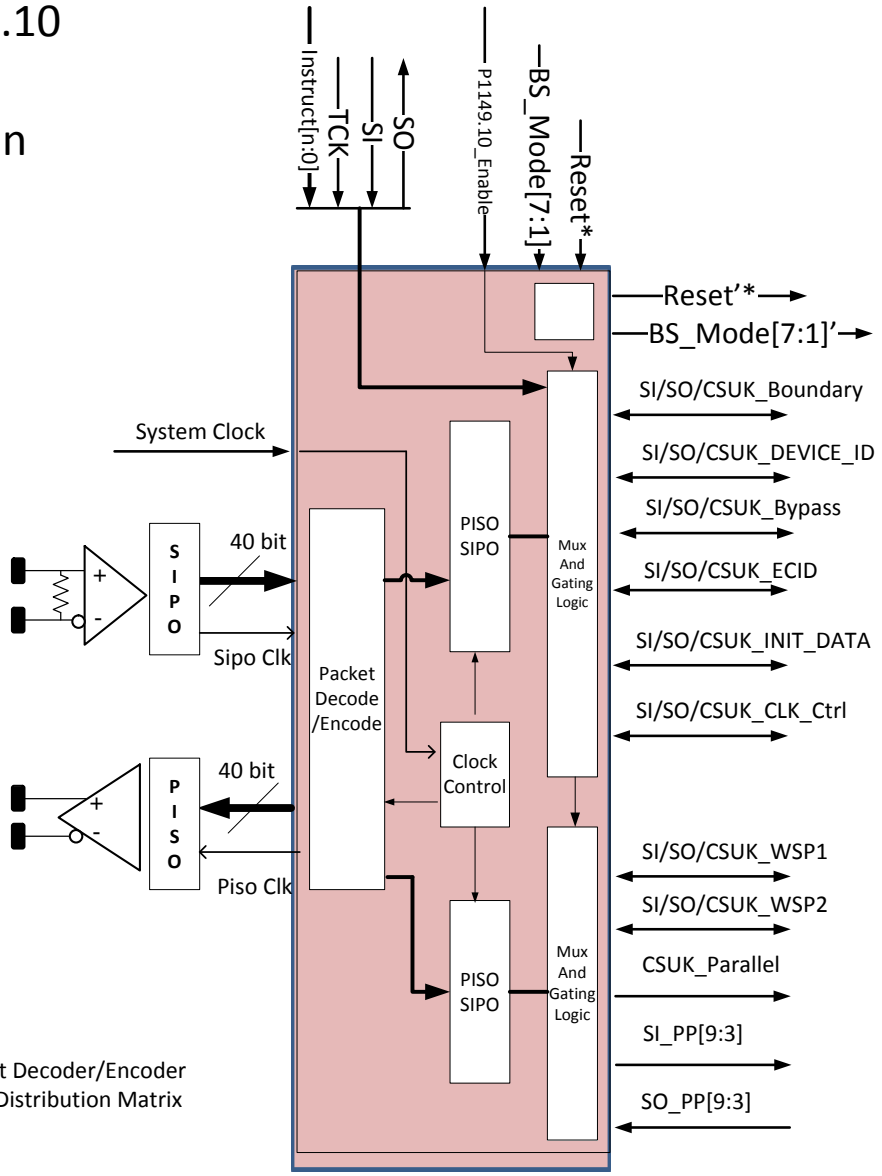
Define packet encoder/decoder & distribution Matrix (shaded area)

Define packets for packet decoder

Enable packet formats to validate link during testing (CRC32, running disparity, etc)

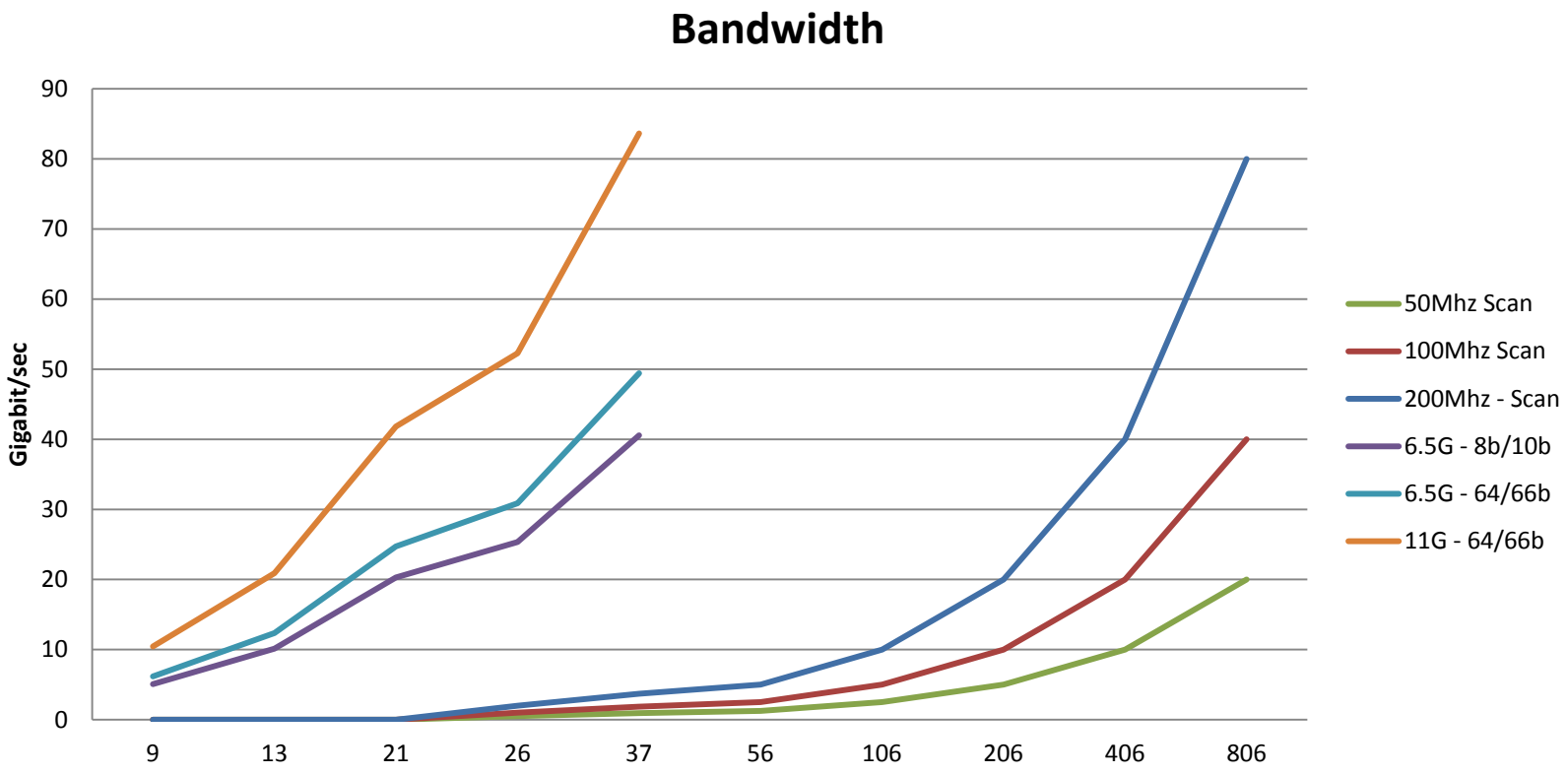
Define vendor documentation for Enabling P1149.10 interface, enabling Loopback and documenting requirements of interface (system clock, diff swing, Encoding (8b/10b, 64/66b, 128/130b etc)

Testing or implementation of SERDES BIST Is not an objective of the standard.



Packet Decoder/Encoder with Distribution Matrix

Common Clock = 80G/sec = 400 chains, 806 pins and 200Mhz operation
Embedded Clock SERDES = 80G/sec = User Defined chains, 37 pins and user defined Mhz



SI/SO+TAP+CLK		9	13	21	20	37	50	100	200	400	800
Chains		X	X	X	10	X	25	50	100	200	400
Tester Chan		9	13	21	26	37	56	106	206	406	806

SERDES = 4 pins + 4 pin TAP + clock. Channel bonding is used to have 2,4 and 8 Serdes lanes.
5 SERDES lanes just included for comparison purposes.
Bandwidth adjusted for encoding bit loss and 2% overhead of packet

Observations

80G bandwidth - 806 pins running 400 scan chains at 200Mhz

P1149.10 - More flexible with number of internal scan-chains and scan-chain architecture. Channel bonding can be used for higher bandwidth or multi-site testing
Users can make their own economic choices

Embedded clock SERDES is scalable. More bandwidth coming

Common Clock - reaching ceiling - needs more pins and higher clock rates

Normalizing for ATE pins Embedded Clock is 5 -10x bandwidth than common clock

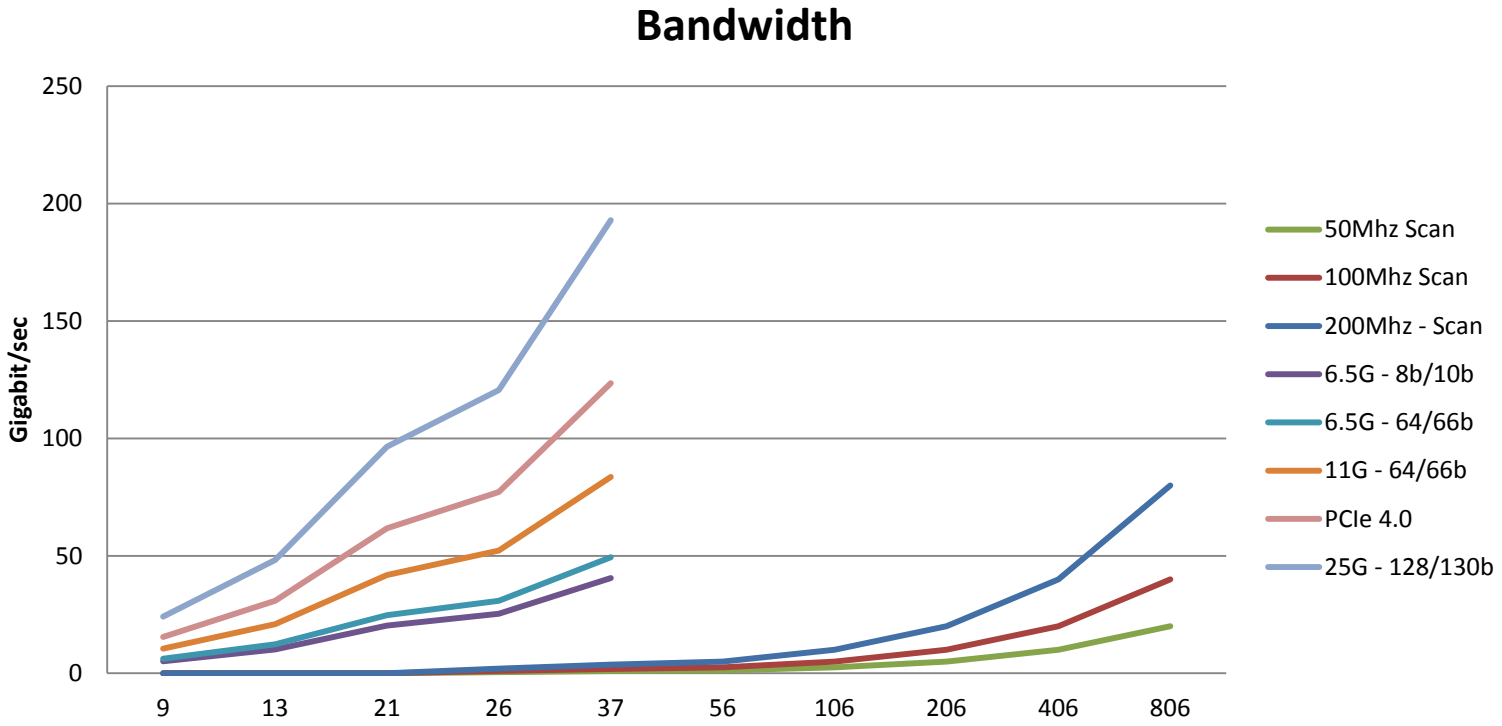
- Common Clock 100 pins = 10G @200mhz
  SERDES 10G bandwidth with 9 pins
  11 sites = 99pins = 110G total bandwidth

CEI-25G 2013 25G/sec 16G/sec PCIe 4.0 - coming

Credo, Snowbush, Avago all with 25G SERDES IP in 2013 - Others?
Some with 28G- Xilinx Virtex 7 HT (shipping) GTZ run to 28G/sec

2 CEI-25G SERDES will yield 50G bandwidth

Need 240 pins at 200mhz to equal one CEI-25G interface link



Cost Trade-offs

Probe Card:

P1149.10 requires Gigabit probe card ('increased' cost) and handler infrastructure

Compare with common clock requires increased cost probe card (800+ contacts for single location).

Handler

Requires gigabit connections but less of them. Could use (Coax however SATA, CAT-6A, Fiber are also choices).

Silicon

re-using mission mode SERDES so not expecting vendor to implement SERDES just for P1149.10. P1149.10 does not preclude dedicated SERDES either.

No use P1149.10 does not mandate it is used during wafer test. So one may use P1149.10 in later stage processes. Instrument access at benchtop, characterization and FPGA configuration.

The numbers

200	0	0	0	2	3.70	5	10	20	40	80
100	0	0	0	1	1.85	2.5	5	10	20	40
50	0	0	0	0.5	0.93	1.25	2.5	5	10	20
6.5G w/ 8b/10b	5.07	10.14	20.28	25.35	40.56					
6.5G w/ 64/66b	6.18	12.35	24.71	30.88	49.42					
11G w/64/66b	10.45	20.91	41.81	52.27	83.63					
16G PCIe 4.0	15.44	30.88	61.76	77.19	123.51					
25G w/ 128/130b	24.12	48.25	96.49	120.62	192.98					
SI/SO+TAP+CLK	9	13	21	20	37	50	100	200	400	800
Chains	X	X	X	10	X	25	50	100	200	400
Tester Chan	9	13	21	26	37	56	106	206	406	806