IEEE 1149.4 Mixed-Signal Test Bus Working Group Meeting Minutes

for
July 23rd, 2007

7:30 AM – 8:50 AM PDT

Meeting Agenda:

Time	Topic	Responsibility
7:30-8:50 AM	1. Review the meeting minutes for June 26th, 2007 2. Update/Review on ABSDL for: a. Straw Dog example. b. STA400 chip. 3. Update/Review on action items for ABSDL documentation draft. a. Review the last sentence of the introduction for section 10.4 - BSDL Documentation. b. Boundary-scan circuitry diagram for section 10.4.5. c. Verifying description of the multiple fanouts case using BSDL parser. d. Review Note 3 - statement on Errata Bulletin. 4. Other issues.	 Adam Ley Bambang Adam Ley Bambang Ken Adam Ley
8:50 AM	Meeting adjourned	Bambang

Meeting Attendees:

Name	Company
Adam Ley	Asset-Intertech
Adam Cron	Synopsys
Ken Parker	Agilent Technologies
Zafar Quadri	Solectron Corp.
Bambang Suparjo	Mentor Graphics

1. Review the Meeting Minutes for June 26th, 2007

The meeting minutes for June 26th, 2007 have been approved, suggested by Adam Cron and seconded by Zafar.

2. Update/Review on ABSDL for:

a. Straw Dog example.

The status is still pending.

b. STA400 chip.

The status is still pending.

3. Update/Review on action items for ABSDL documentation draft.

a. Review the last sentence of the introduction for section 10.4 - BSDL Documentation (Adam Ley).

The status is still pending.

b. Boundary-scan circuitry diagram for section 10.4.5 (Bambang).

The diagram has been reviewed with the following comments:

i. Adam Ley pointed out that the boundary scan registers to control the ABM switching network are not included in the ABM block. Further discussion identifies that the TBIC block has a similar issue.

ii. Another comment from Adam Ley is pin D for the ABM should refer to the signal applied from the boundary scan register.

iii. Ken gives comment on the boundary scan chain data shifting flow. When showing both data shifting flow (with arrow) and the boundary scan register order number, it may give an impression to the user that the boundary scan registers associated to TBICs and ABMs should follow the register/cell order shown in the diagram. A note will be provided to clarify that there is no restriction on the order of register/cell for shifting operation.

Bambang will update the diagram and provide a note based on the comments.

c. Verifying description of the multiple fanouts case using BSDL parser.

An 1149.1 BSDL file containing a sample of multiple fanouts case has been verified by Ken using the available BSDL parser. The file is shown in the appendix. There is no violation has been reported on the boundary scan registers at those fanouts. The only violation is related to BC_4 cell attached to the differential representative port. Adam Ley informed that there is a restriction in 1149.1 that BC_4 cannot be used as an observe cell for differential pins.

Adam Ley will do further verification on the boundary scan registers at the fanouts to check if correct data will be applied from the registers during INTEST. The file needs to be modified to include INSTEST instruction.

d. Review Note 3 - Statement on Errata Bulletin

The status is still pending.

4. Other Issues

The next meeting will be on August 22nd and 23rd, 2007 at 8 AM PDT.

5. The meeting adjourned at 8:50 AM PDT.

Appendix

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--------------------------------------------------------------------------------
-- DATE & TIME    :  Tue Jul  23 2007
-- File Type      :  BSDL for Top-Level Entity basic
--------------------------------------------------------------------------------

 entity basic is

    generic(PHYSICAL_PIN_MAP : string := "DW");

    port (
              BD1                  : inout        bit;
              BD2                  : inout        bit;
              DFIP                 : in           bit;
              DFIN                 : in           bit;
              DFOP                 : buffer       bit;
              DFON                 : buffer       bit;
              IN1                  : in           bit;
              IN2                  : in           bit;
              IN3                  : in           bit;
              OUT1                 : buffer       bit;
              OUT2                 : buffer       bit;
              TR1                  : out          bit;
              TR2                  : out          bit;
              TDI                  : in           bit;
              TMS                  : in           bit;
              TCK                  : in           bit;
              TDO                  : out          bit;
              TRST                 : in           bit;
              GND                  : linkage      bit;
              VDD                  : linkage      bit
         );

    use STD_1149_1_2001.all; -- Get IEEE 1149.1-2001 attributes and definitions

    attribute COMPONENT_CONFORMANCE of basic : entity is "STD_1149_1_2001";

    attribute PIN_MAP of basic : entity is PHYSICAL_PIN_MAP;


    constant DW : PIN_MAP_STRING :=
       "BD1: 6," &
       "BD2: 7," &
       "DFIP: 8," &
       "DFIN: 9," &
       "DFOP: 11," &
       "DFON: 12," &
       "IN1: 3," &
       "IN2: 4," &
       "IN3: 5," &
       "OUT1: 15," &
       "OUT2: 16," &
       "TR1: 13," &
       "TR2: 14," &
       "TDI: 2," &
       "TMS: 18," &
       "TCK: 1," &
       "TDO: 17," &
       "TRST: 19," &
       "GND: 10," &
       "VDD: 20";

    attribute PORT_GROUPING of basic : entity is

      "Differential_Voltage  ( (DFIP, DFIN), " &
                "(DFOP, DFON)) " ;

    attribute TAP_SCAN_IN of TDI : signal is true;
    attribute TAP_SCAN_MODE of TMS : signal is true;
    attribute TAP_SCAN_OUT of TDO : signal is true;
    attribute TAP_SCAN_CLOCK of TCK : signal is (5.00000000e+06, BOTH);
    attribute TAP_SCAN_RESET of TRST : signal is true;
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    attribute INSTRUCTION_LENGTH of basic : entity is 4;
    attribute INSTRUCTION_OPCODE of basic : entity is
        "extest (0000),"  &
        "bypass (1111),"  &
        "sample (0001),"  &
        "preload (0001)";

    attribute INSTRUCTION_CAPTURE of basic : entity is "0001";
    attribute REGISTER_ACCESS of basic : entity is
        "BOUNDARY (extest, sample, preload), " &
        "BYPASS (bypass)";

    attribute BOUNDARY_LENGTH of basic : entity is 18;
    attribute BOUNDARY_REGISTER of basic : entity is
      --- num       cell      port      function   safe  [ccell  disval  rslt]
       "0    (      bc_1,     OUT2,      output2,     X)," &
       "1    (      bc_1,     OUT1,      output2,     X)," &
       "2    (      bc_1,        *,      control,     0)," &
       "3    (      bc_1,      TR2,      output3,     X,      2,      0,    Z)," &
       "4    (      bc_1,        *,      control,     1)," &
       "5    (      bc_1,       R1,      output3,     X,      4,      1,    Z)," &
       "6    (      bc_1,     DFOP,      output2,     X)," &
       "7    (      bc_4,     DFOP,      observe_only,     X)," &
       "8    (      bc_1,     DFIP,        input,     X)," & -- captures DFIP
       "9    (     bc_1,      DFIP,        input,     X)," & -- captures DFIP
       "10   (     bc_4,      DFIP,      observe_only,     X)," &
       "11   (     bc_2,        *,       control,     0)," &
       "12   (     bc_7,       BD2,        bidir,     X,     11,      0,    Z)," &
       "13   (     bc_2,        *,       control,     1)," &
       "14   (     bc_7,       BD1,        bidir,     X,     13,      1,    Z)," &
       "15   (     bc_1,       IN3,        input,     X)," &
       "16   (     bc_1,       IN2,        input,     X)," &
       "17   (     bc_1,       IN1,        input,     X)";

end basic;
```