IEEE 1149.4 Mixed-Signal Test Bus Working Group Meeting Minutes

for
August 30th, 2007

8 AM – 12 PM PDT

Meeting Agenda:

Time	Topic	Responsibility
8 PM - 12-PM	1. Review the meeting minutes for July 23rd, 2007 2. Update/Review on the following action items: a. Review the last sentence of the introduction for section 10.4 - BSDL Documentation. b. Boundary-scan circuitry diagram for section 10.4.5. c. Verifying the description of the multiple fanouts case. d. Review Note 3 - statement on Errata Bulletin. 3. Overall review on the draft.	 Adam Ley Bambang Adam Ley Adam Ley All
12 PM	Meeting adjourned	Bambang

Meeting Attendees:

Name	Company
Adam Ley	Asset-Intertech
Adam Cron	Synopsys
Ken Parker	Agilent Technologies
Zafar Quadri	Solectron Corp.
Bambang Suparjo	Mentor Graphics

1. Review the Meeting Minutes for July 23rd, 2007

a. Correction on minute 3c on statement "Adam Ley informed that there is a restriction in 1149.1 that BC_4 cannot be used as an observe cell for differential pins".

The correct statement is "Adam Ley informed that for any pins where INTEST is defined as a support instruction, BC_4 cannot be used as observe cells".

b. The meeting minutes for July 23rd, 2007 have been approved with the correction in minute 3c, suggested by Adam Cron and seconded by Zafar.

2. Update/Review on the following action items:

a. Review the last sentence of the introduction for section 10.4 - BSDL Documentation (Adam Ley).

The introduction for section 10.4 has been updated:

The purpose of developing BSDL (Boundary Scan Description Language) extensions for IEEE Std 1149.4 is to define the mandatory means to document the mixed-signal test features of a device designed to be compliant with this standard. The information to be documented includes the control structures for the Test Bus Interface Circuit (TBIC) and Analog Boundary Modules (ABM). This information, along with the BSDL elements mandated by IEEE Std 1149.1, can be used to facilitate automatic pattern generation for interconnect testing and discrete component testing at the board level.

b. Boundary-scan circuitry diagram for section 10.4.5 (Bambang).

The diagram has been reviewed with the following comments:

i. For TBICN, replace "Base" with "Base, No Partition".

ii. On the related issue, TBIC(N) in Figure 27 needs to be replaced with TBICN.

iii. Use ticker line for core and chip boundaries.

c. Verifying description of the multiple fanouts case (Adam Ley).

When supporting INTEST, BC_4 cannot be used as an observe cell for any pins. Table B.11 in IEEE Std. 1149.1 is the main reference for this discussion. For this reason, if observe cell is needed when INTEST is supported, use other cell type. Figure 55 needs to be split into two diagrams; one without INTEST where using BC_4 is fine, and the other is when INTEST is supported where in this example BC_4A is used for observe cell. Adam Ley will review further rule 10.4.4.5.2.

d. Review Note 3 - Statement on Errata Bulletin

The status is still pending.

3. Overall review on the draft

Reviewing the BSDL example:

Ken identified that some of the cells' number in BSDL file example do not match with the cells' number shown in the diagram. Bambang will review the file.

4. The meeting adjourned at 12 PM PDT.