Implementing and Using a Mixed-Signal Test Bus

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Tutorial outline

- Introduction to Mixed-Signal Boundary Scan and Test
  - 1149.1, .4, and LF analog test buses
- Architecture and Design of 1149.4
  - Architecture, Instruction set, ABM & TBIC design
- System Test Methodologies
  - Test automation, BSDL
  - System test methods

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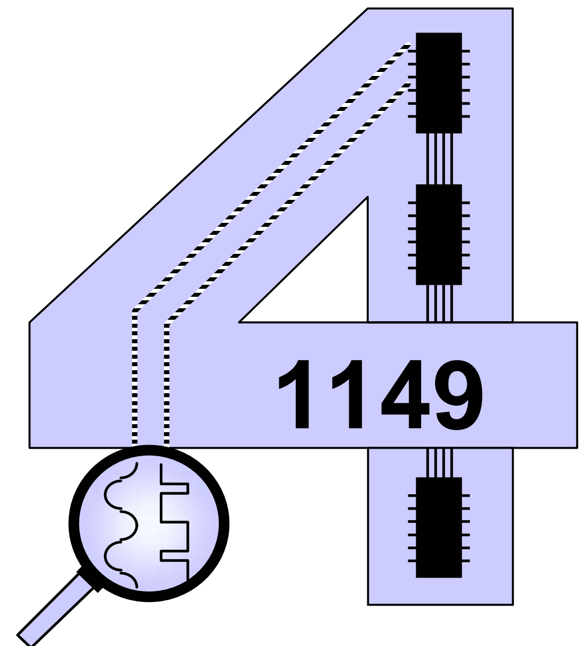
Introduction to Mixed-Signal Boundary Scan



Introduction to Boundary Scan

- Motivation for developing boundary scan
  - Circuit board size getting too small/expensive to probe
  - Need standard access to on-chip test capabilities
- Expected benefits
  - Lower test cost – less hardware, complexity
  - Faster time to market – more automation, reuse
- Result: JTAG, IEEE 1149.1 - 1990
  - Serial, digital access to all IC “digital” pins
  - Standard 4~5 pin Test Access Port

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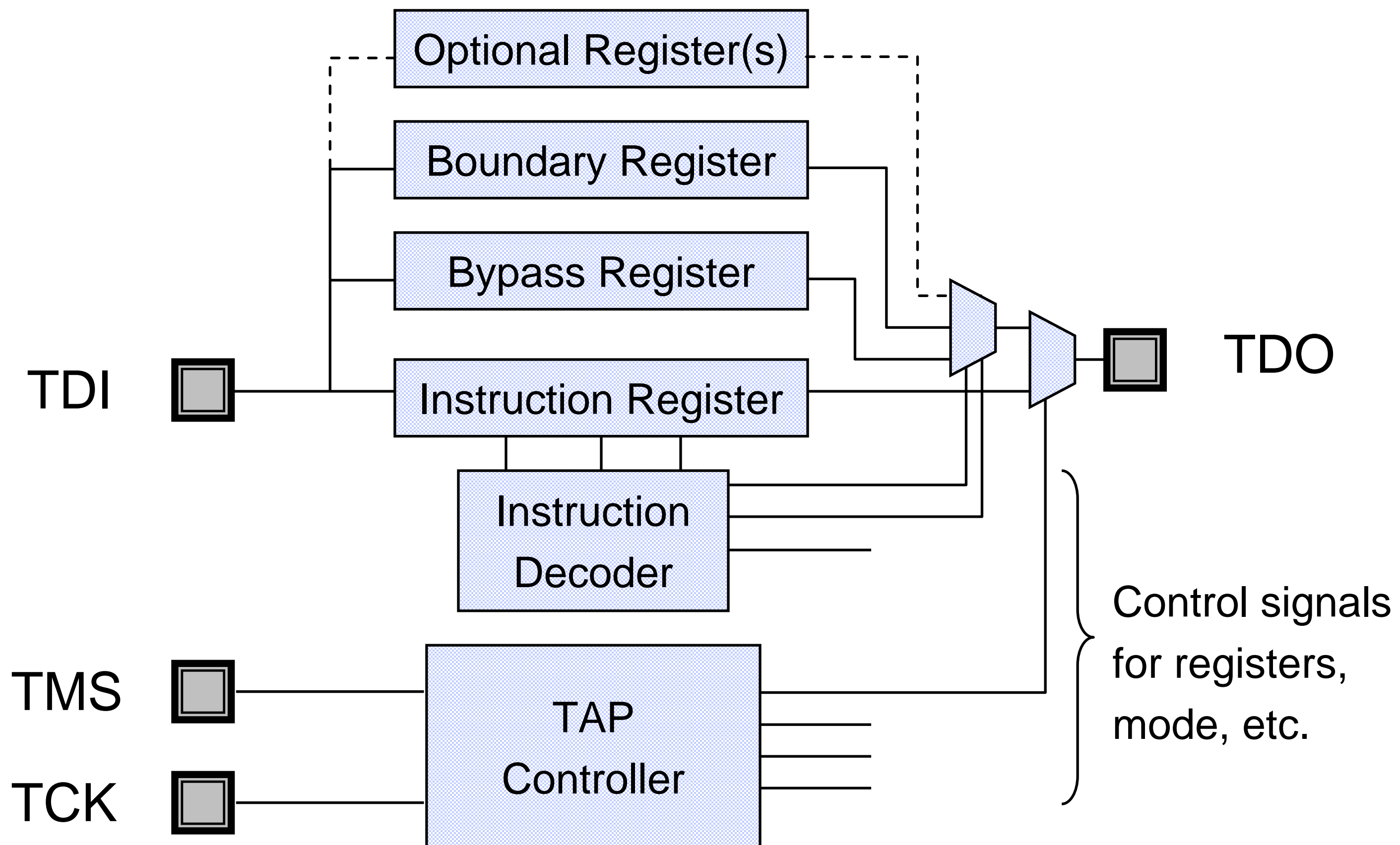
1149.1 digital control

(only mandatory TAP pins shown)

- 4 pin Test Access Port used for all control and observation



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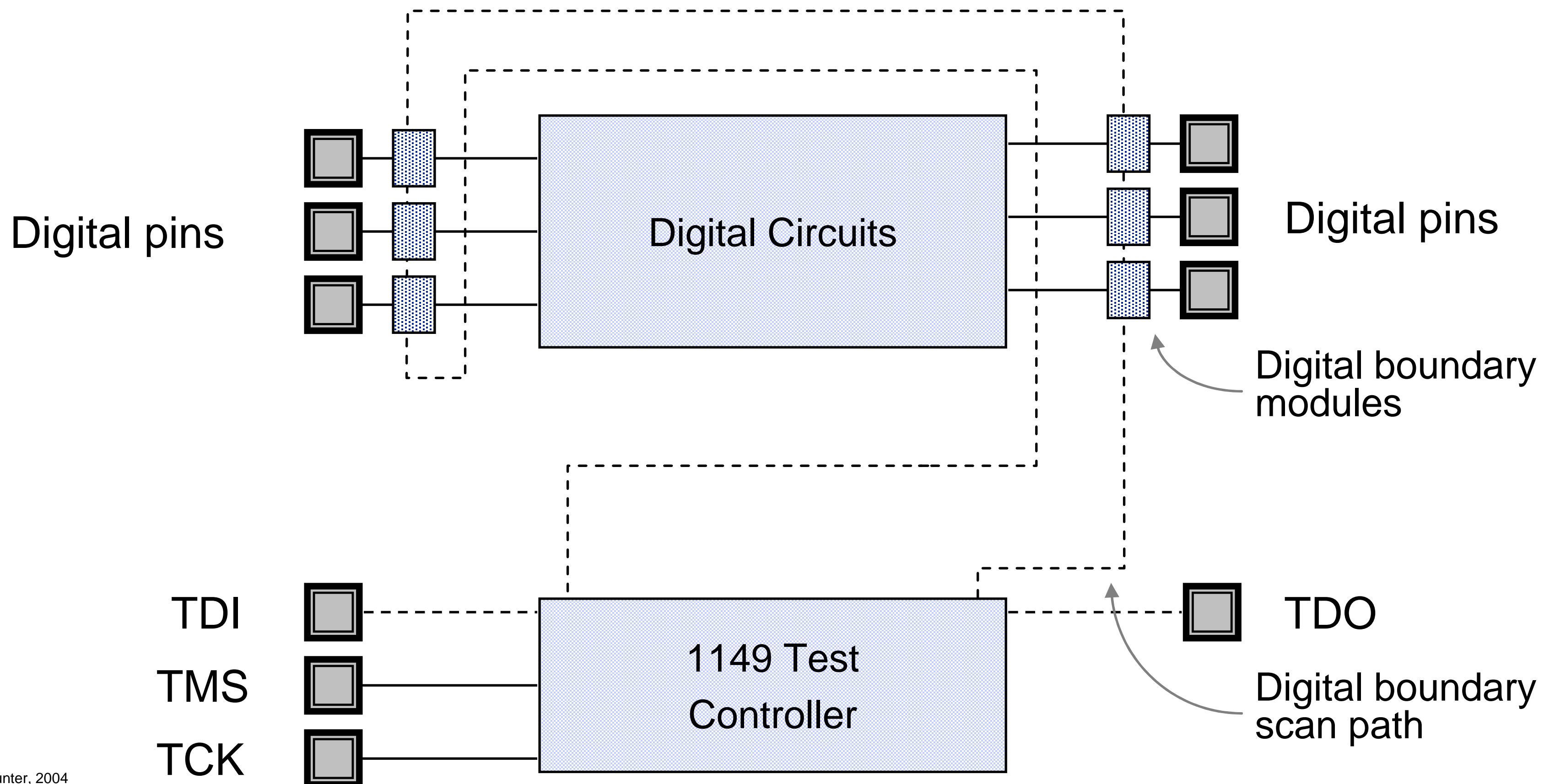
1149.1 view of digital IC



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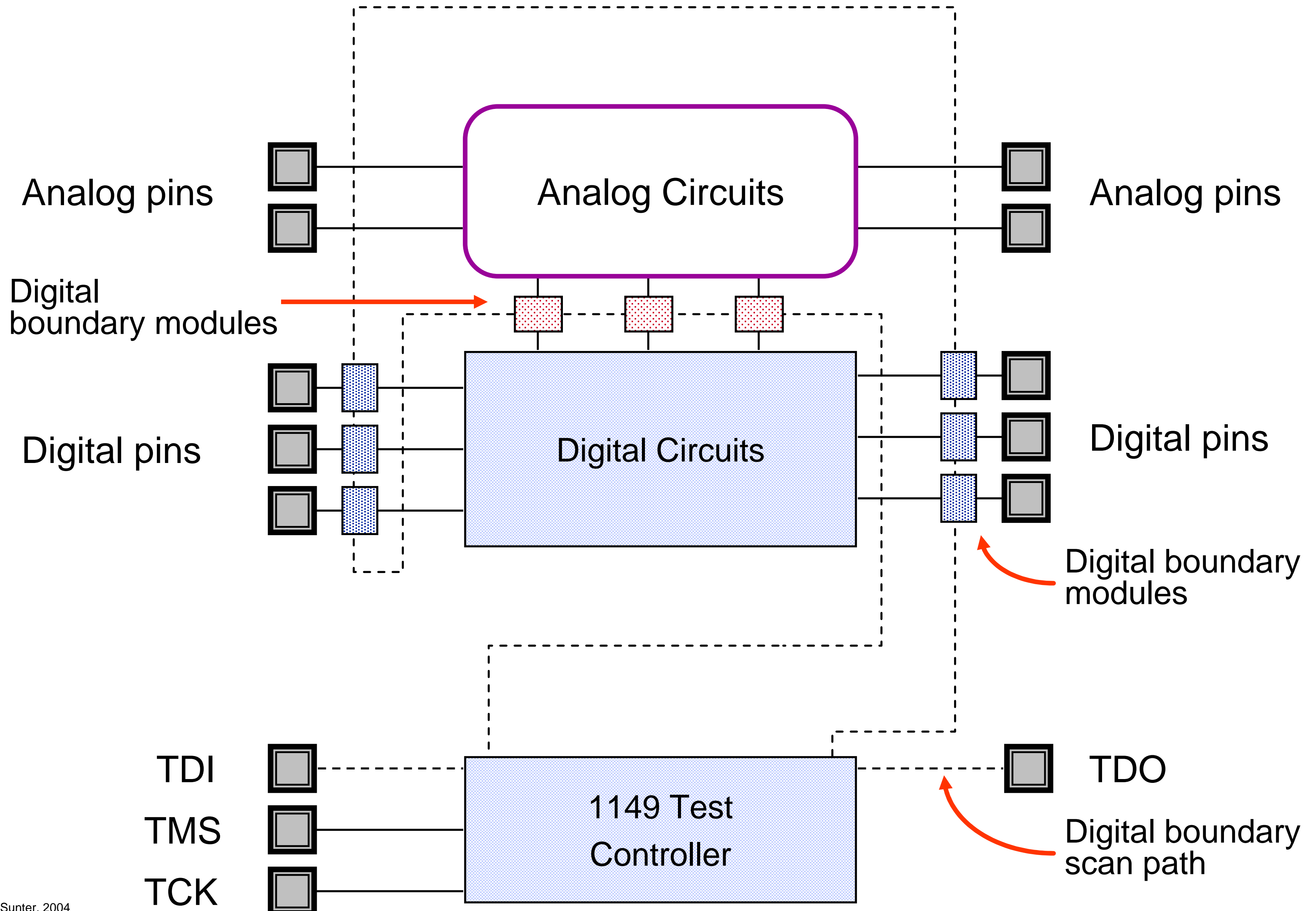
1149.1 view of mixed-signal IC



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What's wrong with this picture?

- Analog pins not handled by 1149.1
  - New ICs & boards with mixed-signal is >50%
  - Number of digital pins with analog circuitry is growing
    - termination resistors, pull-ups, capacitors
- Differential pins not handled by 1149.1
  - Number of differential pins growing
    - Higher speed, lower V_{DD}, lower power, less EMI
- Digital ICs can have significant analog content
  - V_{BIAS}, V_{REF}, on-chip V_{DD}/V_{BB} generation

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Introduction to 1149.4

- Motivation for developing boundary scan
  - 1149.1 success is limited by analog circuitry
  - Board passive components getting too small to probe
  - *P1149.4 Working Group started in 1992*
- Expected benefits
  - Lower test cost, time to market, … *for all boards*
- Result: IEEE 1149.4 - 1999
  - Serial, analog access to all IC “analog” pins
  - Standard 2 pin Analog TAP (low frequency, analog bus)

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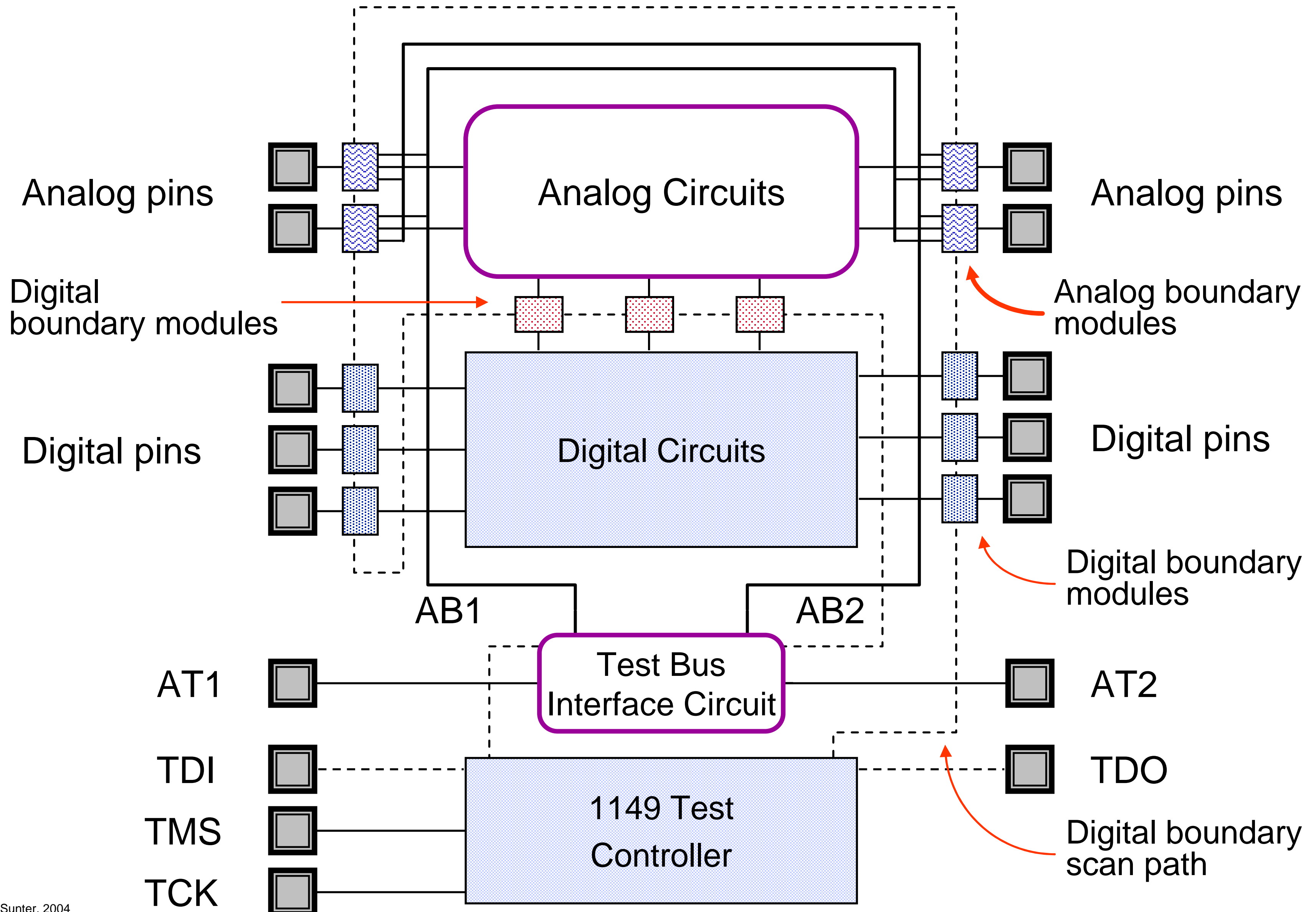
1149.4 view of mixed-signal IC



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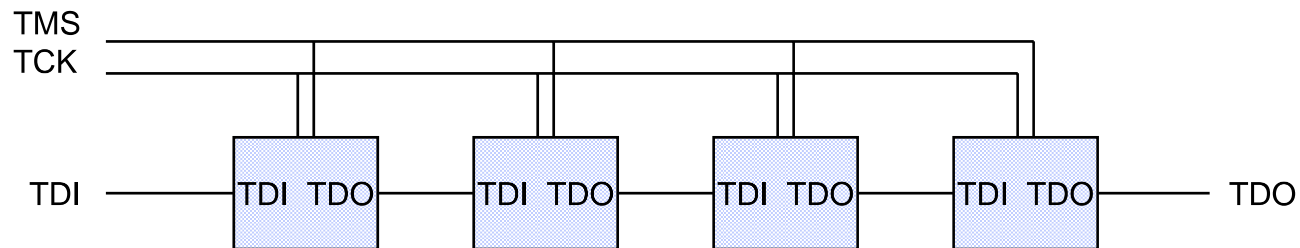
1149.1 board-level view

- Parallel control bus
- Serial (or parallel) data bus



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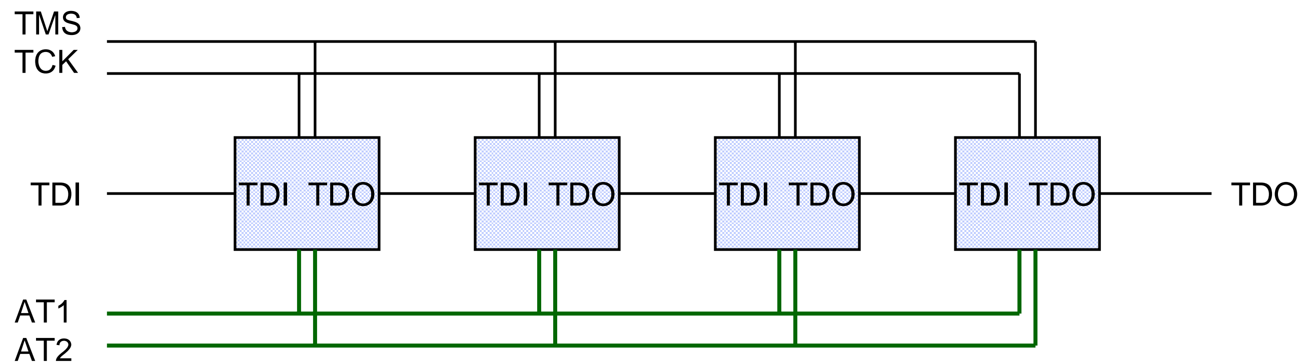
1149.4 board-level view

- 1149.1 control and data buses
- Parallel analog bus



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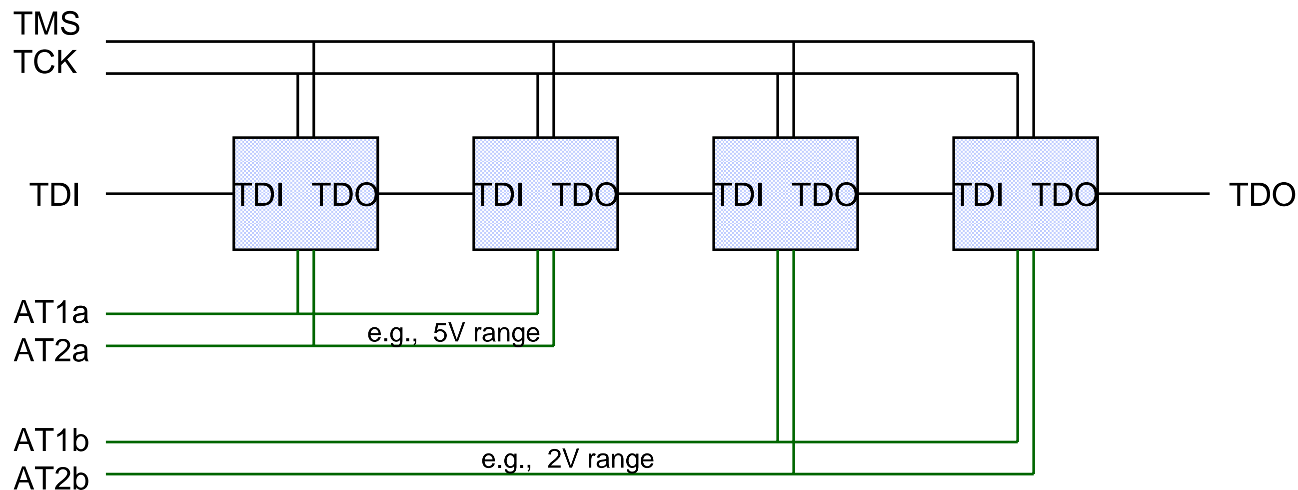
1149.4 board-level view

- Alternative arrangement to accommodate ...
  - Multiple voltage ranges
  - Diverse frequency ranges
  - Large number of devices



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Why low frequency bus?

LF: <100 kHz (allows <1ms measurements)

- Won't affect, or be affected by, other circuitry
  - Coupling via interconnect C and L is minimal at LF
  - Most interference is from digital at HF – easy to LPF
- Relatively cheap to measure accurately
  - 16~24b resolution Generators/Digitizers are LF
  - Can implement on-chip using sigma-delta
- 1149.4 requires LF, but does not preclude HF

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Why analog 2-wire bus?

- Continuous time, voltage, current
  - Choose sampling rate, accuracy, precision… post-silicon
  - Many parameters inherently analog

- Lowest power, widest voltage range
  - CMOS transmission gates + logic: ≈ zero DC current
  - CMOS transmission gates convey voltages outside rails

- Two wires
  - Stimulus/response, force/measure, ± differential

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Myths about LF analog bus

- ✗ Not useful for HF analog circuit test
  - ✓ Can measure DC biases, termination impedances, and can drive/monitor AC via on-chip mod/demod
- ✗ Not useful for digital circuit test
  - ✓ Can measure output drive (V_{OL}/ I_{OL}), V_{IL}, pull-ups, V_{DD}, … without probing the pins
- ✗ Slow – long test times
  - ✓ Up to 50 measurements/ms, with 16-bit accuracy
- ✗ 1149.4 is a set of constraints for a LF analog bus
  - ✓ All rules had to satisfy criteria of "necessary & sufficient"

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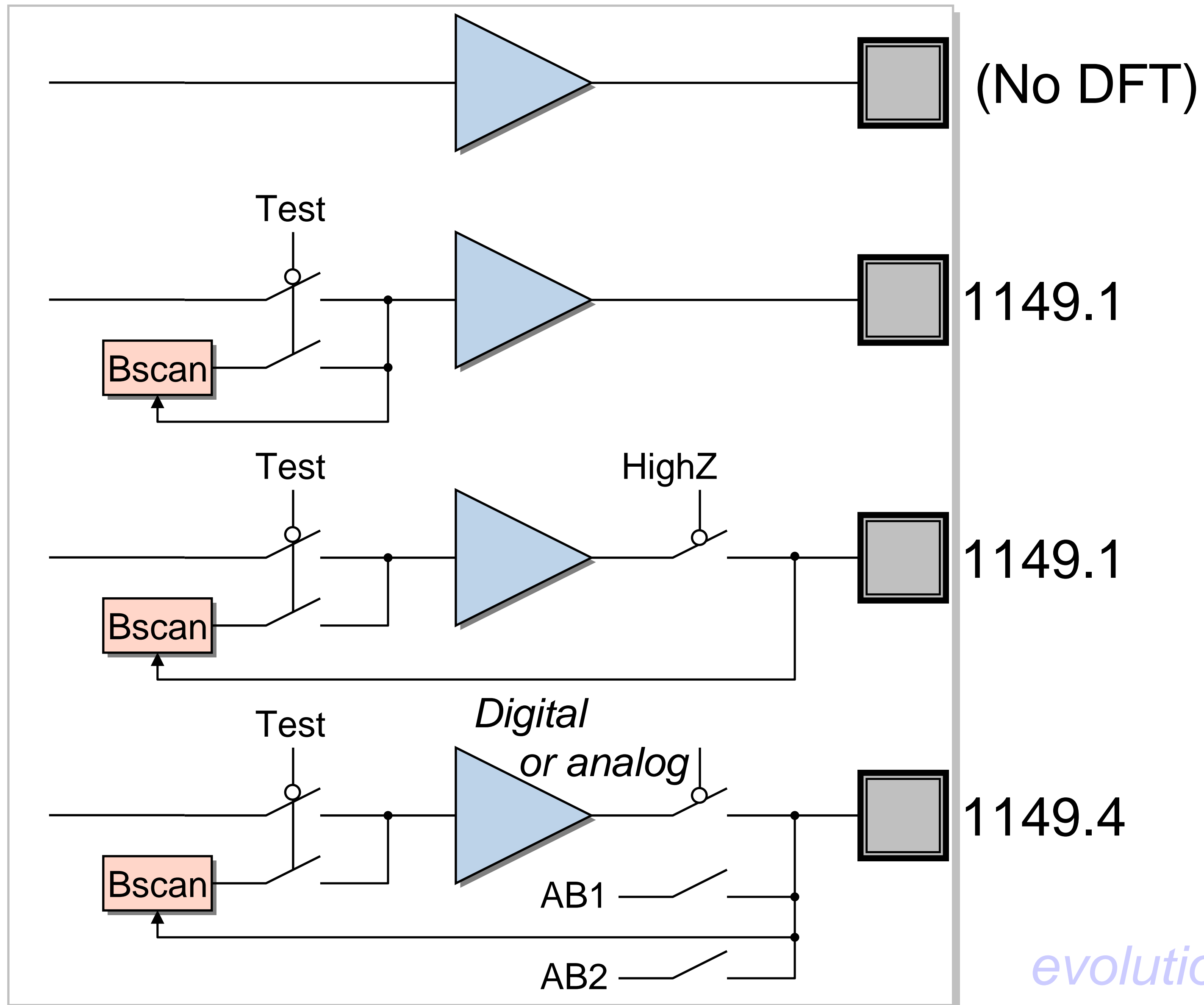
Pin test circuitry overview



evolutionary

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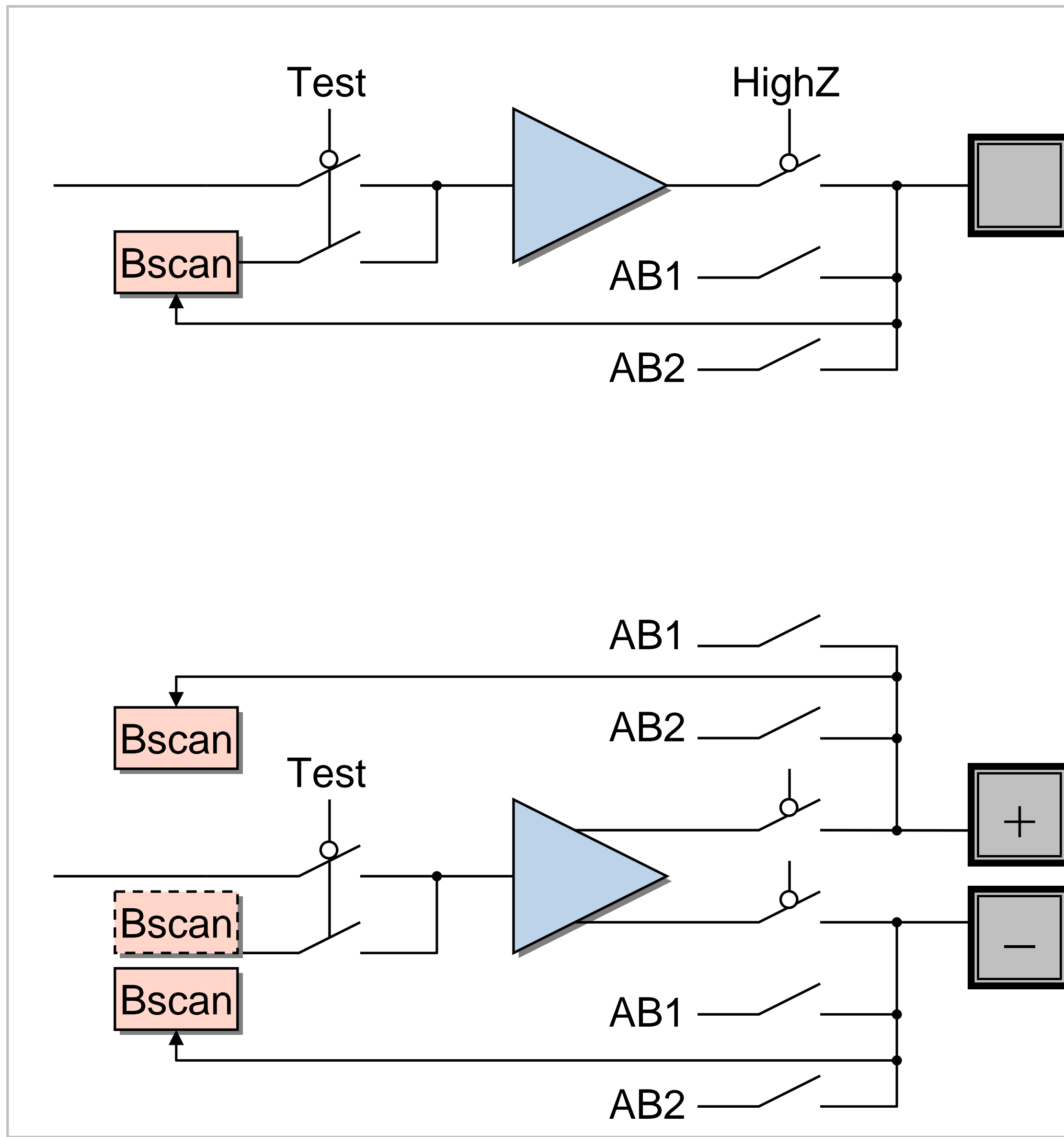
Pin test circuitry overview



1149.4
Single-ended
Digital or analog

1149.4
Differential
Analog

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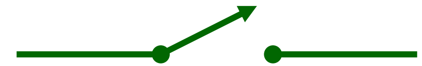
Required test functions for each pin

Each "analog" pin shall be able to

Achieve isolation



- Connect to core
- Disconnect from core, i.e., from all active circuitry ("CD state")

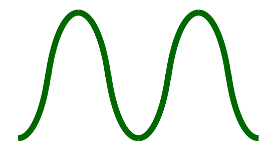
Perform tests equivalent to 1149.1

- Drive pin's V_{MAX} , V_{MIN} (D.C.)
- Compare V_{PIN} to pin's V_{TH}, where $V_{TH} \approx (V_{MIN}+V_{MAX})/2$

101101

Facilitate analog parametric tests

- Deliver analog ground (V_G) via power rail
- Deliver current to pin via AT1 pin and AB1 bus
- Monitor pin's voltage via AB2 bus and AT2 pin



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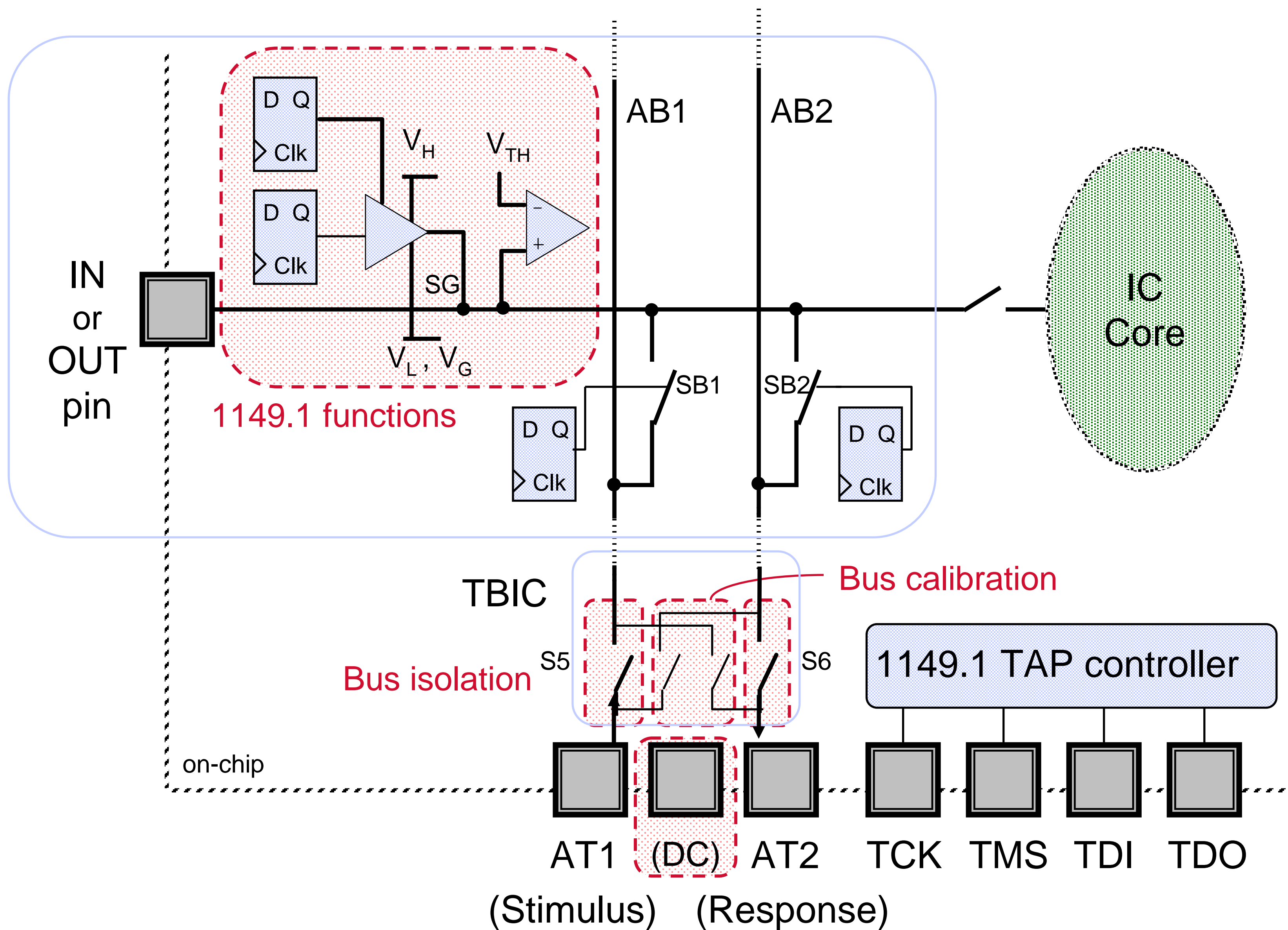
Required test functions



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Test pins

Pin	Name	Function
TCK	Clock	Rising edge latches TMS, TDI Falling edge updates TDO
TMS	Mode Select	Determines next state
TDI	Data In	Instructions or scan data
TDO	Data Out	Test results or for next chip
TRST	$\overline{\text{Reset}}$	Resets test circuitry (optional)
AT1	Analog Test	Stimulus current bus
AT2	Analog Test	Resultant voltage bus
AT1N	Analog Test	Inv. stimulus current (optional)
AT2N	Analog Test	Inv. resultant voltage (optional)

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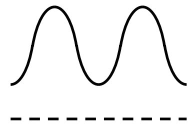
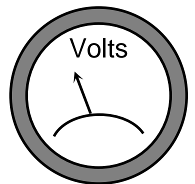
Analog Test Access Port (ATAP)

AT1: stimulus input

- at least capable of conveying ±100 μA
  - may be any combination of AC and DC
  - DC–10 kHz minimum bandwidth (±0.04 dB/ ±0.5%)
  - sufficient for state-of-the-art ATE to achieve <1% accuracy



AT2: response output



- at least capable of conveying ±100 mV
  - range at ABM: V_{SS}–100 mV to V_{DD}+100 mV
  - ensures that protection diodes are not activated

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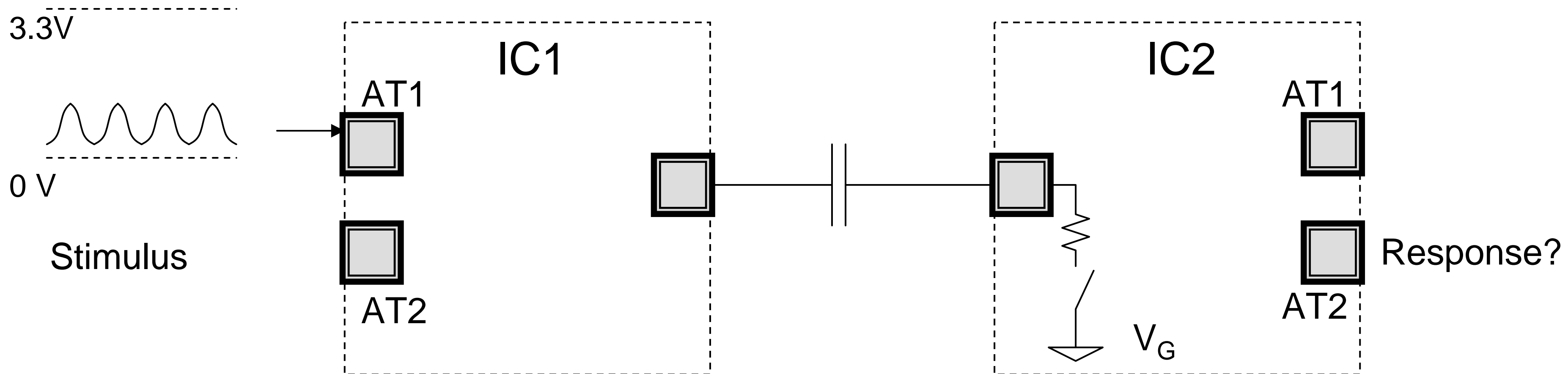
V_{SS} – 100 mV ?

- Why does voltage range of analog buffer need to extend 100 mV outside power rails?



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< 100 µA and < 100 mV ?

- Max switch resistance permitted is 10 kΩ
  - 1 kΩ appears optimal
  - Switch resistance is non-linear
  - >100 µA may cause >1% distortion and inaccuracy
- CUT impedance for 1% accuracy is 10 Ω ~100 kΩ
  - 1kΩ is geometric mean – 100 µA causes 100 mV
  - Larger AC voltage swing around V_{SS} or V_{DD} may activate protection diodes
- But … for some measurements, >1 mA is OK !

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Core access

- Not required, and has no rules
  - Must not interfere with boundary tests
  - Permit separate analog buses for boundary, core
- Facilitates …
  - Reusable, *ad hoc* tests for random analog circuitry
    - Within company, from IP suppliers, and from universities
  - Systematic parametric test access
    - Measure temperature, impedance, drive, switching point, …
    - Inject corrected signals, analog faults, deviations, …

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Feature overview

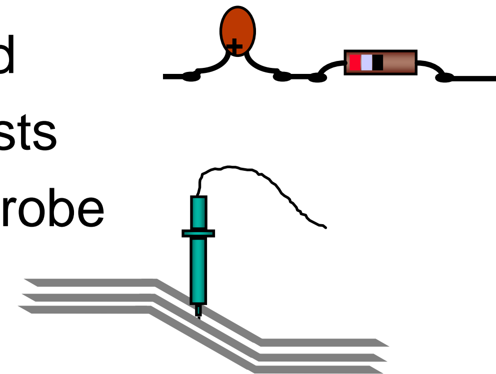
Capabilities

- Continuous time voltage & current access, via 2 analog pins
- Measure R, C, L, drive, etc. with <1% accuracy
- True differential access, and other options
- 1149.1-compliant

Mixed-signal tester per pin   +   core access

Benefits/value

- Parametric structural test of IC & board
- Standard access: reusable analog tests
- *In situ* diagnosis/test: virtual guided probe
- Infrastructure for self-test



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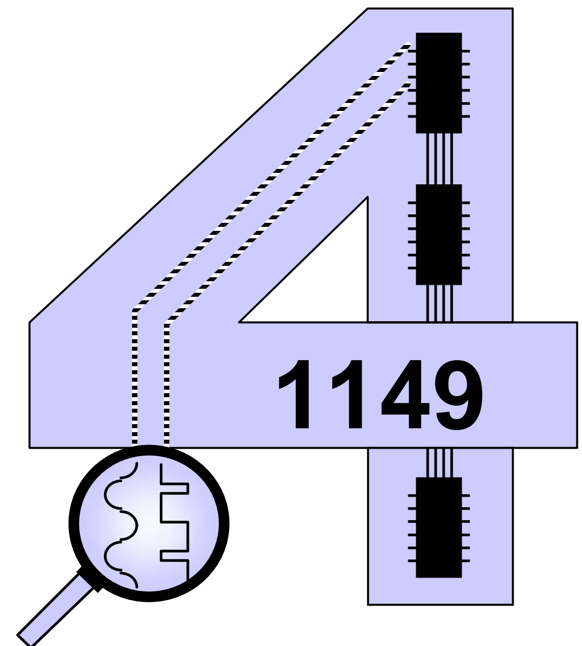
Architecture and Design of 1149.4



Outline

- Design of ABM, TBIC, TAP
- Details
  - Switches, core disconnect
  - Differential pins
  - Design vs. accuracy, speed
  - On-chip access
- Accessing HF signals
- Example ICs

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1149.4 Circuit Implementation

C
D Q
Clk
D
D Q
Clk
V_H
V_{TH}
−
+
AB1
AB2
IC Core
V_L, V_G
B1
B2
D Q
Clk
D Q
Clk
ABM
TBIC
1149.1 TAP controller
on-chip
AT1 (DC) AT2 TCK TMS TDI TDO
(Stimulus) (Response)

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ABM switch settings in EXTEST

data	control	AB1	AB2	←switch
D	C	B1	B2	
0	0	x	x	CD (tristate)
1	0	x	x	Drive “ground” out
data	1	x	x	Drive data out (1149.1)
x	x	1	x	Connect pin to AB1
x	x	x	1	Connect pin to AB2

x = don’t care

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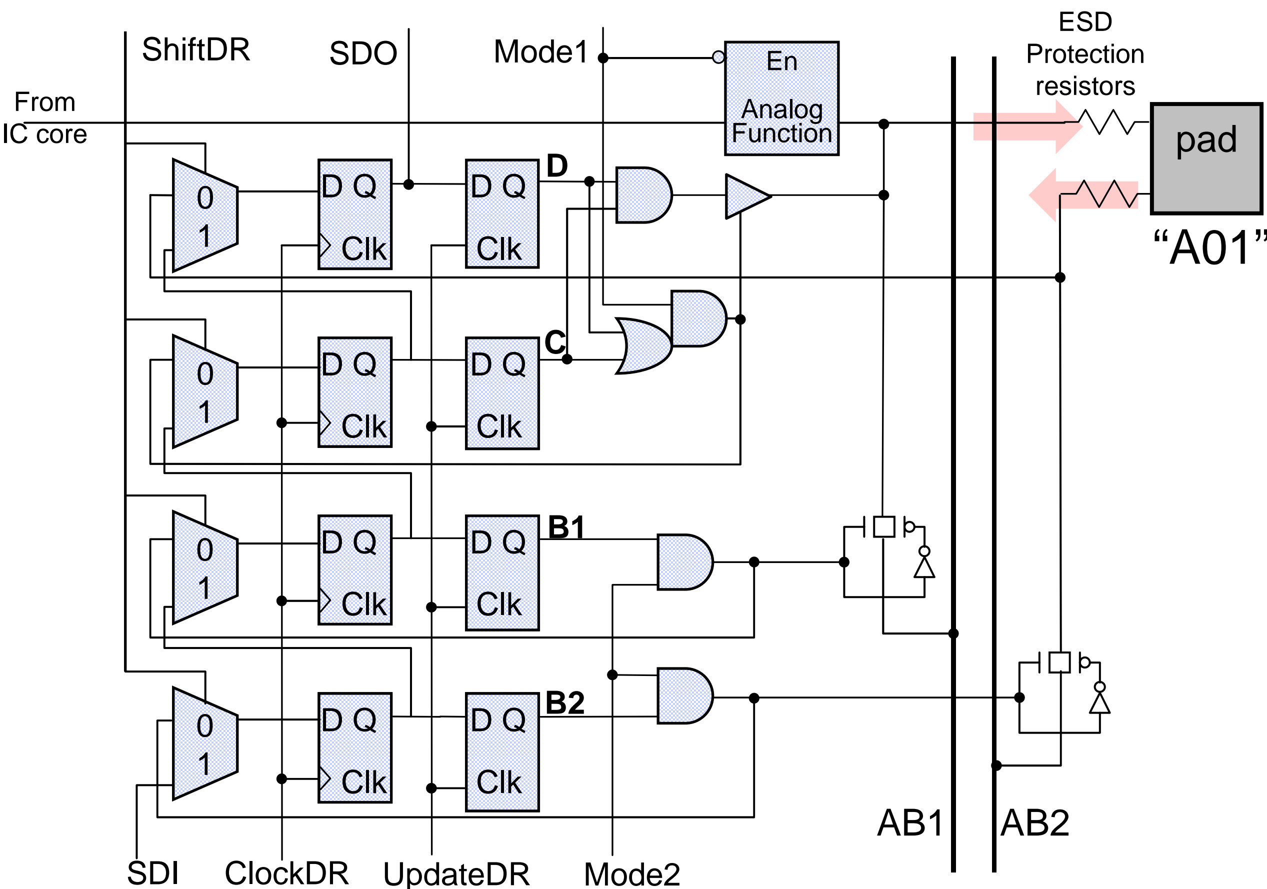
Example ABM schematic



Where is the V_{TH} comparator ?

What is value of V_{TH} ?

What is value of V_G ?

How would you modify this to handle a digital I/O pin?

Lines from my_bscan_cells.all

constant LV_B2: CELL_INFO:=
((INTERNAL, EXTEST, UPD),
(INTERNAL, SAMPLE, ZERO));

constant LV_B1: CELL_INFO:=
((INTERNAL, EXTEST, UPD),
(INTERNAL, SAMPLE, ZERO));

constant LV_D: CELL_INFO:=
((BIDIR_IN, EXTEST, PI),
(BIDIR_OUT, EXTEST, PO),
(BIDIR_IN, SAMPLE, PI),
(BIDIR_OUT, SAMPLE, PO),

constant LV_C:CELL_INFO:=
((CONTROL, EXTEST, UPD),
(CONTROL, SAMPLE, PI));

Lines from my_chip.bsdl file

-- this end closest to TDO

--num	cell	port	function	safe	[ccell	disval	rslt]
" 0	(LV_D,	A01,	bidir,	0,	1,	0,	Z),"&
" 1	(LV_C,	*,	control,	0)," &			
" 2	(LV_B1,	*,	internal,	0)," &			
" 3	(LV_B2,	*,	internal,	0)," &			

etc.

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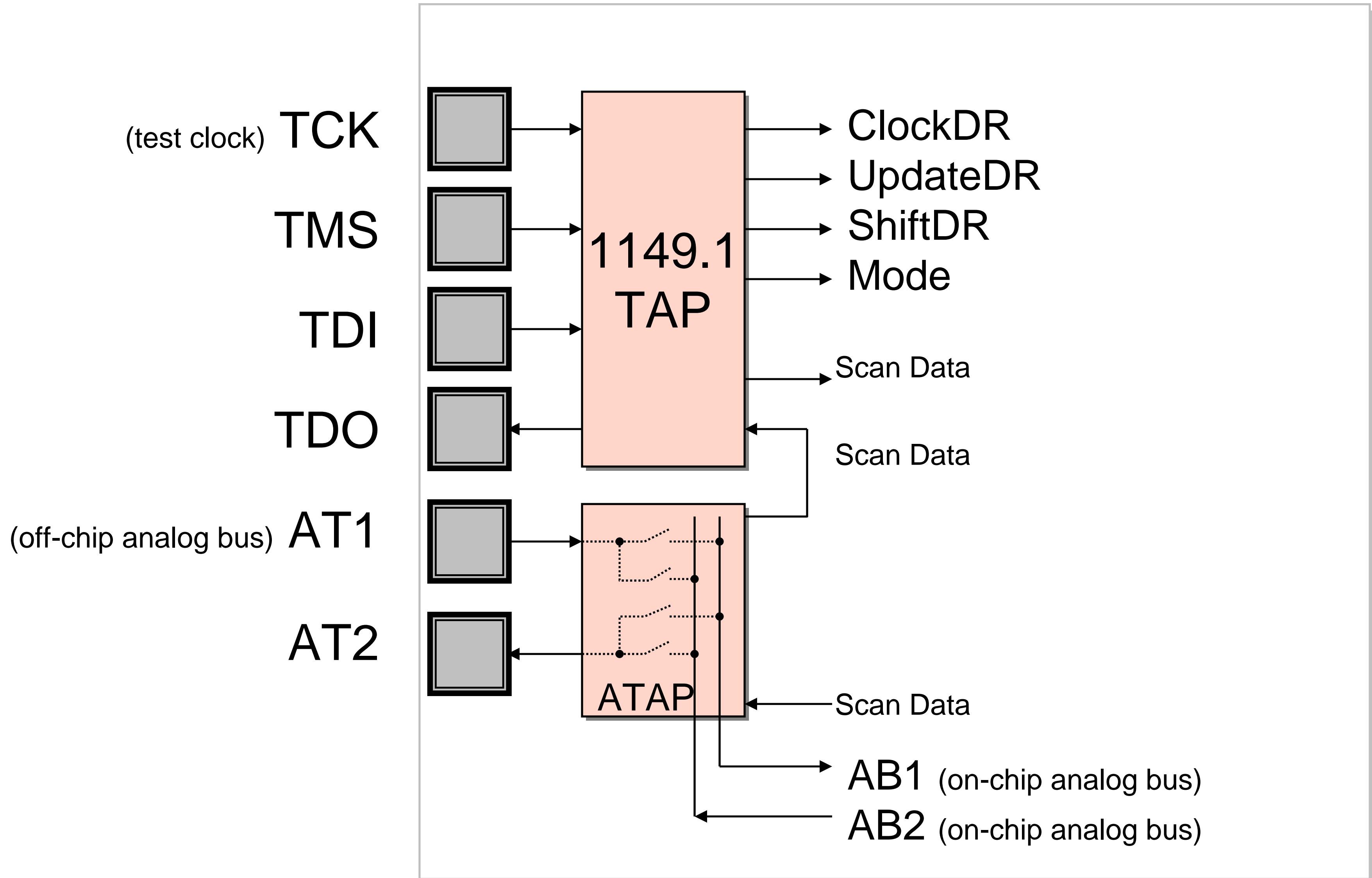
.1 and .4 TAP overview



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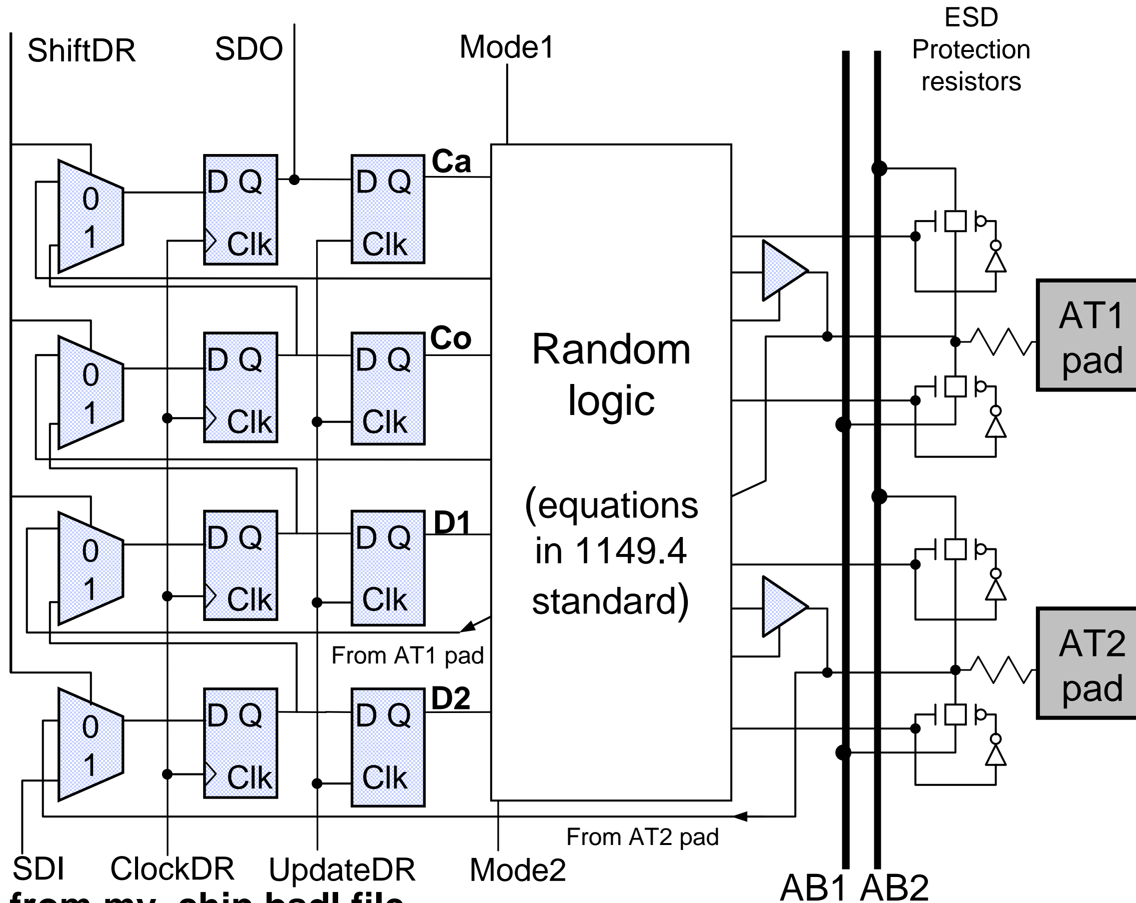
Example TBIC schematic



Lines from my_bscan_cells.all
constant LV_CA: CELL_INFO :=
((INTERNAL, EXTEST, X),
(INTERNAL, SAMPLE, X)),

constant LV_CO: CELL_INFO :=
((CONTROL, EXTEST, X),
(CONTROL, SAMPLE, PI)),

constant LV_D: CELL_INFO:=
((BIDIR_IN, EXTEST, PI),
(BIDIR_OUT, EXTEST, PO),
(BIDIR_IN, SAMPLE, PI),
(BIDIR_OUT, SAMPLE, PO)),

Lines from my_chip.bsdl file

-- this end closest to TDO

--num	cell	port	function	safe	[ccell	disval	rslt]
“ 20	(LV_Ca,	*,	internal,	0),"&			
“ 21	(LV_Co,	*,	control,	0),“ &			
“ 22	(LV_D,	AT1,	bidir,	0,	21,	0,	Z),“ &
“ 23	(LV_D,	AT2,	bidir,	0,	21,	0,	Z),“ &

etc.

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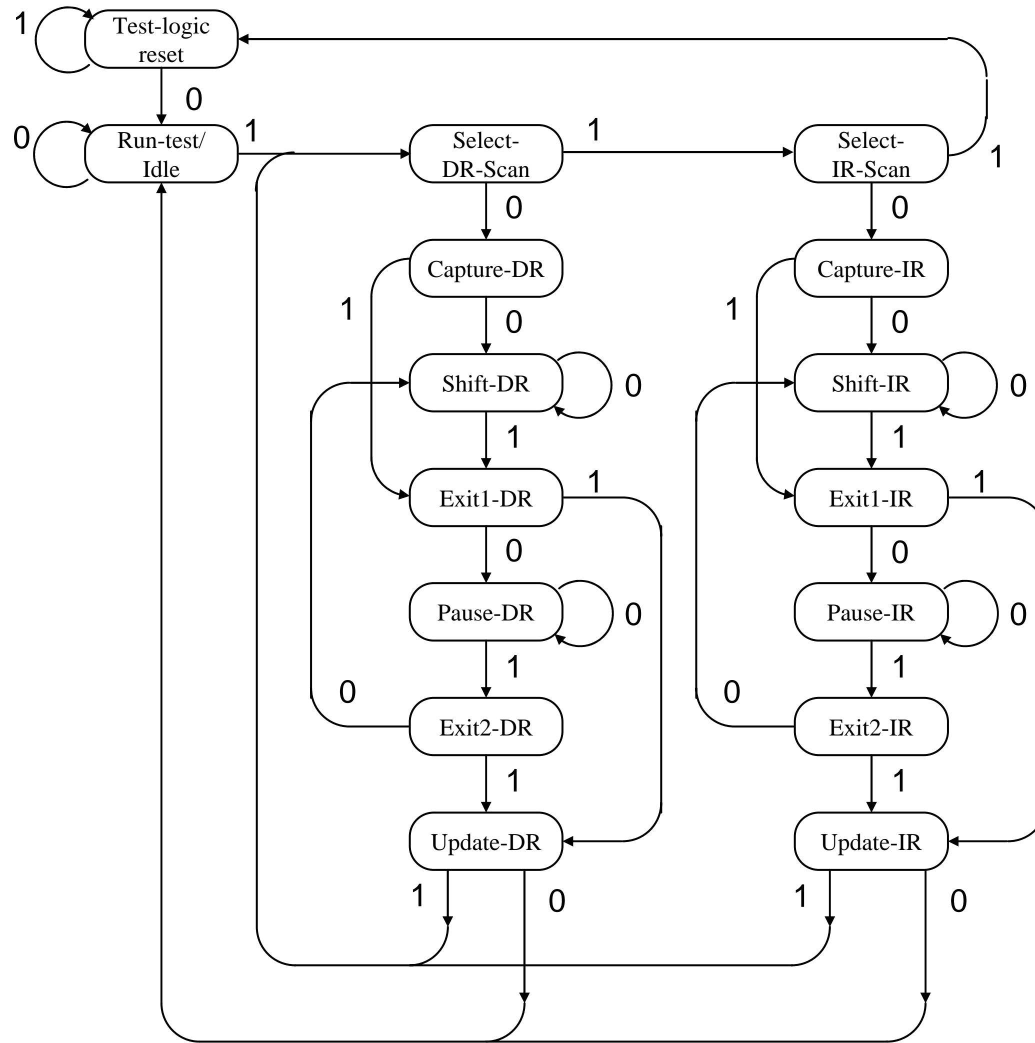
TAP state diagram (1149.1)



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The state transitions are determined by the value of TMS on the rising edge of TCK.

RTL synthesis

- TAP controller typically needs one more bit in IR
  - Analog mode, or *PROBE* instruction
- ATAP and ABMs
  - All synthesizable logic, in IC core, except
    - Transmission gates
    - Connections to pad
    - Optional analog buffers
    - Optional analog comparators
    - Must ensure that analog bus is not “optimized” by synthesis

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1149.4 Instructions

- *EXTEST*
  - Disable mission-mode influence of pins ("Core Disconnect")
  - Drive any pin to VDD/VSS, sample its logic value, access via AT1/AT2
- *PROBE*
  - Mission-mode
  - Sample any pin's logic value, access via AT1 and/or AT2
- *INTEST*
  - Analog pins: same as *PROBE*
  - Digital pins: same as 1149.1 (plus access via AT1/AT2)
- *CLAMP, HIGHZ, BYPASS* same as 1149.1

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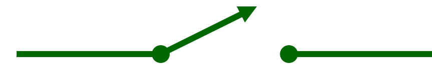
What is a ‘switch’ in 1149.4 ?

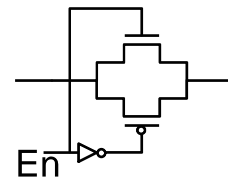
- Allows signals to propagate from one wire to another
- Can be disabled to isolate one signal from the other
- Does *not* need to have ‘low’ impedance (500Ω is OK)

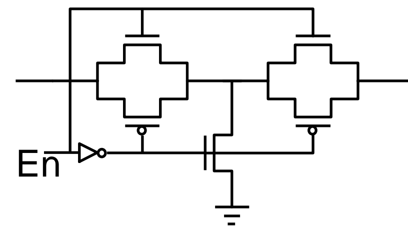
Examples

- CMOS transmission gate
  - allows bi-directional current flow

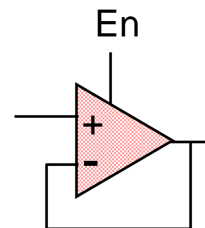


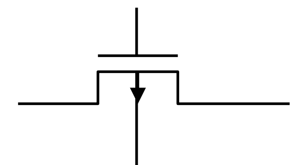
- Voltage buffer; 0 < gain < 1





- Current buffer; 0.5 < gain < 2





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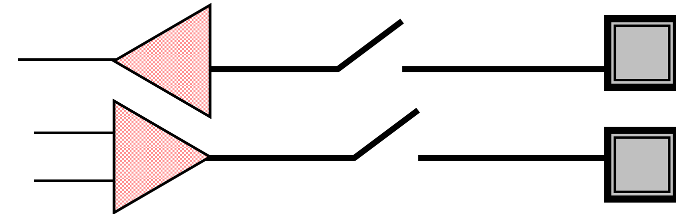
Achieving isolation: CD state

(Core Disconnect)

Ideal isolation

(disconnect, zero influence)

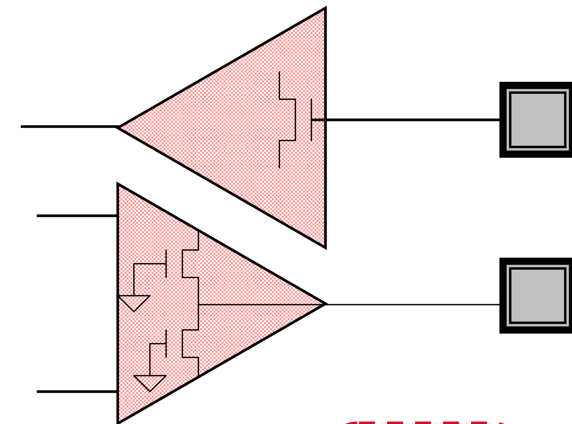
- pin completely isolated from on-chip circuitry



Practical isolation

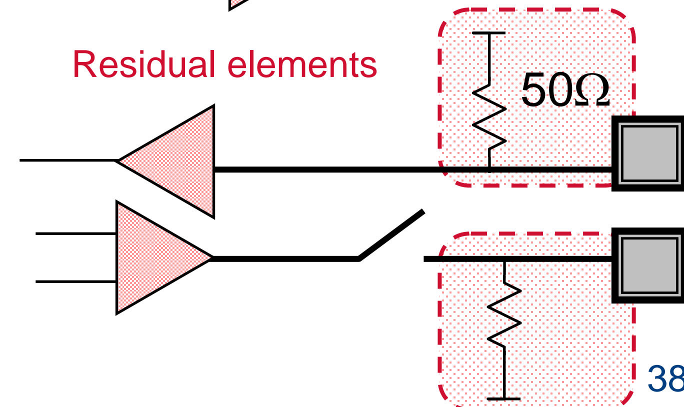
(high Z, minimal influence)

- outputs tri-stated
- inputs to transistor gates only, and function



Minimum isolation

(CD state, predictable influence)



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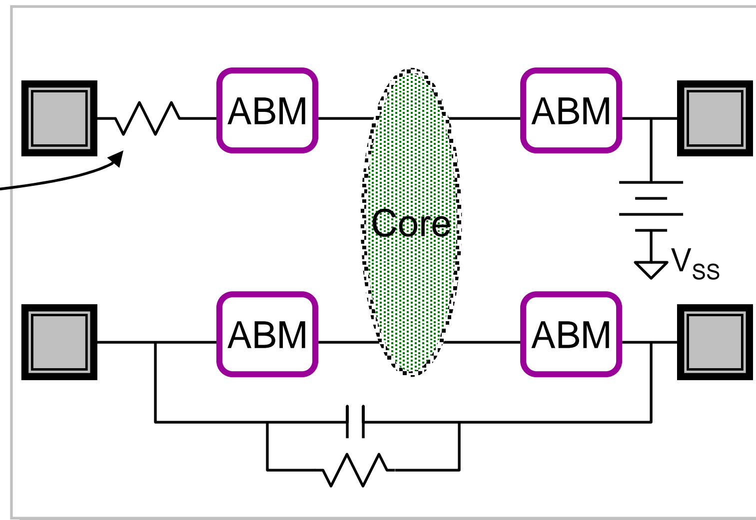
Residual Elements

- Circuitry permitted to connect to a pin in CD state:
  - can be modeled with linear passive elements (R, C, L) and *independent* DC voltage or current source
  - connects only to other analog or power pins, not digital or core
  - documented for IC user

Be especially careful to document any series resistance in the metalization, pad, bond wire, and lead frame



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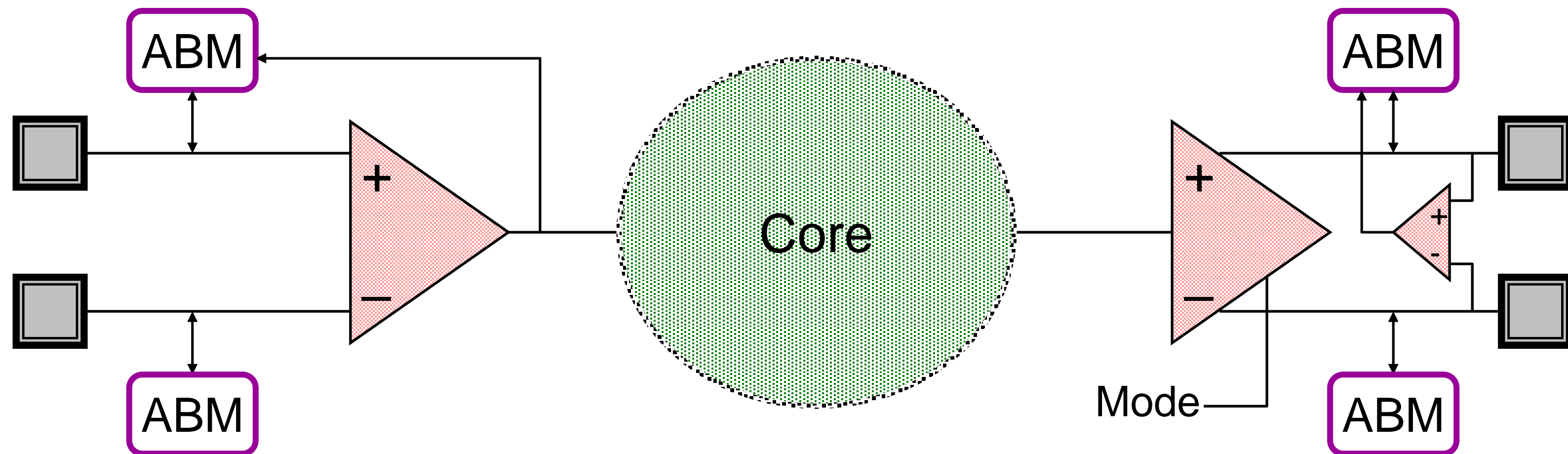
Differential function pins

- Each pin must have its own ABM
  - Inverting pins access AB1 and AB2, or optionally AB1N and AB2N
  - Non-inverting pins access AB1 and AB2
  - Non-inverting pin's ABM monitors comparison result
  - ABM +/– pair drives at least V_H/V_L, V_L/V_H, V_G/CD, CD/V_G, CD/CD



- Note: similar to 1149.6 + analog bus

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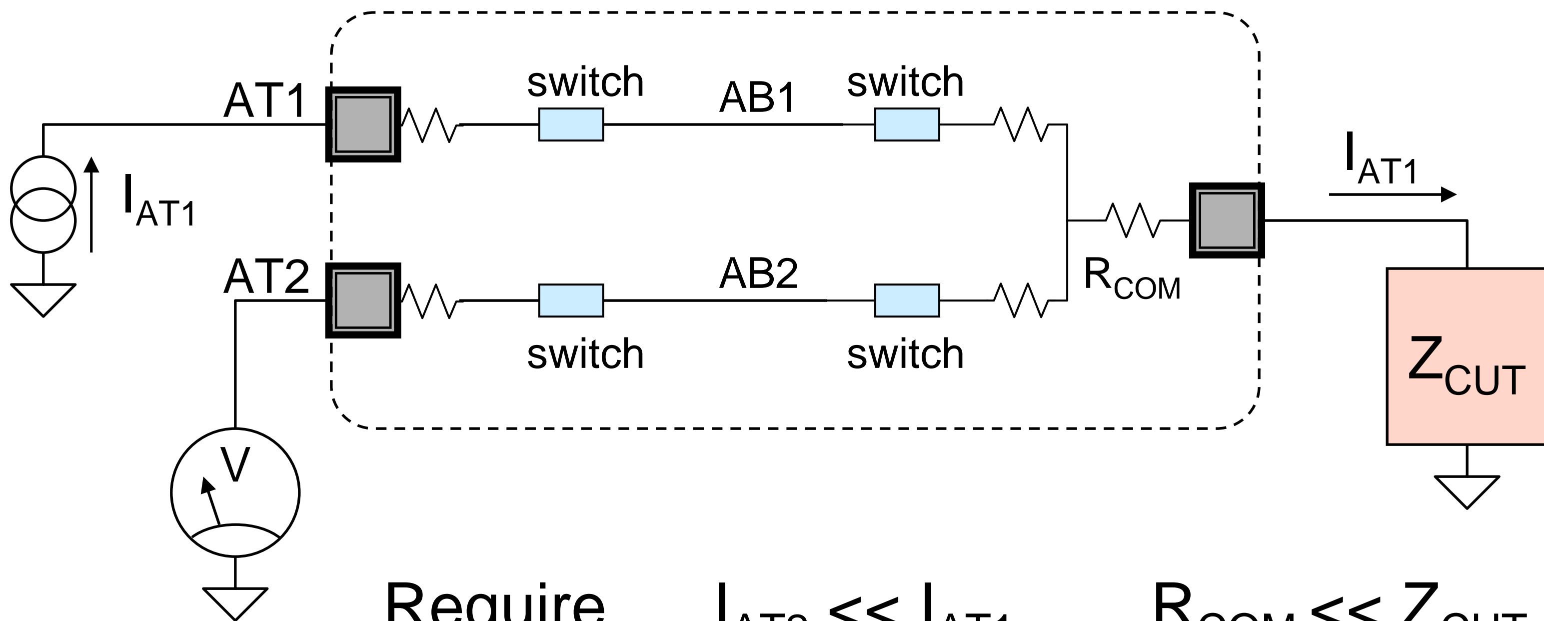
Measuring impedance

- Kelvin probe (or four probe) principle
  - Apply known current via AT1/AB1 path (<100 μA)
  - Measure voltage via AT2/AB2 path



Require $I_{AT2} << I_{AT1}$ (>10 MΩ) $R_{COM} << Z_{CUT}$ (<0.5 Ω)

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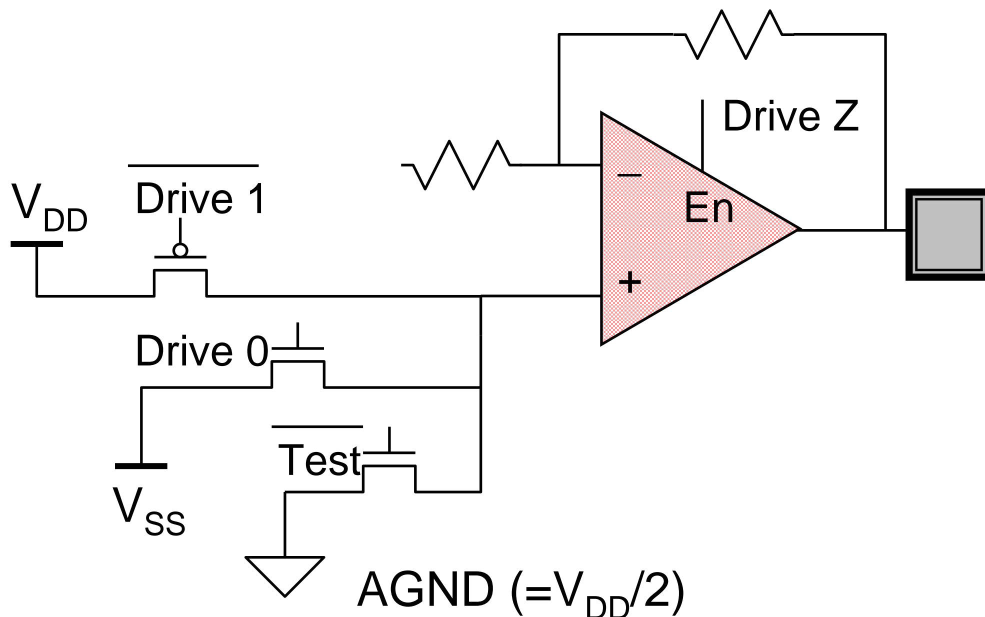
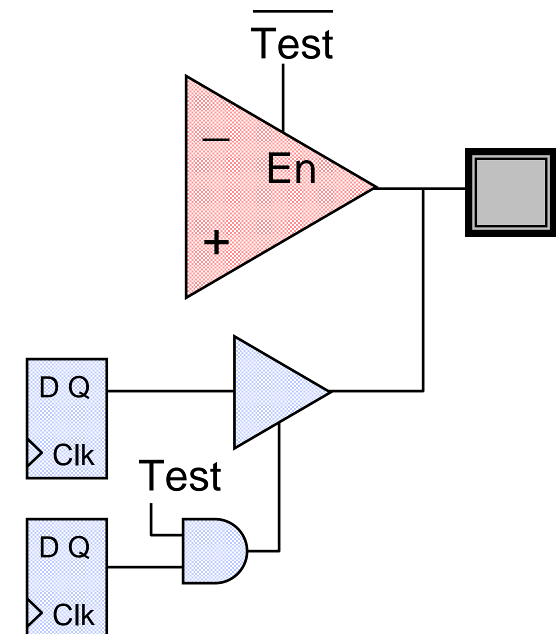
Performing tests equivalent to 1149.1

- Driving a logic 0 or logic 1
  - Force pin driver to drive its normal DC max. or min. voltage
  - Function driver best: high current, verifies driver connection to pin
  - Alternate (digital) driver may be used
  - *Objective:* largest practical voltage swing to allow fast, simple test





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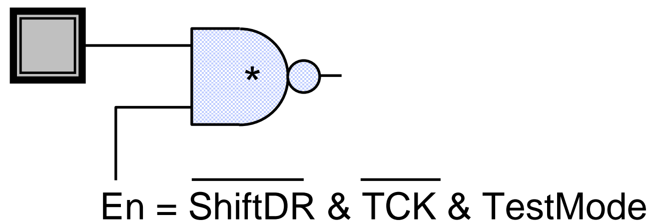
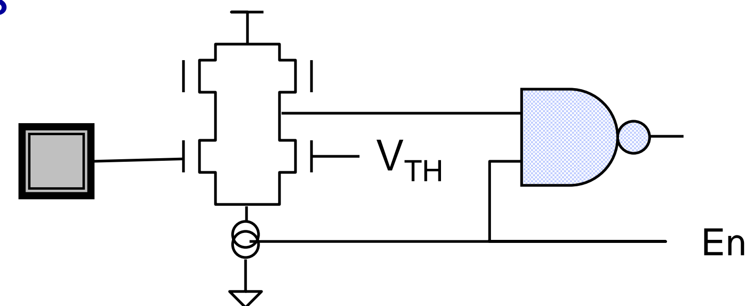
Performing tests equivalent to 1149.1

- Sensing a logic 0 or logic 1
  - Detect pin voltage relative to mid-rail threshold voltage, V_{TH}
  - V_{TH} is between 25% and 75% of (V_{MAX}–V_{MIN})
  - Value is captured as 0 or 1 in boundary scan register

Examples





Weak Nand (or Nor)
- minimal size
- small current (100 µA during Test)
- 1 ns response time

Minimum size comparator
- size of 3 Nands
- minimal current (µA)
- 50 ns response time

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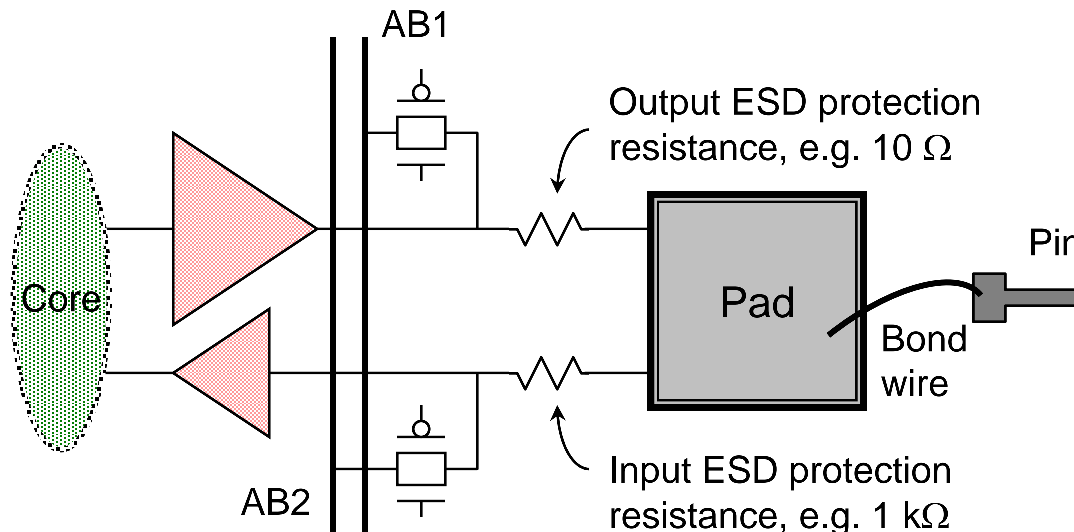
ABM, TBIC implementation in ASICs

- 1149.1 is implementable without help from ASIC supplier
  - All circuitry is digital, and placement not important
- Implementing1149.4 will typically require pad cell changes
  - Two, unbuffered, ESD-protected accesses to pads
  - Transmission gates that can be connected to pads (via ESD prot.)



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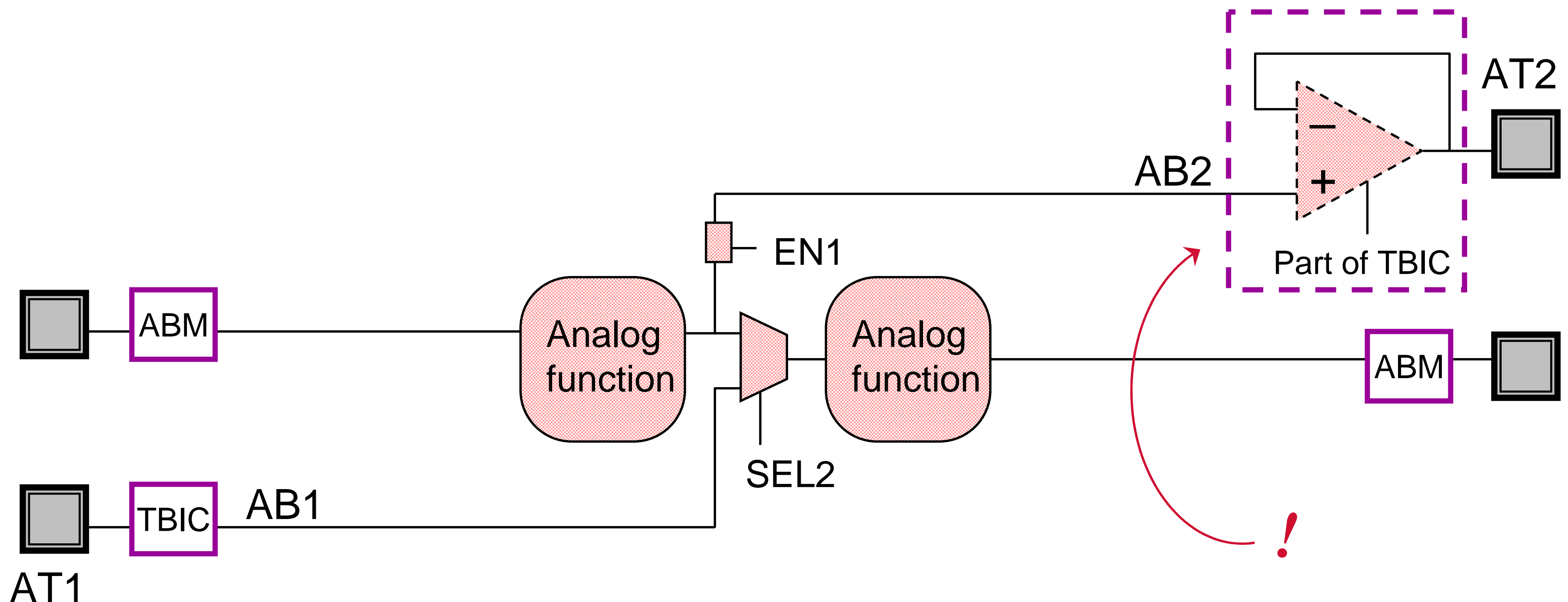
Accessing internal signals

- AB1 and AB2 can access core signals
- Access switches are enabled by dedicated scan bits
  - Enabled via private instruction, and not part of boundary register
  - Both AB2, AB1 would typically convey voltage, between V_{DD} / V_{SS}



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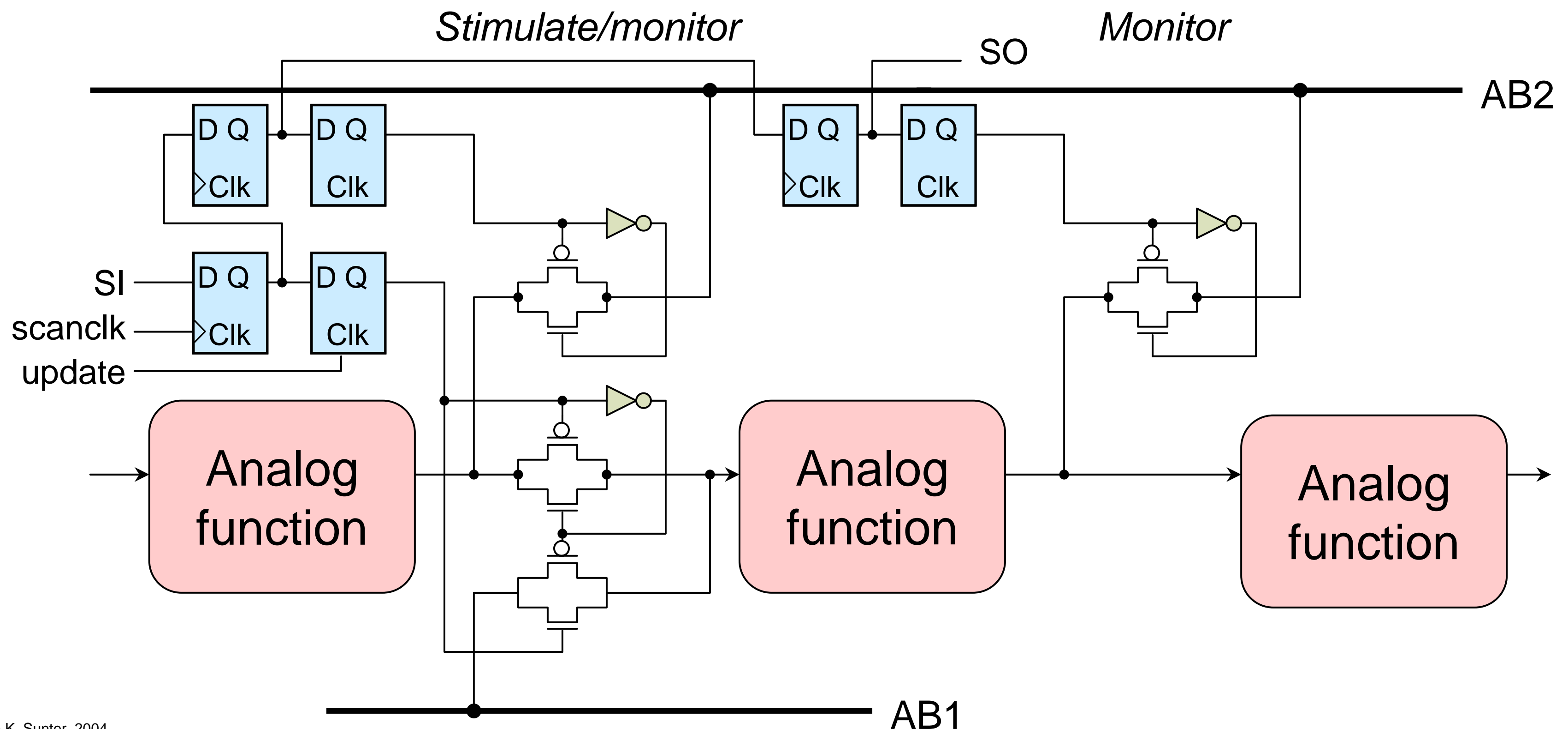
Internal analog scan

- Internal analog buses is a common design practice
  - See reference article by Andlauer & Vu, of Tality
- Limitations of only providing/accessing one signal
- Use update latches to avoid creating transients during scan



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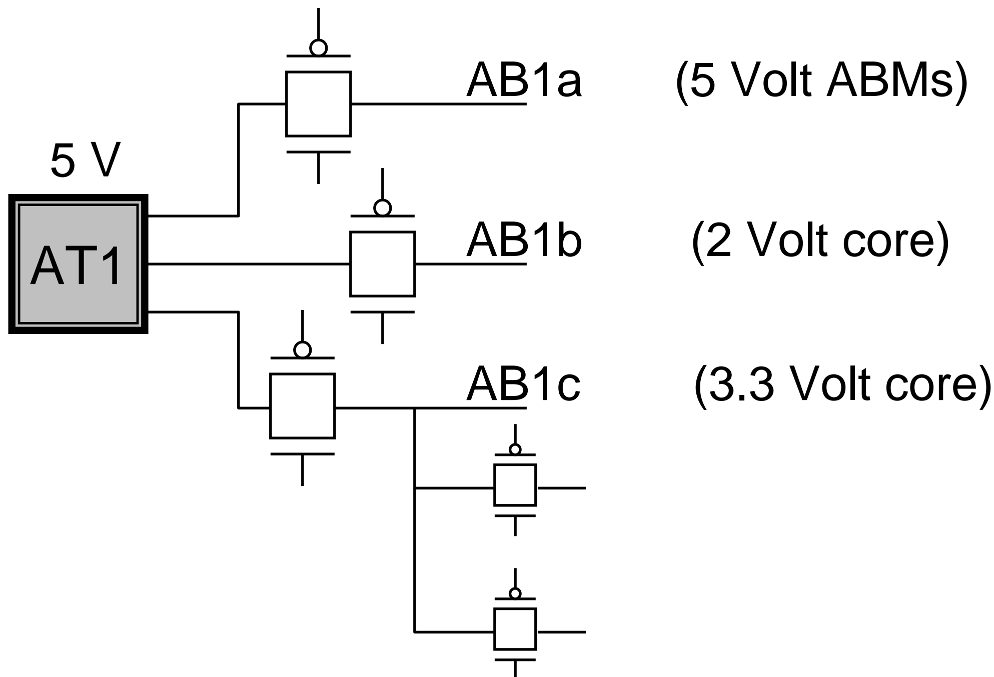
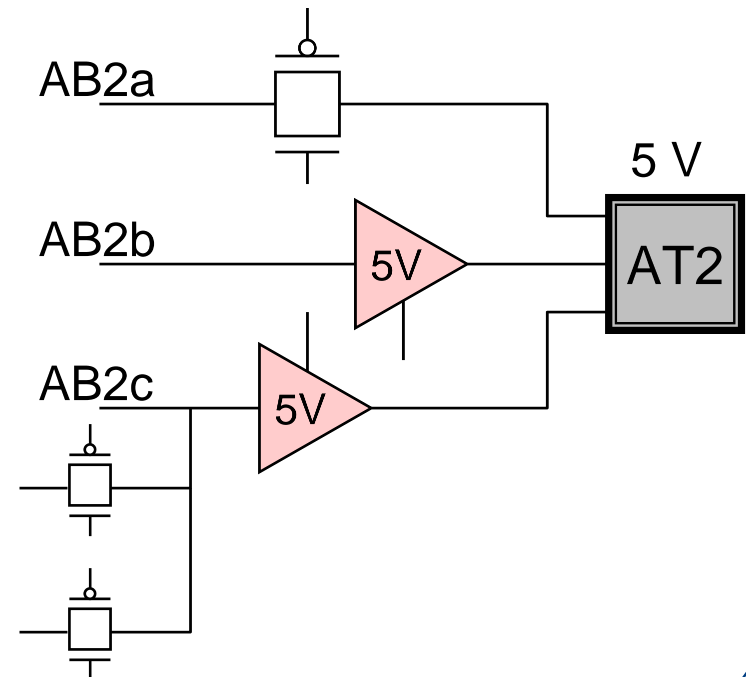
Multiple analog buses

- AB1 and AB2 may be partitioned into many buses
  - Allows multiple voltages, frequency ranges, etc.
  - Reduces bus capacitance ‘seen’ by accessed node
  - ~30 nodes per bus is practical upper limit for CMOS <0.25µm
    - may need hierarchical analog buses (more switches in series)





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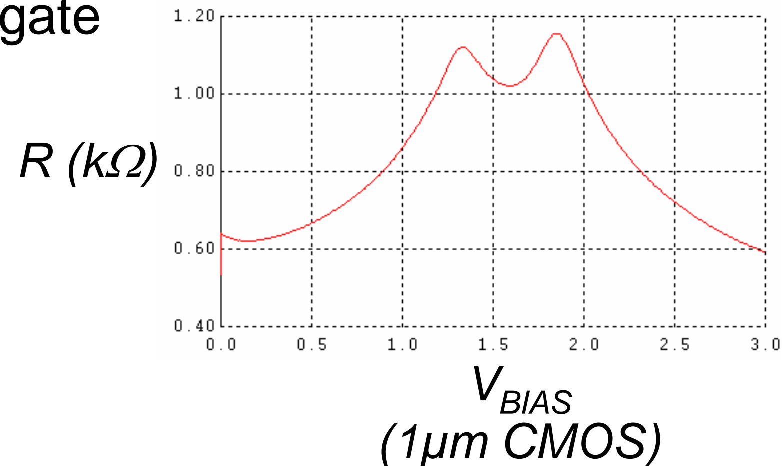
Testing HF analog paths

- Monitor average voltage
  - Switch resistance and bus capacitance are LPF
    (but note that transmission gate is non-linear R)



V_{BIAS}
(1µm CMOS)

- Under-sample
  - Example: under-sample 10 MHz signal
    to obtain 10 kHz signal on bus
  - See next 9 slides

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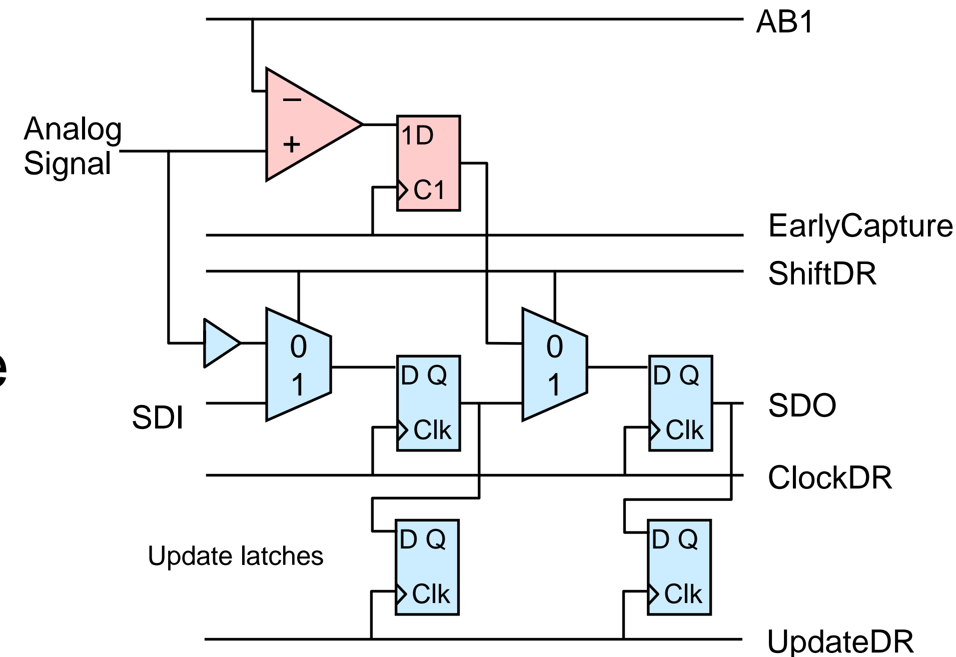
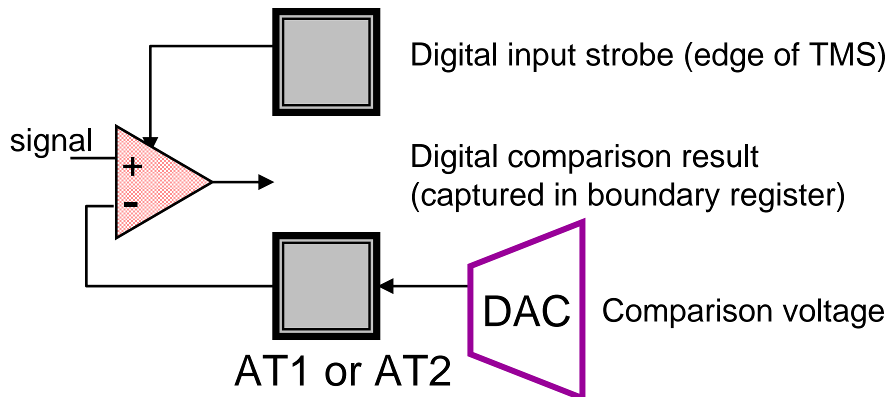
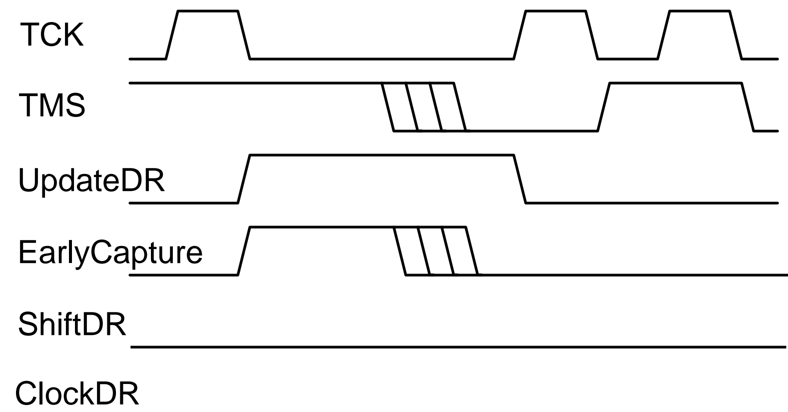
Early capture (K. Lofstrom, ITC'96)

- Analog bus provides DC reference for comparator
- Modified 1149.1 TMS signal used for strobe edge
- Perform binary search to determine signal voltage







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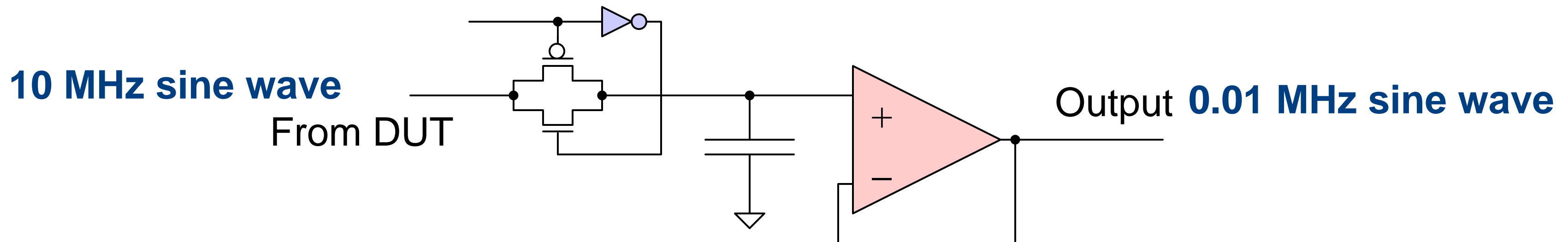
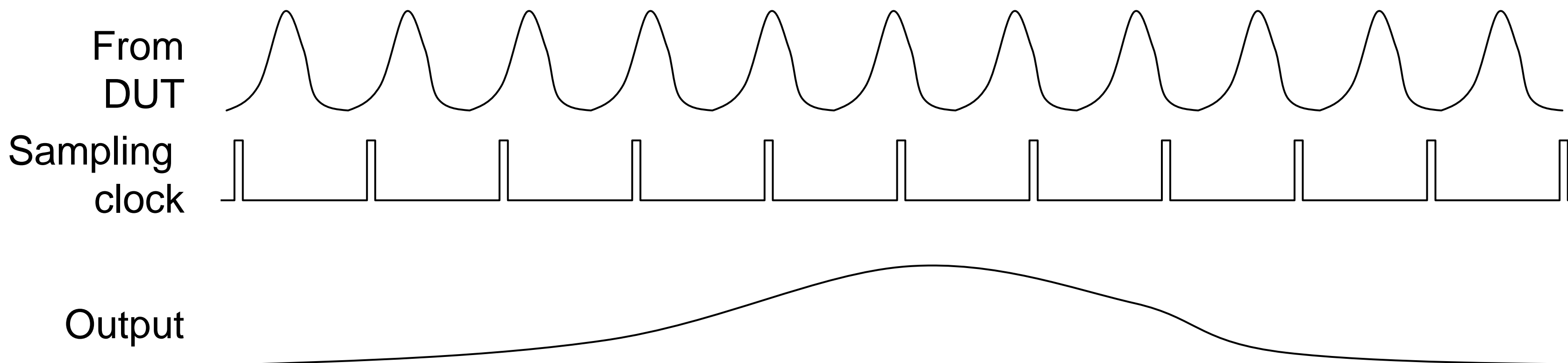
HF under-sampling

- An under-sampling technique (R.Mason, D&T Oct'99)
  - Transmission gate clocked by narrow digital pulse
  - On-chip storage capacitance and buffer
  - (Extension to this in ITC'03 paper 9.4)





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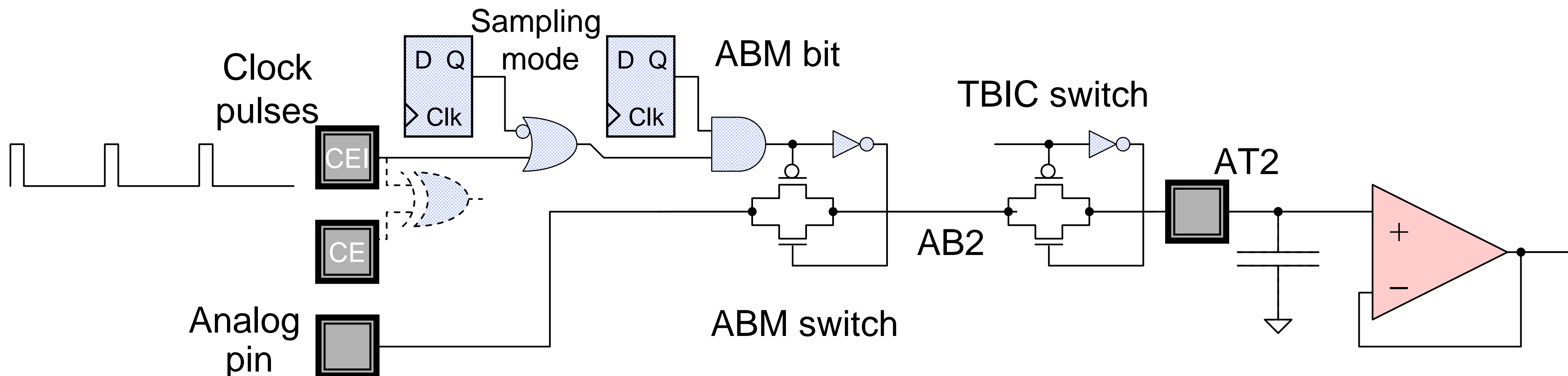
HF under-sampling via 1149.4 IC

- Improvements
  - Re-use ABM transmission gate
  - Exploit off-chip bus capacitance (as LPF)
  - Keep bus frequency <10 kHz



$$f_{BUS} = f_{CUT} - n\, f_{CLK}$$

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Limits to bandwidth

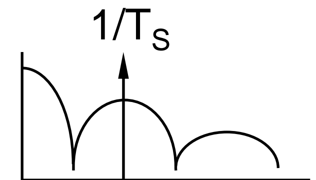
Example: f_{SAMPLE}= 10 MHz τ = 5 ns

C_{BUS} = 100 pF R_{SW} = 1kΩ

1. Pulse duty cycle <100% increases apparent R_{SW} that drives bus capacitance

   $f_{BUS-3dB} = \tau f_{SAMPLE} / 2\pi R_{SW} C_{BUS}$ $f_{BUS-3dB} \approx$ 80 kHz

2. Non-zero pulse width causes $(\sin x)/x$ roll-off



   Amplitude $\propto \sin(n\pi\tau/T_S) / (n\pi\tau/T_S)$

   $f_{SIGNAL-3dB} = 0.44 / \tau$ $f_{SIGNAL-3dB} \approx$ 88 MHz

(Sunter, ITC'01)

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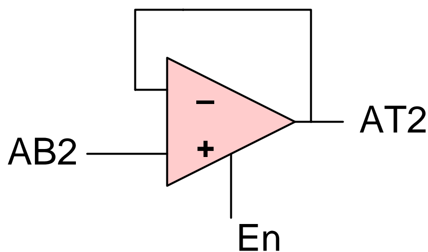
Analog bus buffers

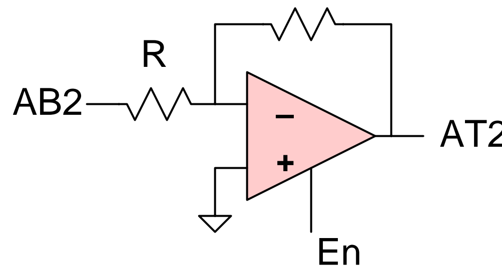
- How to provide a buffer between AB2 and AT2 ?
  - Rule: high input impedance (10 MΩ)
  - Rule: handle signals between V_{SS}–100mV and V_{DD}+100mV
  - Rule: <1% non-linearity

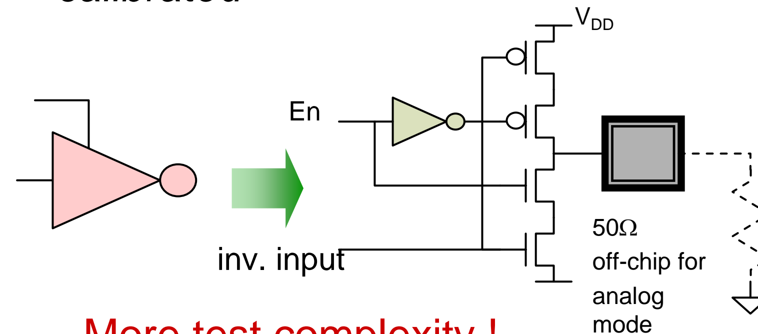
Full-swing op-amp
output range: V_{DD}–V_{SS}
→ *insufficient output range*

Inverting amplifier, gain <1
input/output range: OK
→ *typ. input impedance <1MΩ*

Standard CMOS digital 3-state inv
input/output range: OK
input impedance: OK
→ *non-linear, but can be calibrated*







OK for core signals, but not compliant for pin signals

$ area

More test complexity !

Conclusion: simple CMOS transmission gates may be best

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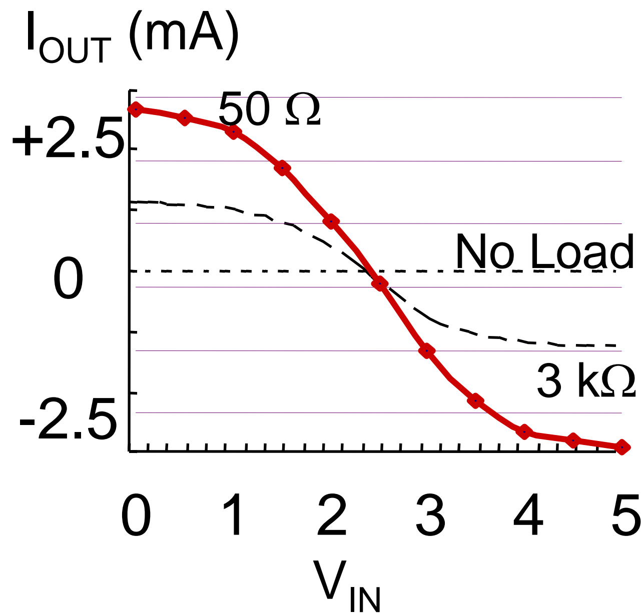
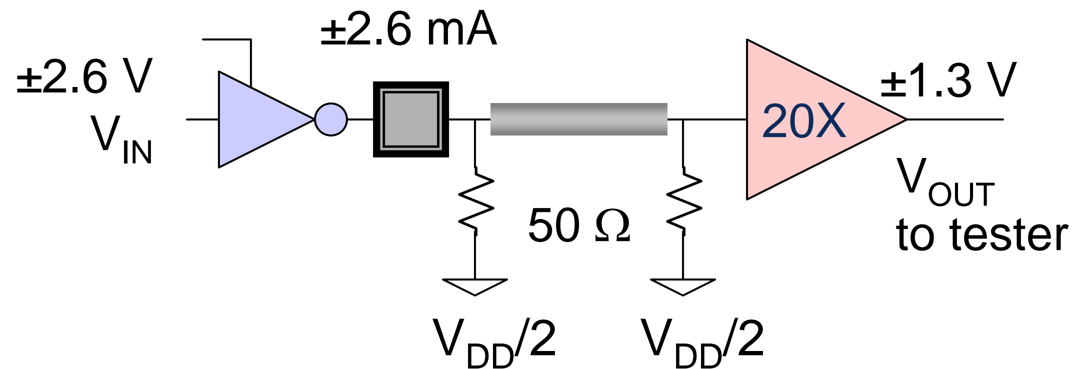
Monitoring HF signals directly

- Analog buffers monitor with less impact on CUT





- Bandwidth >30 MHz
- Calibrate non-linearity via TBIC, and use for analog signals
- Or use unloaded for digital output
- Buffers enabled by bits (one for AB1, one for AB2) in second data register

Sunter, VTS'96

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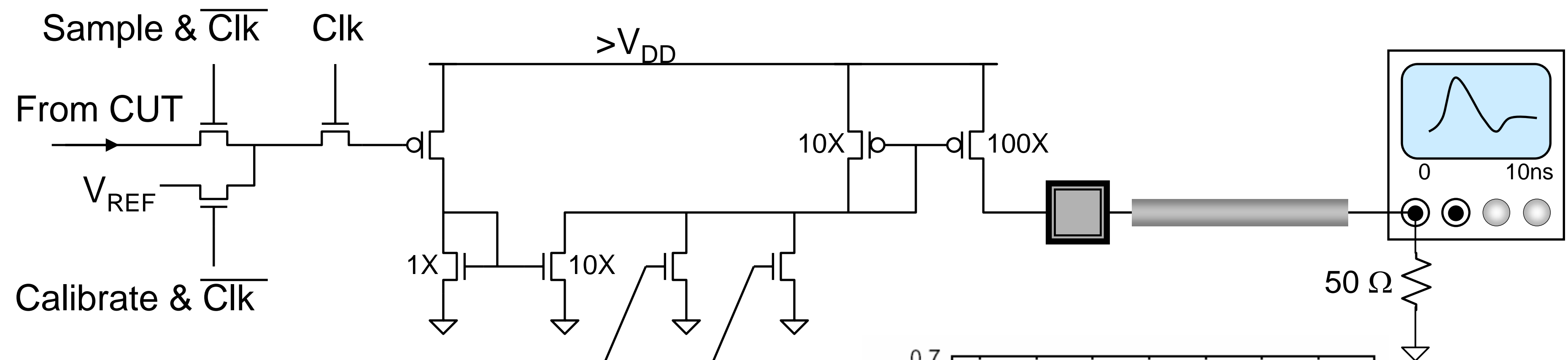
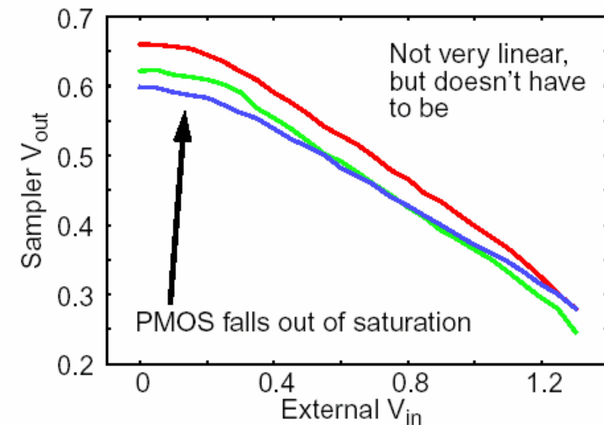
Under-sampling analog buffer

- Measured transfer function for strobed, 1 transistor monitor (near minimum size) with current mirrors for gain
- >1 GHz bandwidth





R.Ho *et al* (students of M.Horowitz), VLSI Design Symposium, 2001

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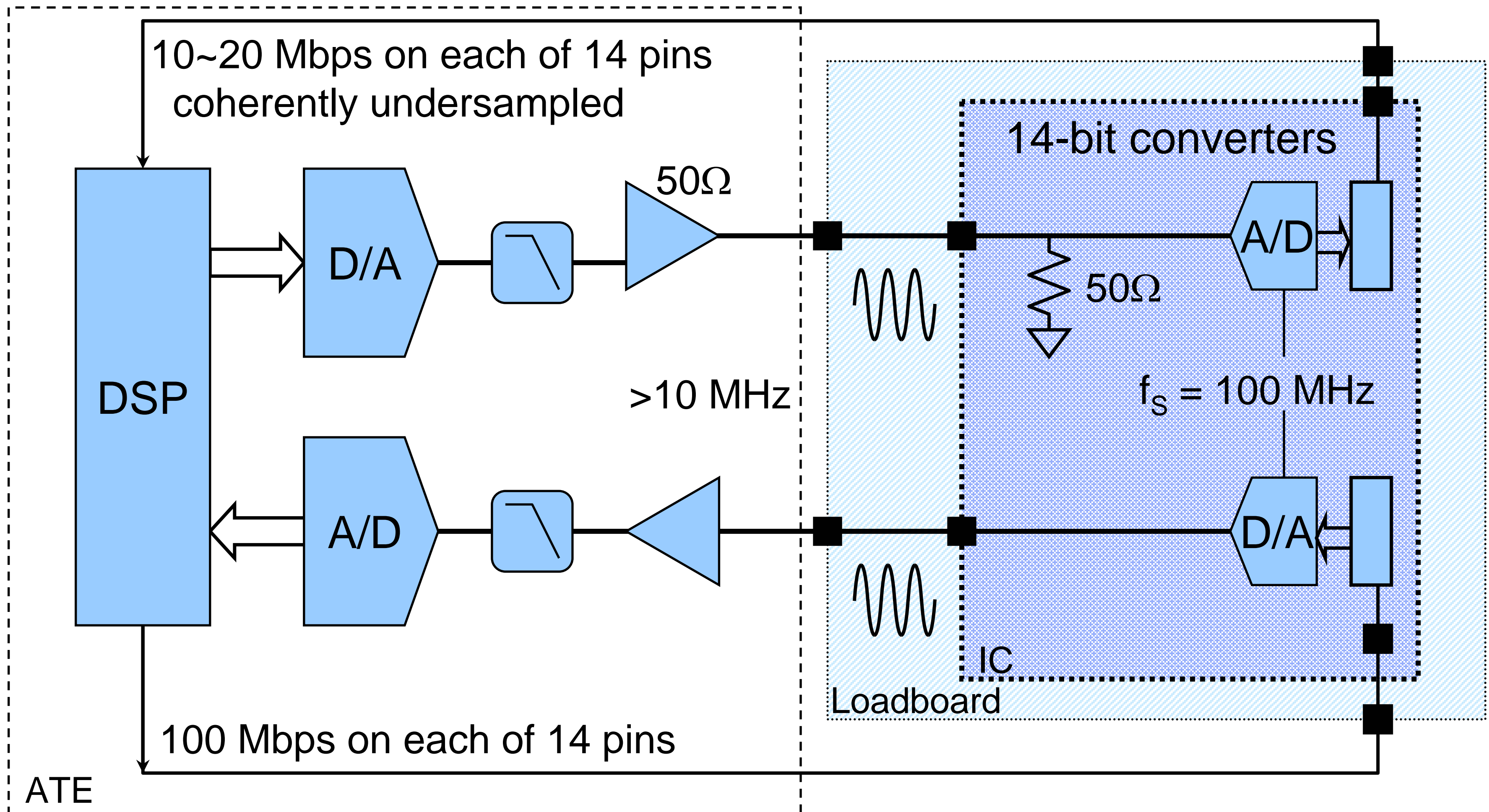
DFT for high-speed A/D and D/A ?



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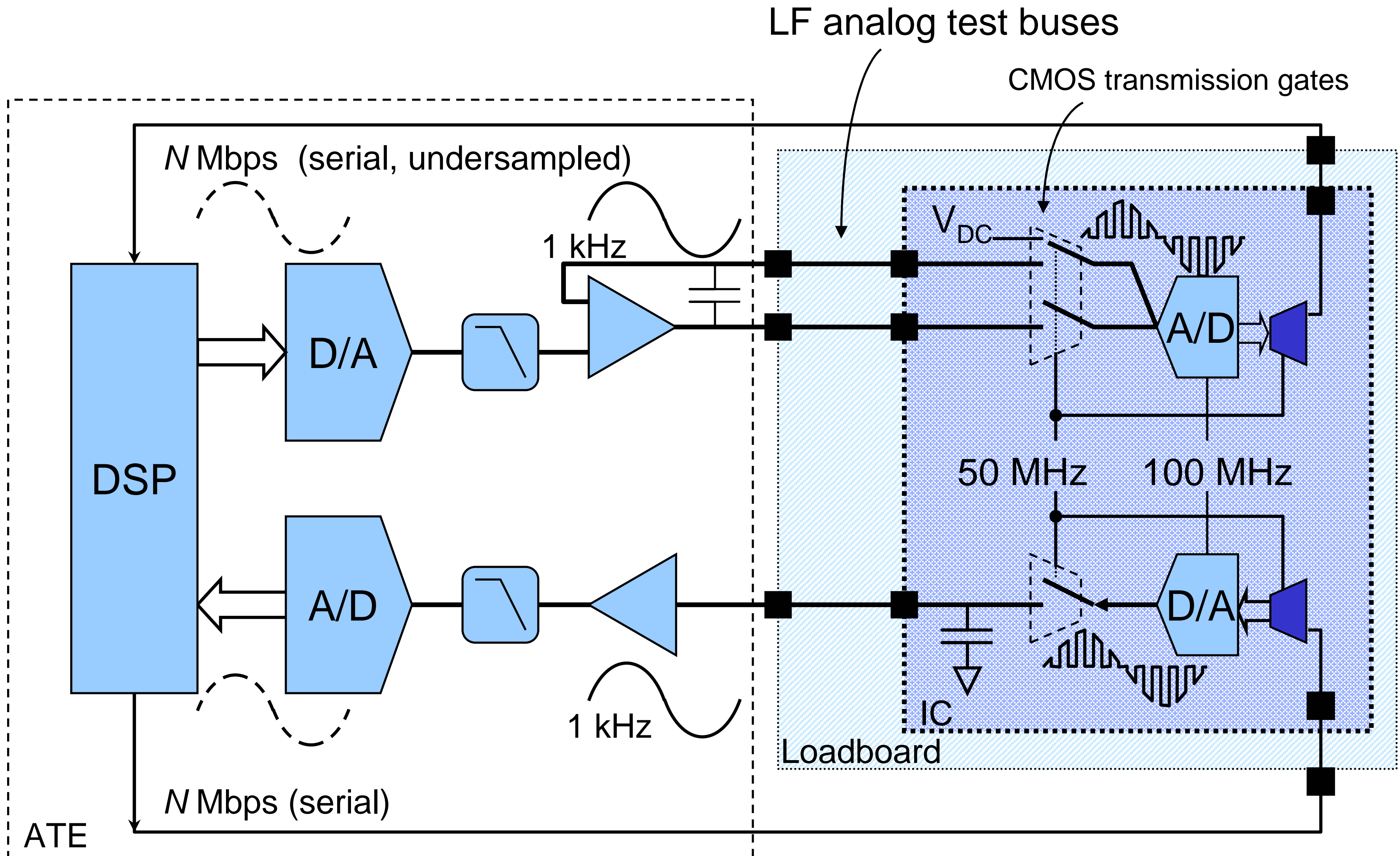
Synchronous under-sampling



Sunter, ITC'03

Shown single-ended. Typically, differential.

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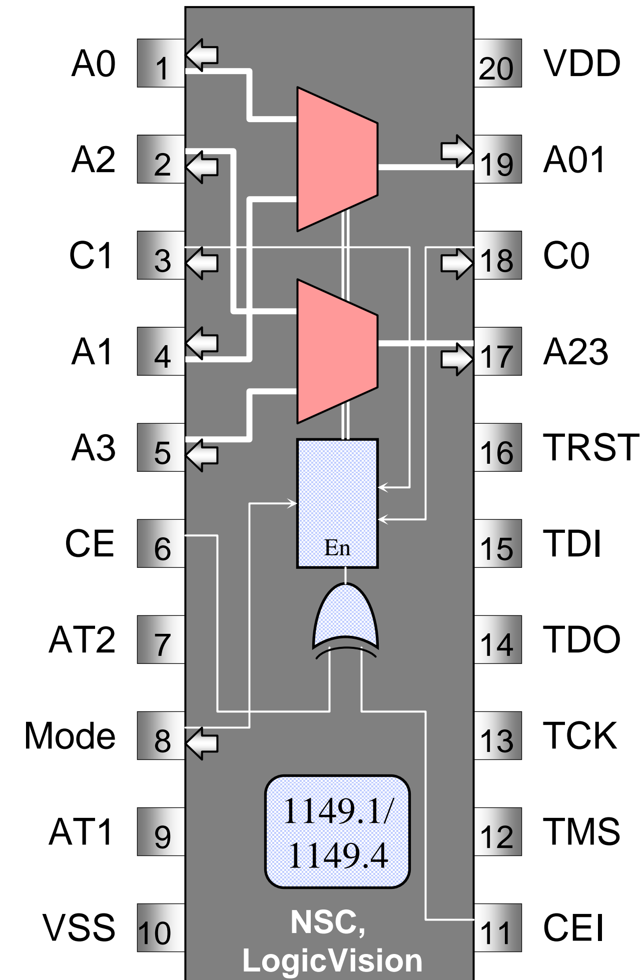
1149.4 ICs and lessons learned

- K.Lofstrom/IMP, 1996
  - Basic scheme works
  - Early Capture technique for HF signals
  - Switches in series with outputs impractical
  - T-switches important
- HP/Matsushita, 1998
  - ABM gate count is small
  - Layout of AB switch connections important
  - Switch non-linearity and leakage significant
- LogicVision/NationalSemi., 2000
  - TBIC buffer design is non-trivial
  - ABMs on digital pins can meet 1149.1 rules
  - R_{COM} <1Ω essential for accuracy
  - IC also known as D4access, and SCANSTA400



Pinout, showing internal circuit blocks and ABM-probed pins, when configured as a differential mux/demux.

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Summary

- Basic architecture is robust, simple
  - Suitable for logic synthesis
  - A few details are essential for accuracy
  - Almost no rules for internal access – innovation rules!
    - Analog bus access is a common design practice
- A variety of techniques for HF access
  - Under-sampling
  - V/I → I/V buffers, limited-swing voltage buses
- Experimental results published for 3 chips

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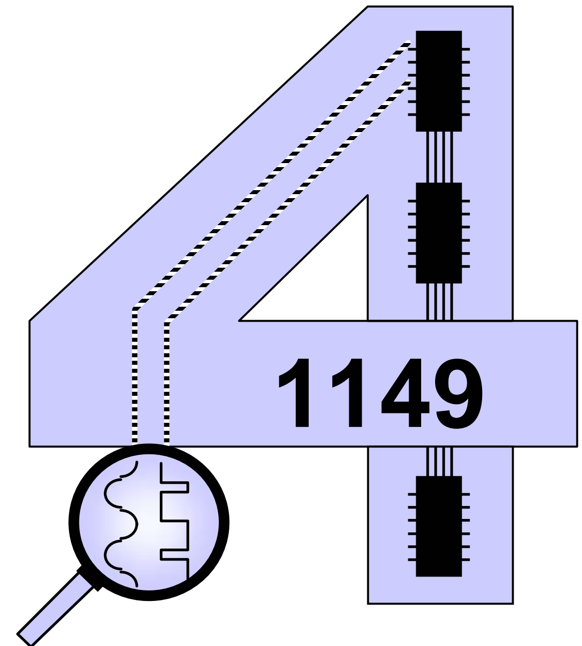
System Test Methods

Stephen Sunter



Outline

- Automating Test
  - BSDL
  - Analog BSDL
- “EXTESTing”
  - Pins: digital, analog, power
  - Board-level paths: digital, differential
  - Using commercially available software
  - Tester within a laptop PC
- References
- Conclusions

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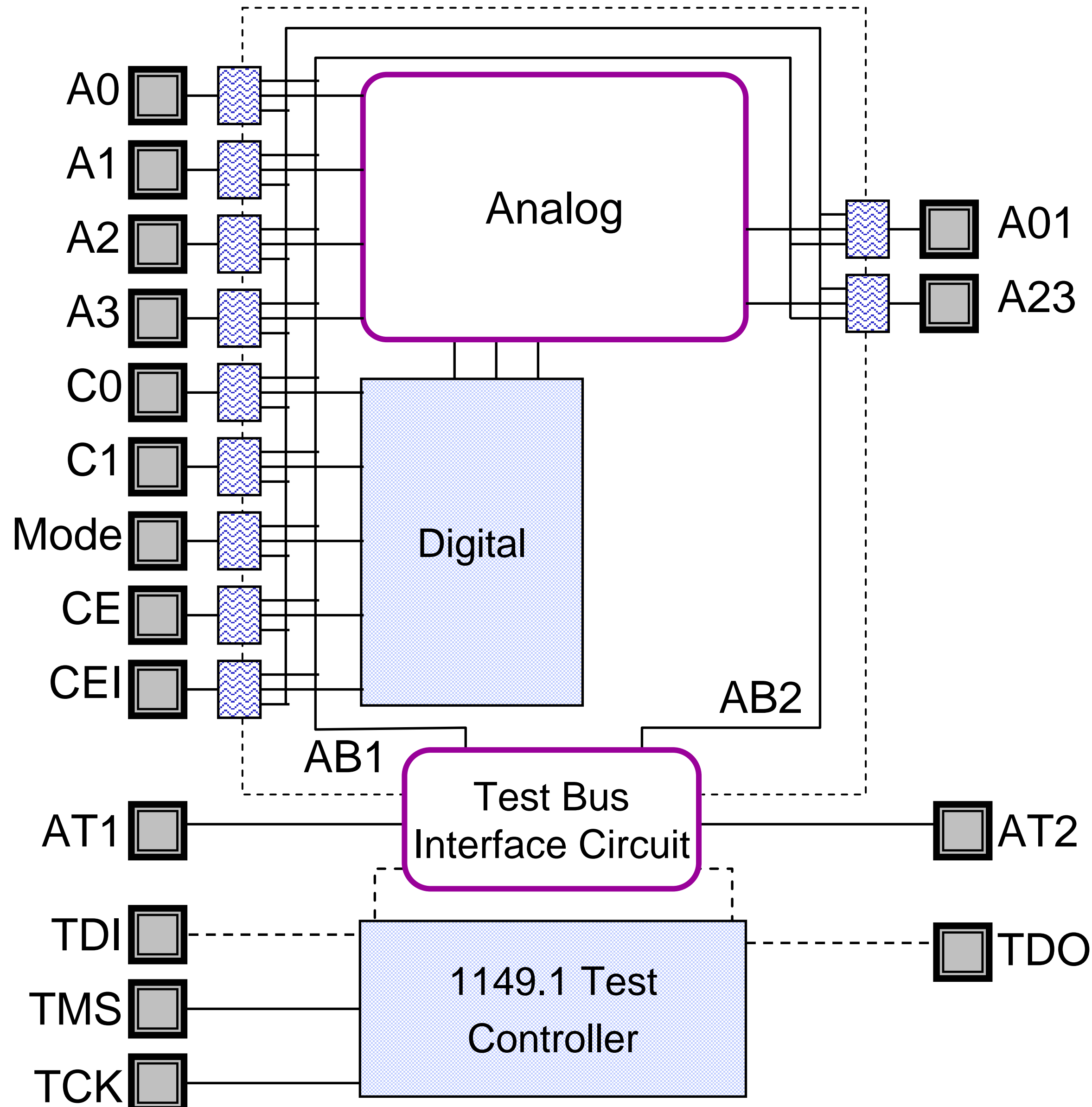
Example 1149.4 IC, with 11 ABMs



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ABM/TBIC description file

```
package MY_BSCAN_CELLS is
    use STD_1149_1_1994.all;       -- comments
      constant LV_B2: CELL_INFO;   -- ABM B2  control bit
      constant LV_B1: CELL_INFO;   -- ABM B1  control bit
      constant LV_D:  CELL_INFO;   -- ABM D   data bit, for analog pins, or for TBIC D1,D2
      constant LV_C:  CELL_INFO;   -- ABM C   control bit, for analog pins
      constant LV_CA: CELL_INFO;   -- TBIC CA control bit
      constant LV_CO: CELL_INFO;   -- TBIC CO control bit
end MY_BSCAN_CELLS;

package body MY_BSCAN_CELLS is
    use STD_1149_1_1994.all;
    constant LV_B2: CELL_INFO :=
       ((INTERNAL, EXTEST,  UPD), (INTERNAL, SAMPLE, ZERO));
    constant LV_B1: CELL_INFO :=
       ((INTERNAL, EXTEST,  UPD), (INTERNAL, SAMPLE, ZERO));
    constant LV_D:  CELL_INFO :=
       ((BIDIR_IN, EXTEST,   PI), (BIDIR_OUT, EXTEST,  PO),
        (BIDIR_IN, SAMPLE,   PI), (BIDIR_OUT, SAMPLE,  PO));
    constant LV_C:  CELL_INFO :=
       ((CONTROL, EXTEST,  UPD),  (CONTROL, SAMPLE,   PI));
    constant LV_CA:  CELL_INFO :=
       ((INTERNAL, EXTEST,   X),  (INTERNAL, SAMPLE, ONE));
    constant LV_CO:  CELL_INFO :=
       ((CONTROL, EXTEST,    X),  (CONTROL, SAMPLE,  PI));
end MY_BSCAN_CELLS;
```

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Example BSDL file (top half)

```
-- comment
entity my_chip is
    generic (PHYSICAL_PIN_MAP : string := "DEFAULT_PACKAGE_NAME");
     port (
        CE                    : inout    bit;
        ...
        AT1                   : inout    bit;
        AT2                   : inout    bit;
        TCK                   : in       bit;
        ...
        TDO                   : out      bit;
        VDD                   : linkage  bit;
        VSS                   : linkage  bit);
    use STD_1149_1_1994.all;
    use MY_BSCAN_CELLS.all;
    attribute COMPONENT_CONFORMANCE of top: entity is "STD_1149_1_1993";
    attribute PIN_MAP of top: entity is PHYSICAL_PIN_MAP;
    constant DEFAULT_PACKAGE_NAME: PIN_MAP_STRING :=
    "A0     : 1    , " &
    "A2     : 2    , " &
    ...
    "VDD    : 20     " ;
   attribute TAP_SCAN_RESET of TRST     : signal is true;
   ...
   attribute TAP_SCAN_CLOCK of TCK      : signal is (2.0e+07, BOTH);
   attribute INSTRUCTION_LENGTH of top: entity is 20;
-- continued on next slide
```

All 1149.4 pins are “inout”

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Example BSDL file (bottom half)

```
attribute INSTRUCTION_OPCODE of top: entity is
   "BYPASS    (11111111111111111111)," &
   "EXTEST    (00000000000000000000,"  &
             " 11111111111111101000)," &
   "SAMPLE    (01111111111111111000)," &
   "PROBE     (11111111111111111000)," &   -- 1149.4 instruction
   "HIGHZ     (01111111111111001111)," &
   "CLAMP     (11111111111111101111) " ;
 --
attribute INSTRUCTION_CAPTURE of top: entity is "xxxxxxxxxxxxxxxxxx01";
attribute REGISTER_ACCESS of top: entity is  "BOUNDARY   (PROBE)" ;
attribute BOUNDARY_LENGTH of top: entity is 48;
attribute BOUNDARY_REGISTER of top: entity is
 -- This end is closest to TDO
 -- num  cell         port     function       safe     [ccell disval  rslt]
 "    0  (LV_B1       , *      , internal     , 0   )                        ,"&
 "    1  (LV_B2       , *      , internal     , 0   )                        ,"&
 "    2  (LV_C        , *      , control      , 0   )                        ,"&
 "    3  (LV_D        , A3     , bidir        , 0    ,   2     , 0     , Z    ),"&
 ...
 "   20  (LV_CA       , *      , internal     , 0   )                        ,"&
 "   21  (LV_CO       , *      , control      , 0   )                        ,"&
 "   22  (LV_D        , AT1    , bidir        , 0    ,  21     , 0     , Z    ),"&
 "   23  (LV_D        , AT2    , bidir        , 0    ,  21     , 0     , Z    ),"&
 ...
 "   47  (LV_D        , A0     , bidir        , 0    ,  46     , 0     , Z    )";
end my_chip;
```

Selects boundary scan register

Selects bypass register

Mode2

Mode1-inv

Safe value *Control cell* *Disable value* *Disable result*

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EXTEST switch settings

ABM

D	C	(AB1) B1	(AB2) B2	(analog access switches)
0	0	0/1	0/1	CD (tristate)
1	0	0/1	0/1	Drive “ground” out
data	1	0/1	0/1	Drive data out (1149.1)

TBIC

Ca	Co	(AT1) D1	(AT2) D2	
0	0	0/1	0/1	Connect AT1→AB1 or AB2→AT2
0	1	data	data	Drive data out (1149.1)
1	0	1	0	Calibrate: AT1→AB1→AT2
1	0	0	1	Calibrate: AT1→AB2→AT2

[all other settings are undefined]

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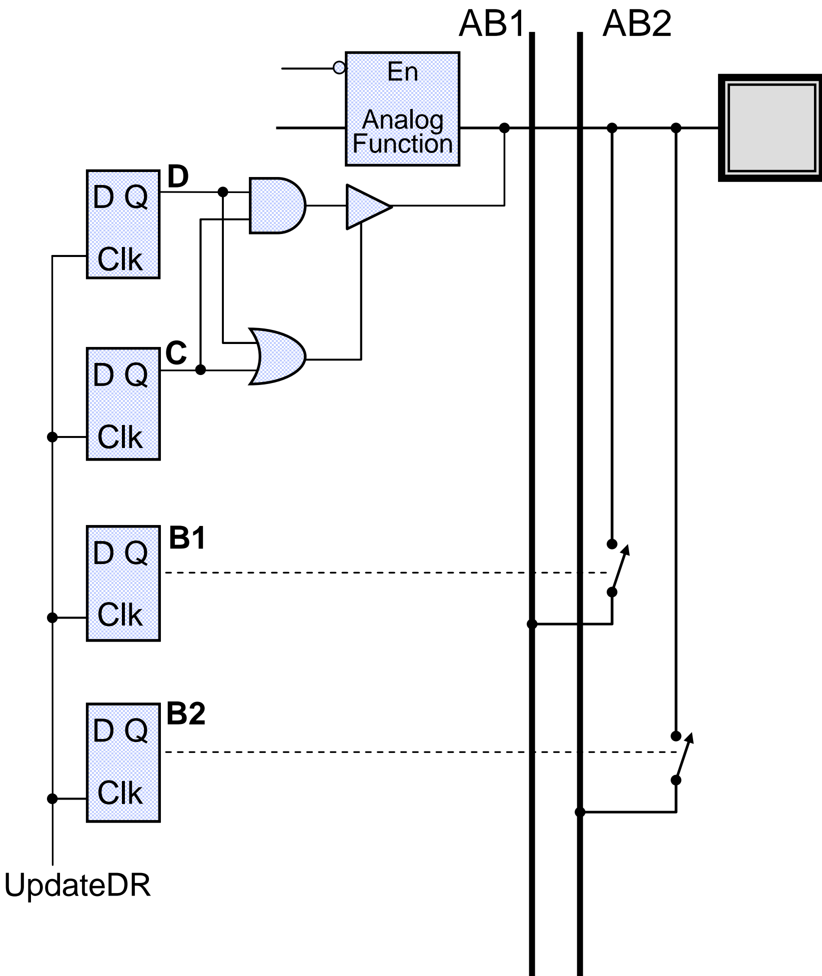
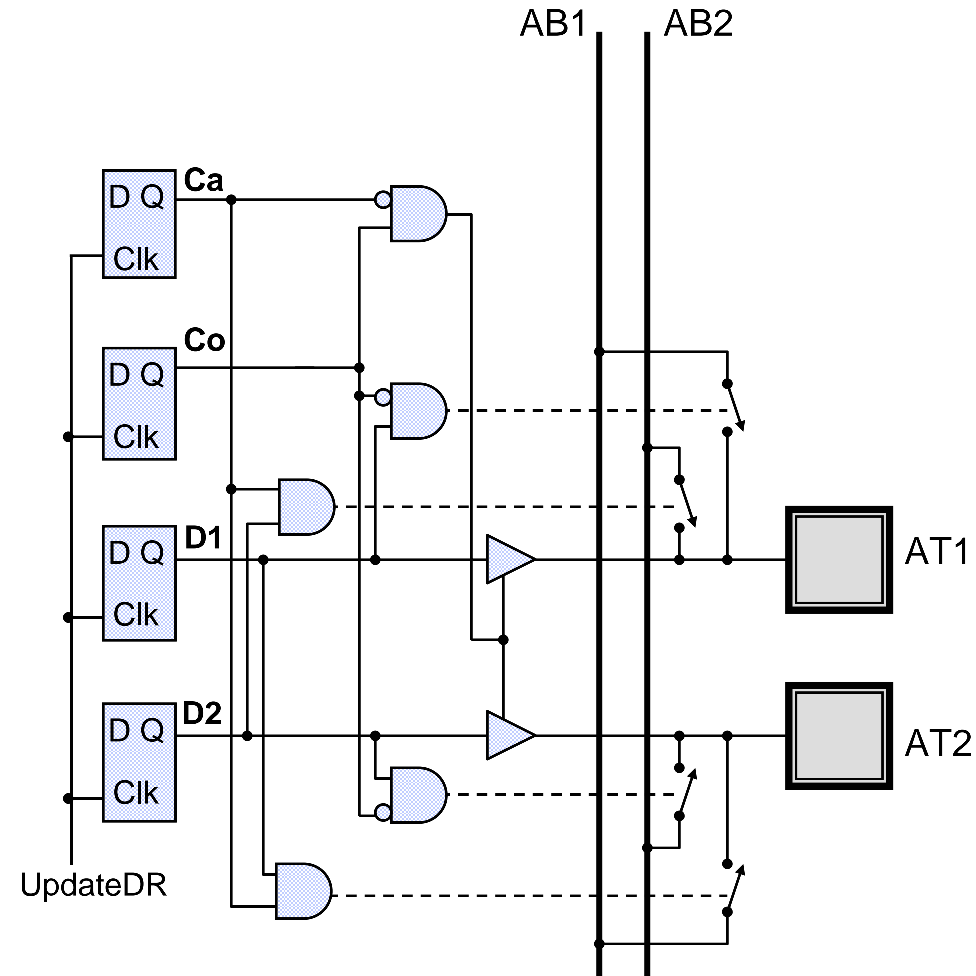
EXTEST switch connections





For simplicity, Mode1 and Mode2 connections are not shown.

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Summary of Instructions

Instruction	Requirement	TDI – TDO path	Mode of function pins
BYPASS	Mandatory	Direct (bypass)	Function
SAMPLE/ PRELOAD	Mandatory	Bscan register	Function
EXTEST	Mandatory	Bscan register	Test
PROBE	Mandatory	Bscan register	Function
INTEST	Optional	Bscan register	Test – digital pins Function – analog pins, clock pins
CLAMP	Optional	Direct (bypass)	Test
HIGHZ	Optional	Direct (bypass)	High-Z – digital pins CD-state – analog pins
RUNBIST	Optional	Bscan register	Test – output pins Function – input pins
IDCODE	Optional	Ident. register	Function
USERCODE	Optional	Ident. register	Function

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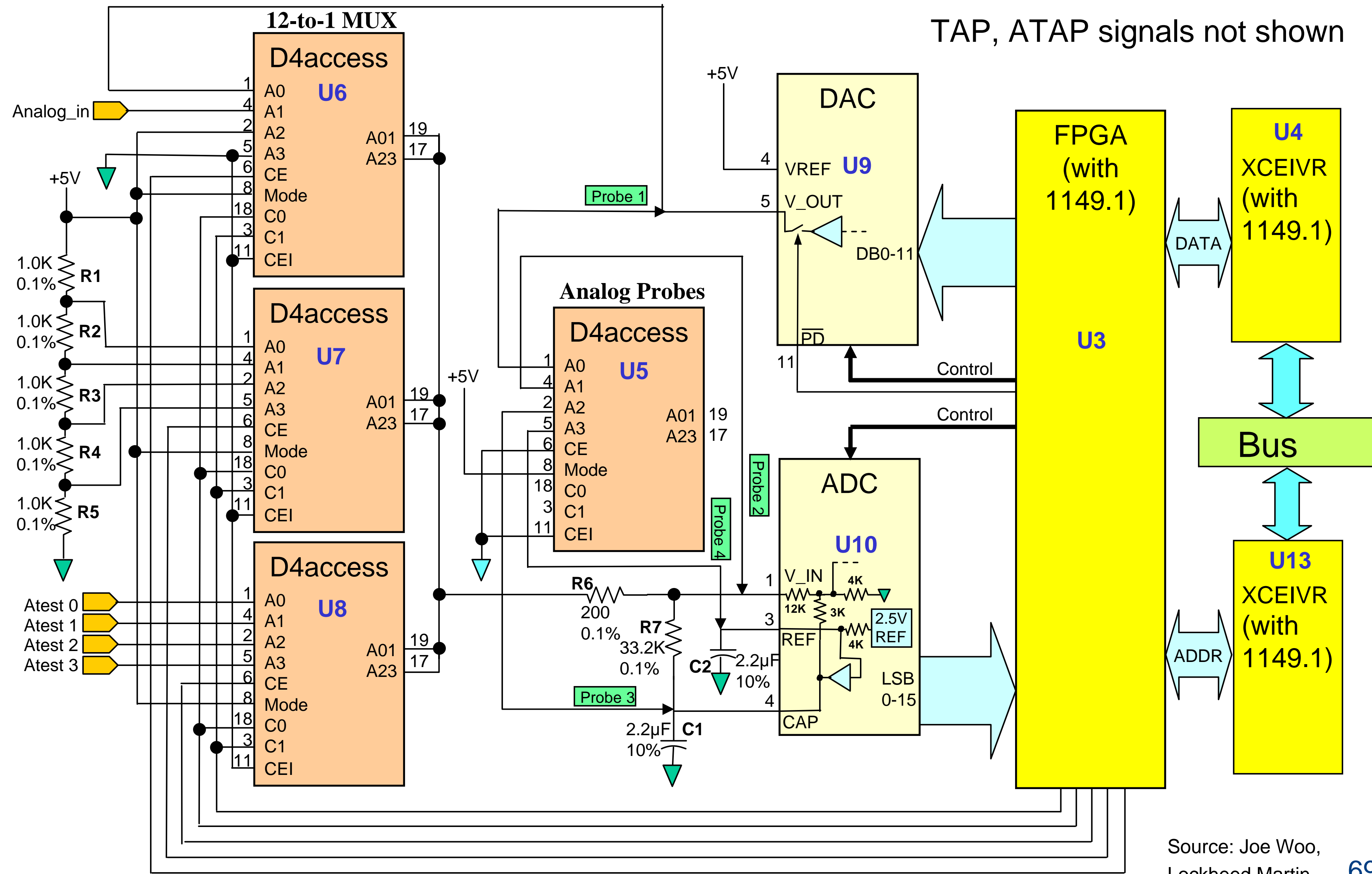
Example circuit board



Source: Joe Woo, Lockheed Martin

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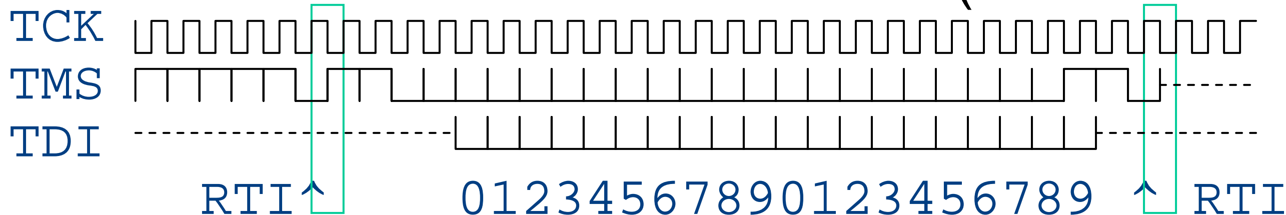
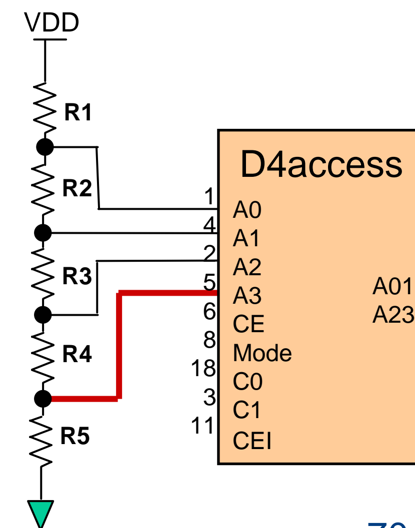
Measuring DC impedance at A3 pin

- Load EXTEST instruction (*refer to BSDL, next slide*)



- Load boundary scan register
  - Enable TBIC switches: AT1→AB1, AB2→AT2
  - Enable A3 ABM switches: AB1→pin, pin→AB2
  - Disable all other switches



- Apply 100 µA to A3, via AT1
- Measure V_{A3}, via AT2

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Example BSDL file (again)

```
attribute INSTRUCTION_OPCODE of top: entity is
   "BYPASS   (11111111111111111111)," &
   "EXTEST   (00000000000000000000,"  &
            " 11111111111111101000)," &
   "SAMPLE   (01111111111111111000)," &
   "PROBE    (11111111111111111000)," &  -- 1149.4 instruction
   "HIGHZ    (01111111111111001111)," &
   "CLAMP    (11111111111111101111) " ;
 --           ^Mode2          ^Mode1-inv
attribute INSTRUCTION_CAPTURE of top: entity is "xxxxxxxxxxxxxxxxxx01";
attribute REGISTER_ACCESS of top: entity is  "BOUNDARY   (PROBE)" ;
attribute BOUNDARY_LENGTH of top: entity is 48;
attribute BOUNDARY_REGISTER of top: entity is
 -- This end is closest to TDO
 -- num  cell         port     function      safe     [ccell disval  rslt]
 "   0   (LV_B1      , *      , internal     , 0    )                        ,"&
 "   1   (LV_B2      , *      , internal     , 0    )                        ,"&
 "   2   (LV_C       , *      , control      , 0    )                        ,"&
 "   3   (LV_D       , A3     , bidir        , 0    ,     2      , 0      , Z    ),"&
 ...
 "  20   (LV_CA      , *      , internal     , 0    )                        ,"&
 "  21   (LV_CO      , *      , control      , 0    )                        ,"&
 "  22   (LV_D       , AT1    , bidir        , 0    ,    21      , 0      , Z    ),"&
 "  23   (LV_D       , AT2    , bidir        , 0    ,    21      , 0      , Z    ),"&
 ...
 "  47   (LV_D       , A0     , bidir        , 0    ,    46      , 0      , Z    )";
end my_chip;
```

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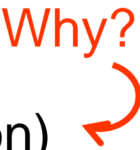
Testing digital pins

- Output drive
  - Via boundary scan, drive pin to logic 0 (or 1)
  - Apply ≥100 µA via AT1; measure V_{PIN} via AT2

- Pull-up impedance, or pin+wire capacitance
  - Via boundary scan, drive pin to CD (don't use *HIGHZ* instruction)
  - Apply 10 µA (AC for capacitance) via AT1; measure V_{PIN} via AT2



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Testing power pins

- Power rail voltage
  - Via boundary scan, drive unloaded pin to logic 0 (V_{SS}) or 1 (V_{DD}) or monitor a pin connected to another V_{DD} access (see U6-A2 pin)
  - Measure V_{PIN} via AT2
    (transmission gates can monitor voltages 100 mV beyond rails)
  - millivolt changes in power rail voltage may indicate faults

- How to detect rail glitches with excess amplitude?
  - Power rail quality test – next 3 slides

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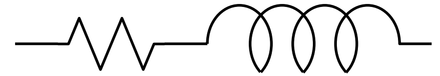
Power rail impedance



- R, L of power rail is a key source of delay faults
  - Output signal skew
  - Propagation delay
- How much impedance is too much?
  - When it causes delay faults (or changes of state)
- Power pins typically not tested
  - ICs can have 100’s, boards may have 1000’s
  - Proposals for testing: X-ray, measure IR_{DC} on-chip

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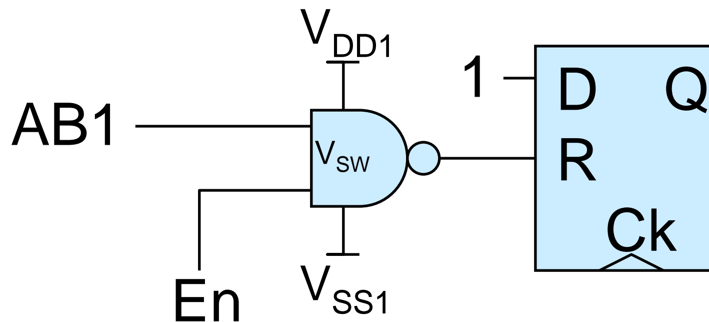
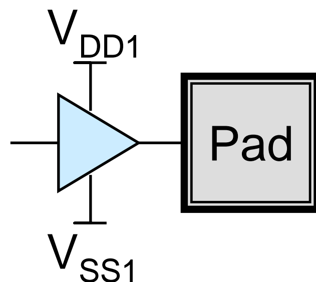
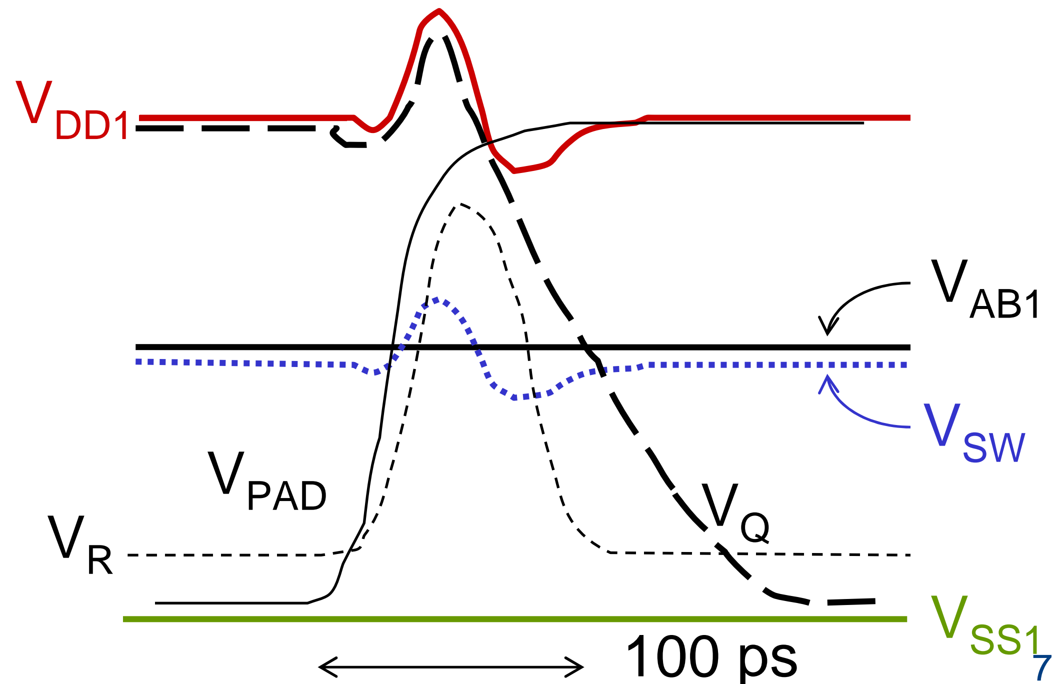
Power rail test

- Test whether logic gate's switching point changed
  - Via AT1, apply V_{SW} +100 mV to flip-flop's reset
  - Via boundary scan, cause nearby output pin transition
  - Flip-flop changes state if power rail glitch >200 mV







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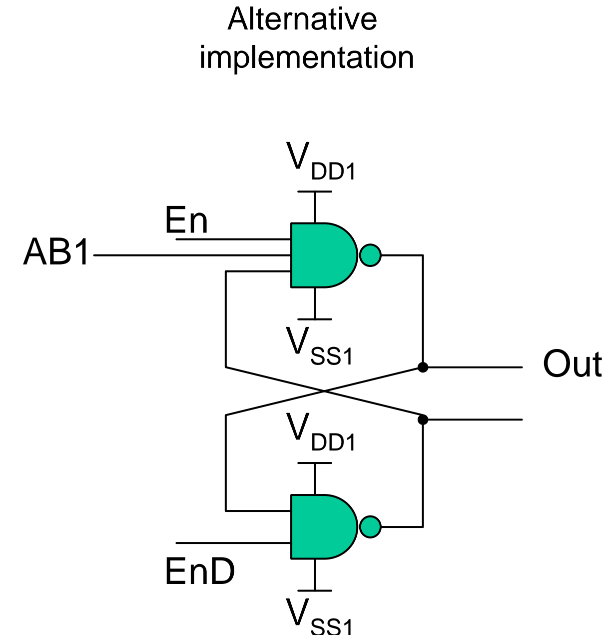
Power rail test - discussion

- Benefits
  - Programmable sensitivity via AB1 voltage
  - Use active-low (or high) reset to detect positive (or negative) glitches
  - Minimal IC area, and scannable



- Limitations
  - Must measure V_{SW} for each die, or flip-flop
  - Analog bus noise – capacitance to quiet signals helps, so noise margin needs to be characterized

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Testing analog pins

- Measuring input and output impedance
  - Similar to digital, except use *PROBE* or *INTEST* so that analog pin voltage is mid-range
    (and driven by function driver)
- Analog stimulus for core input
  - Limited drive via analog bus
  - Use AT1 to force stimulus voltage
  - Use AT2 to monitor stimulus voltage at input pin
    (and adjust stimulus as necessary)
    then to monitor response at output pin

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Testing digital paths

- Example: digital control signals
  - FPGA digital output has 1149.1
  - D4access digital input has 1149.4
  - Use conventional 1149.1 test software

    (BSDL: B1, B2 bits declared INTERNAL, safe value = 0)

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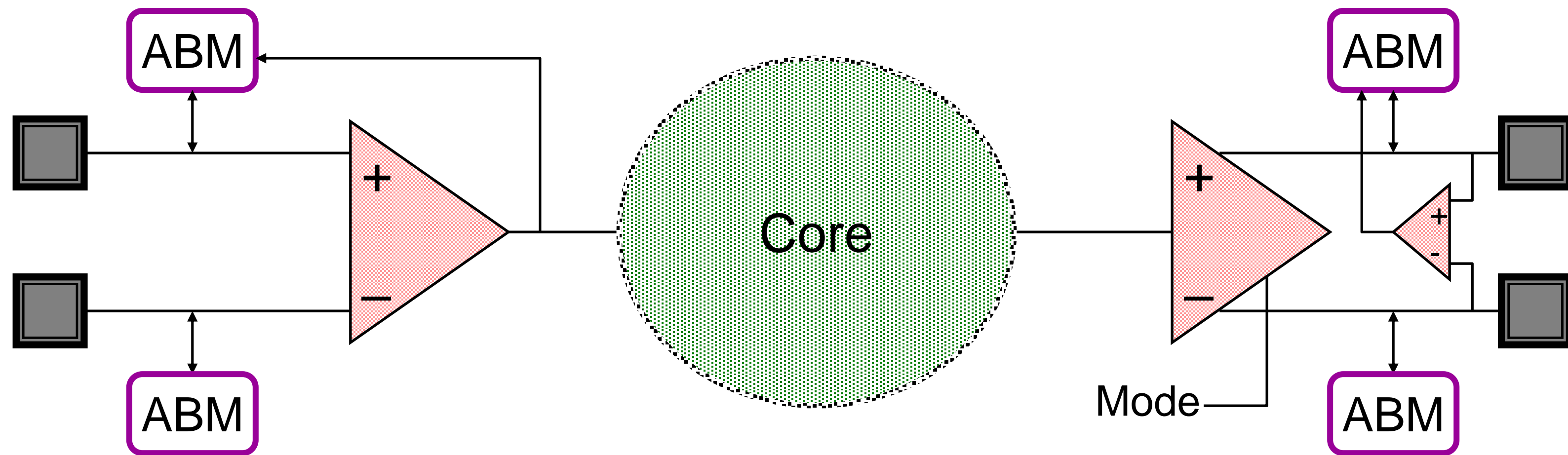
Differential interconnect testing

- (Discussed earlier)
- 8 boundary scan bits per pair



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Differential interconnect tests

- A noise tolerant test for each DC-coupled pair
  - Drive logic 1 (then logic 0)
    - Measure received average pin voltages, via AT1 (–) and AT2 (+) simultaneously!
    - Capture received logic values (may ignore single-ended values)
- A noise tolerant test for each AC-coupled pair
  - Transmitter and receiver in CD state (e.g., high Z)
    - Drive sine wave at transmitter pin via AT1
    - Measure response at each receiver pin via AT2

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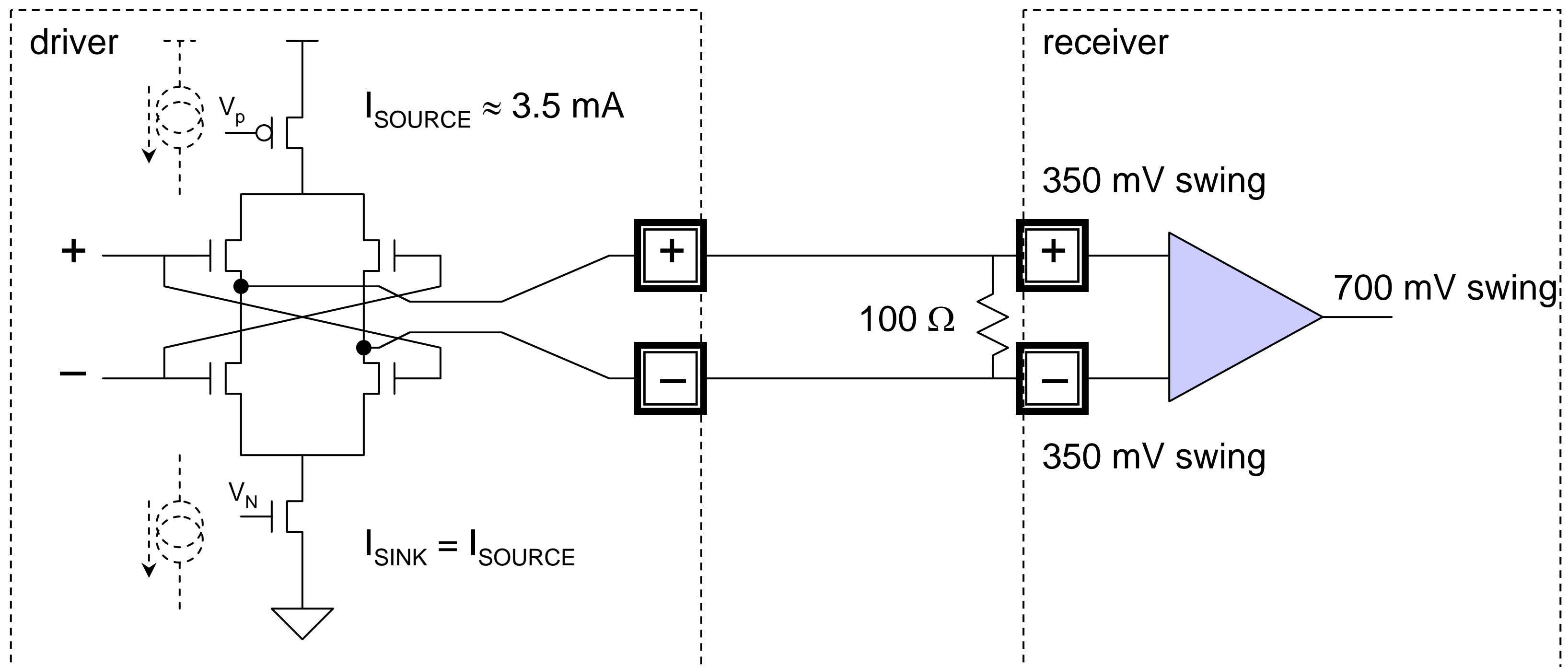
LVDS example

- Correct termination resistance essential >100 Mb/s
- Testable by 1149.4, but not by 1149.1



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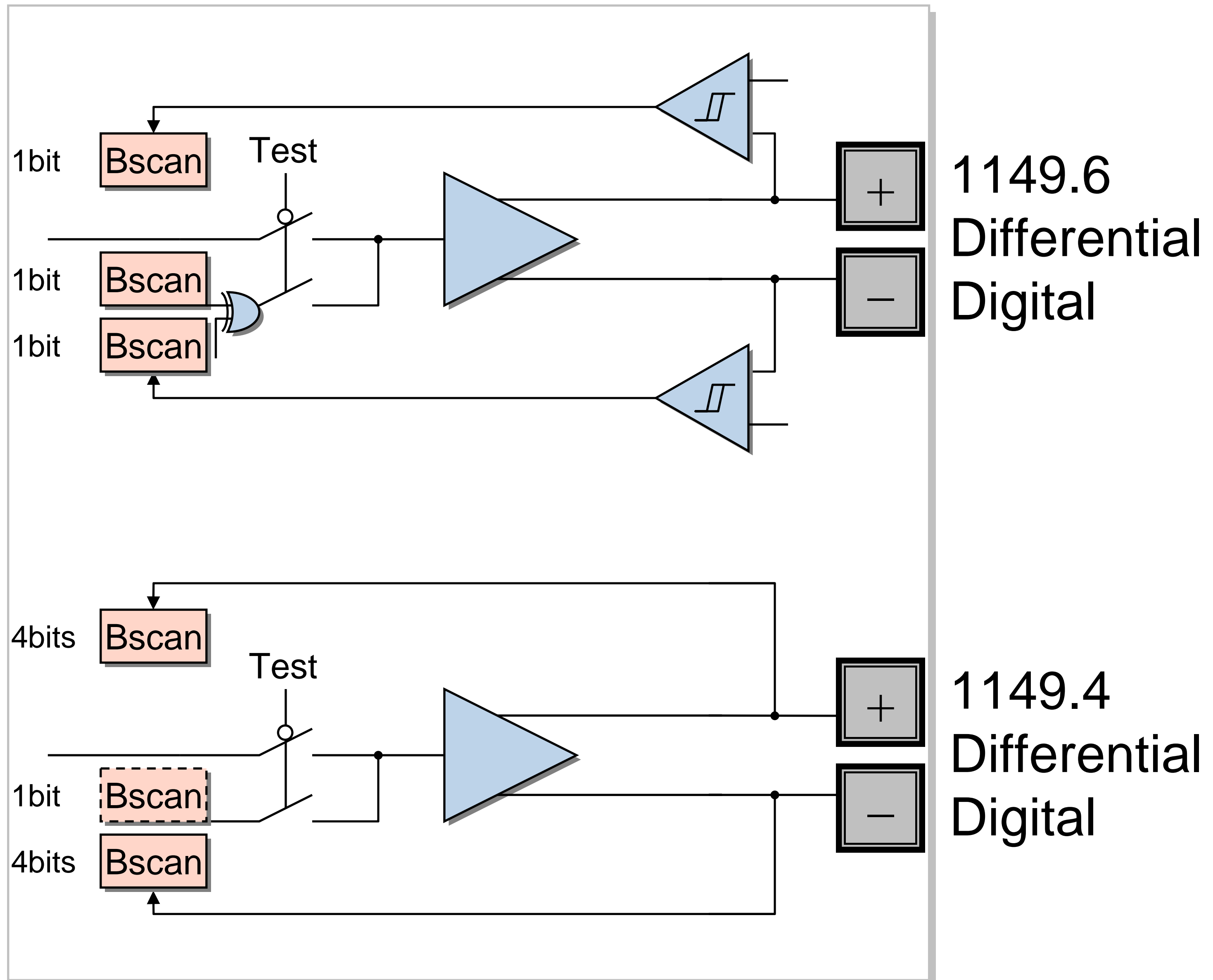
Pin test circuitry overview



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Differential interconnect testing

- 1149.4 vs. 1149.6

1149.4	1149.6
Measures R,C	Only pass/fail
+2 analog pins	No extra pins
Analog stimulus	Digital stimulus (1149.1)
Crummy switches	Hysteretic comparator, RC (?)
+2 crummy comparators/pair	+2~4 accurate comparators/pair
+ one instruction	+ two instructions
1~10 ms/pin = 1~10 sec/1K pins (but whole board test time >3 min.)	~1 ms for all pins in parallel

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Probing wires via the Internet

- 1149.1-based test via the Internet is available from many vendors (ASSET, Corellis, Intellitech, JTAG, ...)
- 1149.4 facilitates diagnosis of almost-failures or parametric failures
- Demonstrated by Lockheed Martin using representative demonstration board, off-the-shelf software, and LogicVision/NationalSemi. chip

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Example of 1149.4-based board access

- Accessing a continuous signal
- Implemented using a variety of off-the-shelf software (from ASSET, Ohio Design Automation, National Instruments)
- Demonstrated with the National Semiconductor IC (SCANSTA400)

Courtesy Lockheed Martin

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Example of 1149.4-based board access

- Measuring a resistance
- Demonstrated by Lockheed Martin across their Intranet, via Microsoft's NetMeeting

Courtesy Lockheed Martin

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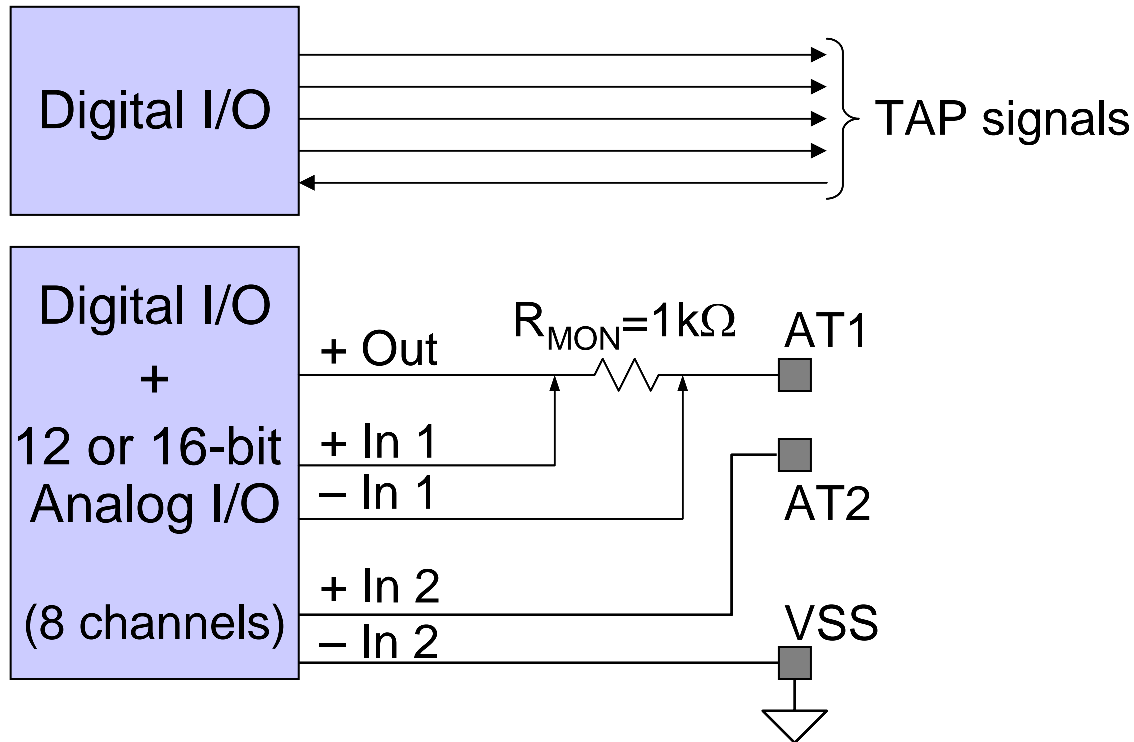
Laptop PC Mixed-Signal Tester



- Digital/Analog I/O cards commercially available from many suppliers (PCMCIA card or USB connection)
- Resistor + 2nd input channel can monitor delivered current

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Test Automation

- When will Analog BSDL happen?
  - Only in response to market demand
  - Simple 1149.4 applications may not need ABSDL
    - Monitoring pin signal voltages
    - Measuring input/output impedances
    - Fault detection for 1 or 2 element networks
  - Automation not essential for few 1149.4 ICs/ board
    - Manual coding of documented values, bits

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Summary

- 1149.4 access can test paths and pins
  - Analog, digital, differential, power rails, etc.
- Analog ATPG is key, but not yet available
  - Useful 1149.4 tests can be done with 1149.1 software
  - Analog hardware commercially available & linkable
- 1149.4 facilitates unique remote tests

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Conclusions

- 1149.4: a serial access structure, not a test solution
  - Many 1149.4-based *solutions* published
    - Faster parametric digital tests
    - Higher frequency mixed-signal tests
    - Unique diagnostic capabilities
- History: difficult to get 1149.4 right first time (it's analog)
  - Help is available
- Most companies waiting for "market pull" before developing formal 1149.4 products
  - Some companies forging ahead anyway
  - ICs with 1149.4 were, and are being, designed at multiple companies

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  - A few chapters available at http://www.chipcenter.com/TestandMeasurement/techarch.html
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