Analog Boundary Scan Description Language (ABSDL)

Bambang Suparjo
ABSDL Development Team Members

- Bambang Suparjo – Mentor Graphics
- Adam Cron - Synopsys
- Adam Ley – Asset-Intertech
- Heiko Ehrenberg – Goepel Electronics
- Keith Lofstrom - KLIC
- Ken Parker – Agilent Tech.
- Pete Collins – JTAG Tech.
- Anthony Sparks – JTAG Tech.
- Karla May - Corelis
- Jake Karrfalt - ASC
- Rohit Kapur – Synopsys
- Wim Driessen – JTAG Tech.
Objectives

- To discuss the status of ABSDL development.
- To identify the features to be added or to be removed.
- To identify the next stage of the development.
Outline of Presentation

- Introduction

- BSDL Description and Mixed-Signal Test (MST) Extension, with semantic checks

- Other Issue

- Conclusion and Future Plan
Introduction

- Effort to continue ABSDL development has been initiated during the 2004 1149.4 meeting.

- The development is based on Straw Dog Proposal-1, proposed by Ken Parker and John McDermid in May 2000.

- The initial proposal has been enhanced to Straw Dog 2.0 and Kitchen Sink 2.2.
Development Approach

- Review the individual requirements for Test Bus Interface Circuit (TBIC) and Analog Boundary Module (ABM) as described in the 1149.4 Standard.

- **TBIC operations should follow:**
  - Table 1 (Switching Patterns for TBIC)
  - Table 2 (TBIC Switching Assignments for Defined Instructions)

- **ABM operations should follow:**
  - Table 6 (Switch Patterns for Sample ABM)
  - Table 7 (Functions of ABM Switching Patterns)
  - Table 8 (Switching Pattern Requirements for Sample ABM).
BSDL Description (in general)

- BSDL description of an 1149.4 device.
- Compatible with 1149.1 BSDL.
- Still suitable for 1149.1 Interconnect Testing software.
BSDL Description Components

- Port Description Statements
- Standard and Optional Use Statements
- Component Conformance Statement
- Device Package Pin Mappings
- Grouped Port Identification
- Scan Port Identification
- Instruction Register Description
- Optional Register Description
- Register Access Description
- Boundary Scan Register Description
# Pin Types in Port Description Statements

<table>
<thead>
<tr>
<th>Pin</th>
<th>in</th>
<th>out</th>
<th>inout</th>
<th>linkage</th>
</tr>
</thead>
<tbody>
<tr>
<td>TAP</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Digital (Single Ended)</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Digital Diff.</td>
<td>X</td>
<td>X</td>
<td>X</td>
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<tr>
<td>ATAP (Single Ended)</td>
<td></td>
<td></td>
<td>X</td>
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</tr>
<tr>
<td>ATAP Diff.</td>
<td></td>
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<tr>
<td>Analog (Single Ended)</td>
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<td>X</td>
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<tr>
<td>Analog Diff.</td>
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<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
</tbody>
</table>
## Port Description Statements Example

```plaintext
port(
  -- TAP pins, as per 1149.1
  TCK, TDI, TMS: in bit;
  TDO: out bit;

  -- ATAP pins, as per 1149.4
  -- = required to be inout (bidirectional)
  AT1, AT2: inout bit;

  -- ATAPN pins, as per 1149.4
  -- = only required for optional differential ATAP
  -- = required to be inout (bidirectional)
  AT1N, AT2N: inout bit;

  -- digital pins, as per 1149.1
  -- = type/ direction not restricted
  A, B: in bit;

  -- digital differential pins, as per 1149.1
  -- = type/ direction not restricted
  D1, D1N: in bit;
  D2, D2N: in bit;

  -- analog pins, as per 1149.4
  -- = required to be inout (bidirectional)
  W, Y: inout bit;

  -- analog differential pins, as per 1149.4
  -- = required to be inout (bidirectional)
  X1, X1N: inout bit;
  X2, X2N: inout bit;

  -- linkage pins, as per 1149.1
  NC1, NC13: linkage bit;
  GND, VCC: linkage bit);
```
Semantic Checks for Port Description Statements

- Port ID's for the two ATAP pins (AT1 and AT2) shall be specified, with pin type INOUT assigned to them.

- If the device has a differential ATAP, port ID's for the additional ATAP pins (AT1N and AT2N) shall be specified, with pin type INOUT assigned to them.

- Analog ports with dot4 test resources shall be specified with pin type INOUT.

- Digital ports with dot4 test resources shall be specified with pin type INOUT.
Semantic Checks for Port Description Statements (Cont.)

- Analog differential ports with dot4 test resources shall be specified with pin type INOUT (both the positive and negative port of the differential pair).

- Digital differential ports with dot4 test resources shall be specified with pin type INOUT (both the positive and negative port of the differential pair).

- Linkage ports with dot4 test resources shall be specified with pin type LINKAGE.
Standard and Optional Use Statements

-- standard use statement, as per 1149.1
use STD_1149_1_2001.all;
-- Get Std 1149.1-2001 attrs and defns

-- optional use statement, as per 1149.1
-- = standard use statement, as per 1149.4
use STD_1149_4_2005.all;
-- Get MST attributes and definitions
Semantic Checks for Standard and Optional Use Statements

- A USE-statement shall exist for a standard 1149.4 package file to obtain the MST attributes definitions from the 1149.4 standard package file string, "STD_1149_4_2005"
Component Conformance Statement

-- component conformance, as per 1149.1
attribute COMPONENT_CONFORMANCE of Kitchen_Sink_2_2 :
   entity is
"STD_1149_1_2001";

Note: The 1149.4 component conformance and its semantic checks are shown in slides 37 and 38 respectively.
Device Package Pin Mappings

attribute PIN_MAP of Kitchen_Sink_2_2 : entity is PHYSICAL_PIN_MAP;

constant dip24 : PIN_MAP_STRING :=
  "TCK:11, TDI:10, TMS:14, " &
  "TDO:15, " &
  "AT1:8, AT2:17, " &
  "AT1N:9, AT2N:16, " &
  "A:2, B:3, " &
  "D1:4, D1N:5, " &
  "D2:7, D2N:6, " &
  "W:23, Y:22, " &
  "X1:21, X1N:20, " &
  "X2:18, X2N:19, " &
  "NC1:1, NC13:13, " &
  "GND:12, VCC:24";
Grouped Port Identification

-- grouped port identification, as per 1149.1
-- = required for digital differentials
attribute PORT_GROUPING of Kitchen_Sink_2_2 : entity is
  "Differential_Voltage ((D1, D1N),(X1,X1N))"," &
  "Differential_Current ((D2, D2N),(X2,X2N))";

- D1, D1N, D2, D2N – digital pins
- X1, X1N, X2, X2n – analog pins
attribute TAP_SCAN_CLOCK of TCK : signal is (20.0e6, BOTH);
attribute TAP_SCAN_MODE of TMS : signal is true;
attribute TAP_SCAN_IN of TDI : signal is true;
attribute TAP_SCAN_OUT of TDO : signal is true;
Instruction Register Description

attribute INSTRUCTION_LENGTH of Kitchen_Sink_2_2 : entity is 4;

attribute INSTRUCTION_OPCODE of Kitchen_Sink_2_2 : entity is
-- mandatory instructions, as per 1149.1
   "EXTEST  (1000), " &
   "PRELOAD (0010), " &
   "SAMPLE  (0010), " &
   "BYPASS  (0111), " &
   -- mandatory instruction, as per 1149.4
   -- = opcode may have any value except all ones
   -- = opcode value all zeros is not recommended (as per 1149.1)
   "PROBE   (1011), " &
-- optional instructions, as per 1149.1
   "CLAMP   (0100), " &
   "HIGHZ   (1101), " &
   "INTEST  (1110), " &
   "IDCODE  (0001)";

attribute INSTRUCTION_CAPTURE of Kitchen_Sink_2_2 : entity is "0001";
Semantic Checks for Instruction Register Description

- PROBE is a mandatory instruction for an 1149.4 compliant device and therefore shall be defined in attribute INSTRUCTION_OPCODE.

- The opcode value assigned to the PROBE instruction shall be unique.

  (note: the opcode for the PROBE can be any value except all ones)
Optional Register Description

attribute IDCODE_REGISTER of Kitchen_Sink_2_2 : entity is
"XXXX" & -- version
"0000000000000000" & -- part number
"10101010101" & -- manufacturer id
"1";
attribute REGISTER_ACCESS of Kitchen_Sink_2_2 : entity is
    -- access to mandatory registers, as per 1149.1
    "BOUNDARY (EXTEST, PRELOAD, SAMPLE), " &
    "BYPASS (BYPASS), " &
    "BOUNDARY (INTEST), " &

    -- access to mandatory registers, as per 1149.4
    -- = register BOUNDARY must be accessed by instruction PROBE
    "BOUNDARY (PROBE), " &

    -- access to optional register, as per 1149.1
    "DEVICE_ID (IDCODE)";
Semantic Checks for Register Access Description

- Register Access for the mandatory instruction PROBE shall be specified.
- PROBE shall access the Boundary Scan register.
Boundary Scan Register Description

- Boundary Length

  attribute BOUNDARY_LENGTH of Kitchen_Sink_2_2 : entity is 47;

- Boundary Register

  attribute BOUNDARY_REGISTER of Kitchen_Sink_2_2 : entity is

(continue in the next few slides)
Digital Pins

-- following cells (2) are for the digital pins
-- num cell port function safe [ccell disval rslt]
"0  (BC_1,    A, input,        x), " &
"1  (BC_1,    B, input,        x), " &

-- following cells (6) are for the digital differential pins
-- num cell port function safe [ccell disval rslt]
"2  (BC_1,    D1, input,        x), " &
"3  (BC_1,    D1N, input,       x), " &
"4  (BC_1,    *, internal,      x), " & -- D1:D1N Single Ended
"5  (BC_1,    D2, input,        x), " &
"6  (BC_1,    D2N, input,       x), " &
"7  (BC_4,    *, internal,      x), " & -- D2:D2N Single Ended

- Cell 4 is the single ended point of D1 and D1N
- Cell 7 is the single ended point of D2 and D2N
TBIC Based Control

-- following cells (4) are TBIC base controls
-- num cell port function safe [ccell disval rslt]
"8 (BC_1, *, internal, 0), " & -- Ca
"9 (BC_1, *, control, 0), " & -- Co
"10 (BC_7, AT1, bidir, 0, 9, 0, Z), " & -- D1
"11 (BC_7, AT2, bidir, 0, 9, 0, Z), " & -- D2

- Safe value for cell 8 is 0 in order to prevent calibration mode from being invoked during 1149.1 EXTEST operation.

- Safe value for cell 9 is 0. It is needed to control both bidirectional cells (cell 10 and 11).

- Safe values for cells 10 and 11 are 0 – satisfy the TBIC switching patterns for conventional EXTEST mode and extended interconnect test applications.
Semantic Checks for TBIC Based Control

- Boundary Scan cells shall be specified for TBIC Control (6.3):
  - Calibrate cell, functional value INTERNAL.
  - Control cell, functional value CONTROL; shall be listed in <disable_spec> for the TBIC Base Partition's D1 and D2 cells.
  - D1 cell, AT1 pin, functional value BIDIR; <disable_spec> shall be defined.
  - D2 cell, AT2 pin, functional value BIDIR; <disable_spec> shall be defined.
TBICN Based Control

-- following cells (4) are TBICN base controls
-- num cell port function safe [ccell disval rslt]

"14 (BC_1, *, internal, 0), " & -- Ca
"15 (BC_1, *, control, 0), " & -- Co
"16 (BC_7, AT1N, bidir, 0, 15, 0, Z), " & -- D1
"17 (BC_7, AT2N, bidir, 0, 15, 0, Z), " & -- D2

■ TBICN is needed for fully differential test application.

■ In Figure 27 of 1149.4 standard, the name of the TBIC inversion is TBIC(N). The parenthesis needs to be removed in BSDL. Refer to slides 41 and 43.

■ The determination of the safe values is similar to the TBIC based control.
Semantic Checks for TBICN Based Control

- If TBICN ports are defined in the <port description> then four boundary scan cells shall be defined for the TBICN control (6.5):
  - Calibrate cell (INTERNAL).
  - Control cell (CONTROL); shall be listed in <disable_spec> for the TBICN Base Partition's D1 and D2.
  - D1 cell, AT1N pin (BIDIR); <disable_spec> shall be defined.
  - D2 cell, AT2N pin (BIDIR); <disable_spec> shall be defined.
**TBIC and TBICN Extension Controls**

-- following cells (2) are TBIC extension controls
-- num cell port function safe

"12 (BC_1, *, internal, 0), " & -- D1
"13 (BC_1, *, internal, 0), " & -- D2

-- following cells (2) are TBIC extension controls
-- num cell port function safe

"18 (BC_1, *, internal, 0), " & -- D1
"19 (BC_1, *, internal, 0), " & -- D2

-- following cells (2) are TBICN extension controls
-- num cell port function safe

"20 (BC_1, *, internal, 0), " & -- D1
"21 (BC_1, *, internal, 0), " & -- D2

- To control additional internal test buses.
Semantic Checks for TBIC and TBICN Extension Controls

- Boundary Scan cells may be specified for TBIC extension control (6.4):
  - D1 cell (INTERNAL)
  - D2 cell (INTERNAL)

- Boundary Scan cells may be specified for TBICN extension control, if exist:
  - D1 cell (INTERNAL)
  - D2 cell (INTERNAL)
Cells Controlling ABMs (single ended)

-- following cells (4) control the analog signal W
-- num cell port function safe [ccell disval rslt]

"22 (BC_1, *, control, 0), " & -- C
"23 (BC_7, W, bidir, 0, 22, 0, Z), " & -- D
"24 (BC_1, *, internal, 0), " & -- B1
"25 (BC_1, *, internal, 0), " & -- B2

- The safe value of cell 23 needs to be set to 0 in order to prevent the pin from being connected to VG.

- The safe value setting shall be applied to other cells associated to all analog signal pins, in this example, for pins Y, X1, X1N, X2 and X2N.

- Cell 23 is controlled by cell 22.

- Each ABM has its own control cell.
Cells Controlling ABMs (diff.)

-- following cells (4) control the analog differential signal X1

-- num cell port function safe [ccell disval rslt]
"30 (BC_1, *, control, 0), " & -- C
"31 (BC_7, X1, bidir, 0, 30, 0, Z), " & -- D
"32 (BC_1, *, internal, 0), " & -- B1
"33 (BC_1, *, internal, 0), " & -- B2

-- following cells (4) control the analog differential signal X1N

-- num cell port function safe [ccell disval rslt]
"34 (BC_1, *, control, 0), " & -- C
"35 (BC_7, X1N, bidir, 0, 34, 0, Z), " & -- D
"36 (BC_1, *, internal, 0), " & -- B1
"37 (BC_1, *, internal, 0), " & -- B2
Semantic Checks for Cells Controlling ABMs

- Boundary Scan cells shall be specified for analog I/O pins (single-ended and differential) (7.3.5):
  - Control cell (CONTROL)
  - Data cell, analog I/O pin (BIDIR); <disable_spec> shall be defined
  - B1 cell, AB1 (INTERNAL)
  - B2 cell, AB2 (INTERNAL)
Semantic Checks
(Common for Boundary Scan Register)

- If there are no TBICN ports defined in the <port description> then there shall be no Boundary Scan Cells defined for the TBICN control.

- Safe values shall be defined for all TBIC, TBICN, TBIC Extension, TBICN Extension, and ABM Boundary Scan Cells.

- The disable result for all BIDIR cells shall be Z.

- Cell assignments shall be unique; Boundary Scan cells shall not be shared for multiple ABM or TBIC/TBICN control or TBIC/TBICN Extensions control and shall not be used for multiple functions.
MST Extension

- Component Conformance Statement
- ATAP Identification Statement
- TBIC Statement
- ABM Pins Statement
- Differential Pins Statement
Component Conformance Statement

**Statement**

```plaintext
<MST component conformance statement> ::= 
    attribute MST_Component_Conformance of <component name> : entity is 
    <MST conformance string>;

<MST conformance string> ::= "<MST conformance identification>"
<MST conformance identification> ::= STD_1149_4_1999
```

**Example**

```plaintext
-- component conformance, as per 1149.4
attribute MST_Component_Conformance of Kitchen_Sink_2_2 : entity is 
    "STD_1149_4_1999";
```
Semantic Checks for Component Conformance Statement

- Component conformance shall be specified with the attribute MST_Component_Conformance.

- The only valid <conformance string> is "STD_1149_4_1999";
ATAP Identification Statement

**Statement**

\[
\text{<MST ATAP identification statement> ::= attribute MST_AT1 of <component name> : entity is <port ID string>; attribute MST_AT2 of <component name> : entity is <port ID string>; }
\]

\[
[ \text{ attribute MST_AT1N of <component name> : entity is <port ID string>; attribute MST_AT2N of <component name> : entity is <port ID string>; ]}
\]

\[
<\text{port ID string> ::= " <port_ID> "}
\]

**Example**

```
-- ATAP port identification, as per 1149.4
attribute MST_AT1 of Kitchen_Sink_2_2 : entity is "AT1";
attribute MST_AT2 of Kitchen_Sink_2_2 : entity is "AT2";

-- ATAPN port identification, as per 1149.4
-- = only required for optional differential ATAP
attribute MST_AT1N of Kitchen_Sink_2_2 : entity is "AT1N";
attribute MST_AT2N of Kitchen_Sink_2_2 : entity is "AT2N";
```
Semantic Checks for ATAP Identification Statement

- The ATAP ports shall be identified in attributes MST_AT1 and MST_AT2, respectively.

- The pin type for the two ATAP ports shall be defined in the <Port description> as INOUT.

- For a differential ATAP, the additional ATAP pins (AT1N and AT2N) shall be identified in attributes MST_AT1N and MST_AT2N, respectively, otherwise these attributes shall not be present.

- The pin type for the two additional ATAP ports shall be defined in the <Port description> as INOUT.
TBIC Statement

-- TBIC register, as per 1149.4
-- = ref tables 1 and 2
attribute MST_TBIC of Kitchen_Sink_2_2 : entity is
  -- Ca_num Co_num
  "8, 9 : " &
  -- { partition_name D1_num D2_num}
  "IATB0 (10, 11), " &
  "IATB1 (12, 13), " &
  "IATB2 (18, 19)";

-- TBICN register, as per 1149.4
-- = ref tables 1 and 2
attribute MST_TBICN of Kitchen_Sink_2_2 : entity is
  -- Ca_num Co_num
  "14, 15 : " &
  -- {Npartition_name D1_num D2_num}
  "NIATB1 (16, 17), " &
  "NIATB2 (20, 21)";
Semantic Checks for TBIC Statement

- The cell assignment for TBIC control shall be specified in the attribute MST_TBIC.

- The first cell <Ca_num> in this attribute shall be the calibrate cell for the TBIC; the cell shall be listed in the Boundary Scan Register as INTERNAL cell.

- The second cell <Co_num> in this attribute shall be the control cell for the TBIC; the cell shall be defined in the Boundary Scan Register with function CONTROL and shall be listed in the <disable spec> for the ATAP ports.

- A <partition_name> for the TBIC Base Partition shall be specified with its two data cells <D1_num> and <D2_num>; the data cells shall be defined in the Boundary Scan Register.

- TBIC extensions are specified with a <partition_name> and the assigned data cells; the data cells shall be defined in the Boundary Scan Register; the listing order for multiple TBIC extensions is not relevant.
Semantic Checks for TBIC Statement (cont.)

- If a differential ATAP is implemented in the device, the cell assignment for TBICN control shall be specified in the attribute MST_TBICN, otherwise this attribute shall not be present.

- The first cell <Ca_num> in this attribute shall be the calibrate cell for the TBICN; the cell shall be listed in the Boundary Scan Register as INTERNAL cell.

- The second cell <Co_num> in this attribute shall be the control cell for the TBICN; the cell shall be defined in the Boundary Scan Register with function CONTROL and shall be listed in the <disable spec> for the additional ATAP ports.

- A <Npartition_name> for the TBICN Base Partition shall be specified with its two data cells <D1_num> and <D2_num>; the data cells shall be defined in the Boundary Scan Register.

- TBICN extensions are specified with a <Npartition_name> and the assigned data cells; the data cells shall be defined in the Boundary Scan Register; the listing order for multiple TBICN extensions is not relevant.
ABM Pins Statement

attribute MST_ABM_Pins of Kitchen_Sink_2_2 : entity is
  -- ABMs, as per 1149.4 = ref tables 6, 7, and 8
  -- port partition_name C_num D_num B1_num B2_num
     "W   (  IATB0: 22, 23, 24, 25 ), " &
     "Y   (  IATB0: 26, 27, 28, 29 ), " &
     "X1  (  IATB1: 30, 31, 32, 33 ), " &
     "X1N (  NIATB1: 34, 35, 36, 37 ), " &
     "X2  (  IATB2: 38, 39, 40, 41 ), " &
     "X2N (  NIATB2: 42, 43, 44, 45 )";

- **W** is the analog signal pin
- **IATB0** is the TBIC partition to be used for all 4 cells associated to pin **W**.
- The above explanation is also applied to other analog pins, **Y, X1, X1N, X2** and **X2N**.
Semantic Checks for ABM Pins

Statement

- Every ABM shall be listed in attribute MST_ABM_Pins

- Each ABM shall be listed with its port ID, as defined in the port description (attribute <port>), followed by the TBIC partition it is connected to and the four Boundary Scan cells assigned to the ABM control register.

- The TBIC partition name shall be defined in <MST_TBIC>.

- If the ABM is connected to a TBICN partition, than that partition name shall be defined in <MST_TBICN>.

- The order of the Boundary Scan cell assignment in the ABM pins table is the following: Control cell (C_num), Data cell (D_num), B1 cell (B1_num), and B2 cell (B2_num).

Note: The bit order in this attribute is referring to the bit order in Table 8 in the standard.
Semantic Checks for ABM Pins Statement (cont.)

- A Boundary Scan cell assigned to \(<C\_num>\) shall be defined in \(<BOUNDARY\_REGISTER>\) as CONTROL cell.

- A Boundary Scan cell assigned to \(<D\_num>\) shall be defined in \(<BOUNDARY\_REGISTER>\) as BIDIR cell and shall have a \(<\text{disable\_spec}>\) which specifies \(<C\_num>\) as its control cell.

- A Boundary Scan cell assigned to \(<B1\_num>\) shall be defined in \(<BOUNDARY\_REGISTER>\) as INTERNAL cell.

- A Boundary Scan cell assigned to \(<B2\_num>\) shall be defined in \(<BOUNDARY\_REGISTER>\) as INTERNAL cell.
Differential Pins Statement

attribute MST_Diff_Pins of Kitchen_Sink_2_2 : entity is
  -- DBMs at single-ended side of differential drivers/receivers
  -- representative_port associated_port num
  "D1 : D1N ( 4), " &
  "D2 : D2N ( 7)";

- The pin order defines the polarity i.e. D1 is positive and D1N is negative.
- Cell 4 is the single ended point of D1 and D1N.
- Cell 7 is the single ended point of D2 and D2N.
Semantic Checks for Differential Pins Statement

- Boundary Scan data cell numbers for DBMs on the single-ended side of differential drivers/receivers shall be assigned to the respective differential port pair in attribute MST_DIFF_PINS.

- First, the representative port ID shall be listed, then the associated port ID, followed by the Boundary Scan cell number.

- The two port ID's shall be defined in the port description (attribute <port>).

- The DBM's Boundary Scan cell shall be defined in the attribute <Boundary_Register>.
Other Issue

- How to describe internal cells in ABSDL?
  - Which patterns would be valid at ABM that wired to a linkage pin?
Conclusion and Future Plan

- Basic requirements of ABSDL description have been identified.

- More complex or specific conditions need to be identified to provide more stable ABSDL description.