DYNAMIC TESTING FOR RADIATION INDUCED FAILURES IN A STANDARD CMOS SUBMICRON TECHNOLOGY PIXEL FRONT-END[1]

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Abstract

A testing method for the detection of performance degradation induced by high-dose irradiation in high-energy experiments has been developed. This method was successfully applied for testing the analogue CMOS front-end of a silicon pixel detector. The major effects of radiation induced faults have been investigated with respect to the special layout used for the nMOS transistors.

I. INTRODUCTION

Electronic circuits employed in high energy physics experiments are usually exposed to very high secondary particle fluxes originating from proton-beam collision. As a function of the position in the detector these fluxes and thus, the total dose deposited, change significantly ranging from tens of Mrad (inner detector) down to a few krad. Depending on the type of radiation as well as on the properties of the circuit design and the technology, electronic circuits are temporarily or permanently damaged. In order to cope with this problem radiation hard technologies are desirable. However, besides cost considerations, radiation hard processes are not always able to match the low power and high density needs of the complex circuit architecture planned to be used in the Large Hadron Collider (LHC). An alternative approach to achieve radiation resistance is to take advantage of commercial technologies with reduced gate oxide thickness t_{ox} and shallow trench isolation [1]. In particular, the reduction in gate oxide thickness which accompanies the scaling down of the device size in deep submicron technologies, renders transistors naturally less sensitive to radiation damages. Moreover, due to the impressive density of these modern processes, it is conceivable to employ special layout techniques and architectures to increase the radiation hardness of the design. These aspects become very important especially in high energy experiments like those performed at the CERN laboratories, where detector systems of very high complexity are requested comprising an order of 10^7 detector channels [2]. Though much progress has been achieved in the technology of radiation hardness, performance degradations due to irradiation are not completely avoidable. Thus, appropriate test techniques have to be employed to continuously check for the integrity of such complex detector system also during the ongoing experiment. The objective of this work is to dynamically test the analogue front-end of a pixel detector for radiation induced failures and performance degradation. The method used is based on a fault signature generation defined on the basis of the state-space analysis for linear circuits. By sampling the response of the circuit under test (CUT) to a simple rectangular pulse, a set of parameters α are evaluated which are functions of the circuit singularities and constitute a signature for the CUT. Amplitudes perturbations of these parameters engendered by element drift failure, indicate a possible faulty condition. The proposed testing procedure has been successfully applied to investigate the effect of radiation on an analogue front-end circuit which was radiation hardened by using a special layout [3, 10].

II. DYNAMIC TEST PROCEDURE

The method is based on the linear, strictly proper, time-invariant, single-input, single-output network theory. By virtue of this theory, the system input u(t), the observable output y(t) and the state vector X of the all pole system are related by the canonical state equations:

$$\begin{aligned} \dot{X} &= AX + Bu \\ y &= CX \end{aligned} \qquad (1)$$

where B=(0,0,....,1)', C=(1,b1,b2,....,bm,0,...,0) and the coefficient matrix A is an n-order square coefficient matrix. It is assumed that the circuit is stimulated by a piecewise constant input stimulus of amplitudes $(1,\alpha_1,\alpha_2, ...,\alpha_n)$:

$$u(t) = \alpha_k \qquad kT \le \tau \le (k+1)T \qquad (2)$$
$$k=0,1,...,n$$

and α_k and T are respectively the amplitudes and width of each piece of the signal. For X(0) = 0 and α_o normalized to unity, the response to this stimulus is :

$$X((n+1)T) = \left[(e^{AT})^n + \alpha_1 (e^{AT})^{n-1} + \ldots + \alpha_n I_n\right] V \qquad (3)$$

where $V = \left[e^{AT} - I\right] A^{-1} B$ and I is the unit matrix. From the Cayley-Hamilton theorem, it follows that if the amplitudes α_k coincide with the coefficients of the characteristic polynomial of the state transition matrix, the circuit, for $t \ge (n+1)T$ is in a null state. This particular piecewise constant stimulus (fig.1) is known as complementary signal (COMPSIG) [3]. Then the set of α coefficients that after

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initialization of the circuit in [0, T], drives the circuit to zero-state at time (n+1)T depends strictly on the circuit singularities and constitutes a circuit signature. Then if λ_i, i=1,2,...,n are the circuit poles, the α_j j=1,2,..n parameters are given by :

$$\alpha_j = (-1)^j \exp \sum_{i=1}^{n} \lambda_i T \qquad (4)$$

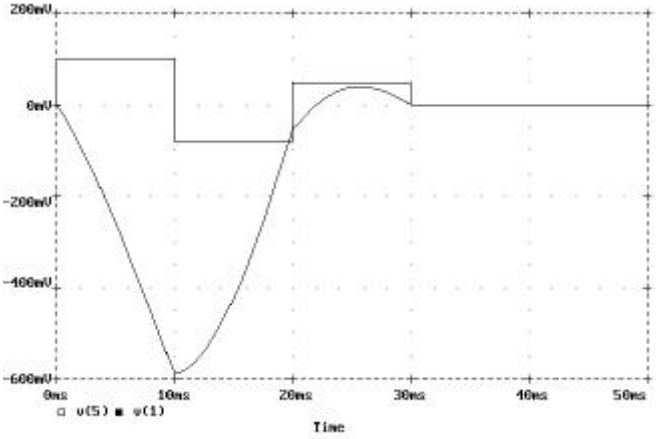

Fig. 1: Input stimulus and circuit response

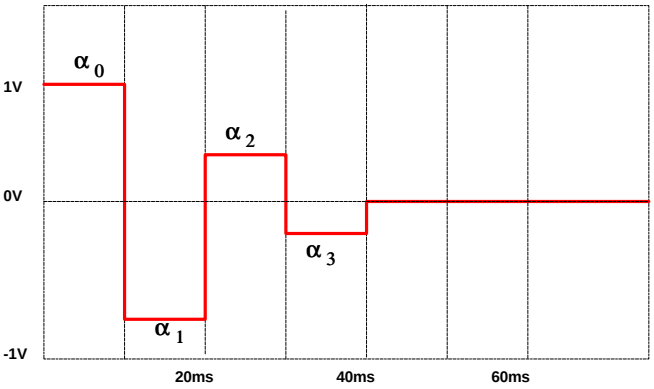

Fig. 2: The COMPSIG signal shape for a third order circuit

In general when transmission zeros are present, the observable output of the network is equal to the weighted sum of the state variables of the equivalent all-pole part of the circuit. It is possible to conclude that each circuit has its own n-set of values which represents its behaviour. Then a faulty circuit can be in principle distinguished from the good one on the basis of this set (signature).

III. Outline of the Test Process

Obtaining the signature of the circuit, corresponds to finding the stimulus able to drive the network to the zero-state at t=(n+1)T. Then the circuit remains in the zero state also for $t \geq (n+1)T$ after the end of the excitation. Analytically stated, the complementary signal may be written as:

$$u(t) = \sum_{k=0}^{n} \alpha_k S(t - kT) \qquad (5)$$

where α_o=1 and S(t) is the shifted pulse function. The strictly proper circuit response to u(t) can be expressed as a sum of the circuit responses to the shifted pulses $y_o(t)$:

$$y(t) = \sum_{k=0}^{n} \alpha_k y_o(t - kT) \qquad (6)$$

this must vanish for $t \geq (n+1)T$. In practice it is possible to conclude from equation (6) that the α 's can be evaluated by sampling in at least (n+1) points the circuit response to a small rectangular pulse of width T and then solving a system of n linear equations whose coefficients are the sampled values of the response (fig.3) [4]. The pulse width T must be chosen so that the signal spectrum covers the nominal circuit bandwidth. In this way optimal sensitivity to circuit pole perturbations is achieved [5].

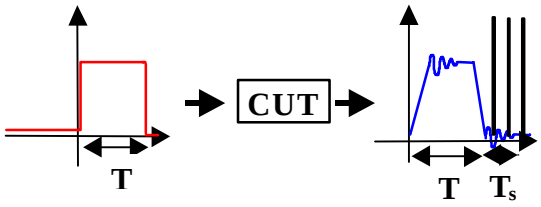

Fig. 3: Outline of the practical evaluation of α. Generally Ts is assumed to be equal to T

A better immunity to measurement noise can be obtained via enlarging the sample size to 2n+1 points, while rejection of possible jitter can be obtained by averaging over several samples. An accurate evaluation of DC offset must be performed as well in order to subtract the value of the base-line from sampled values. Once the α_I parameters are estimated on the basis of the measurements, an acceptability region for them must be defined on the basis of the specifications assigned to the linear performances of the CUT. The mapping of the specification tolerances into an acceptability region in the α-space can be realized by exploiting the analytical relationships between the CUT specifications and the circuit parameters affecting its poles. If such relations are not analytically available or not easy to find, the acceptable α's can be determined by a statistical sampling of the space of the circuit parameters. In other words, the boundaries of the region in which the CUT poles satisfy all given specification can be found by a Monte Carlo simulation.

IV. Circuit Under Test Description

The test chip was designed at CERN [7, 8]. To achieve radiation resistance even in a commercial submicron VLSI technology a special layout technique was used referred to as closed geometry or edgless transistor. Due to this structure no leakage pathes can be created [5, 6, 10]. The considered test chip is a detector circuit for the inner tracking in the LHC experiment [2]. It was manufactured in a standard 0.5µm CMOS technology from Mietec. Each chip comprises of two columns of 64 replicas of the same channel, thus 128 detector channels. Each column can be selected by a test and mask shift register. In figure 4 the circuit schematic of one channel is shown. It comprises of an analogue front-end for the read-out of the signal coming from the pixel detector which is directly bump-bonded to the input of the charge sensitive amplifier (CSA). This amplifier, supplied at 3.3V, is a nMOS cascode stage with a feedback capacitance C_f of 24fF, a gain of $1/C_f$ equal to 40mV/fC and a charge time constant C_f/gm of 5ns. The detector leakage current is one of the most important constrains, as the amplifier is directly coupled to the detector. In order to compensate for the

leakage current from the detector a high impedance DC feedback was implemented using a MOS resistor [9]. This feedback network comprises of a differential p-channel pair. One output is connected to the amplifier input which is equivalent to a resistor of $R_f=1/g_{m1}$ in parallel with C_f. The current of the second differential output (drain of M_{1b}) charges the capacitor C, thus, the resulting voltage controls the gate of the n-channel MOS transistor M_2. This second feedback path is equivalent to an inductor connected in parallel with C_f and therefore the detector leakage current (DC component) flows

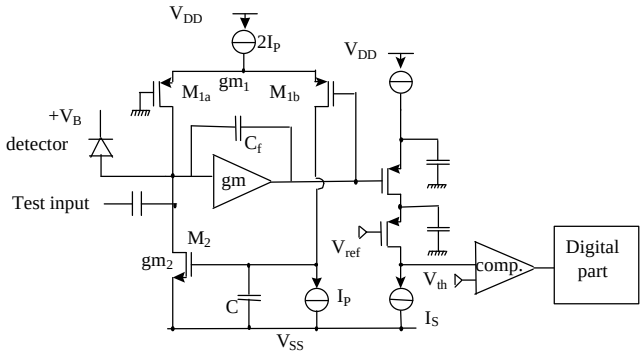

Fig. 4: Schematic of the analogue front-end of a pixel detector.

into M_2 rather than into the equivalent feedback resistor R_f. The main advantage of this configuration is that since M_2 sinks the total detector leakage current, this current may largely exceed the value of I_P without compromising the circuit operation. The bias current I_P for pixel detector is typically in the order of tens of nA and the equivalent feedback resistance is 6MΩ. The transconductance g_{m1} is also responsible of the discharge time τ_f of the CSA wich is defined as $\tau_f=R_fC_f=C_f/g_{m1}=140$ns. The transconductance g_{m2} of transistor M_2 is chosen so that $C/g_{m2}>>C_f/g_{m1}$. The second stage is a 2nd order shaper amplifier with a shaping time of 23 ns. It can be tunned via a bias current I_S. Finally, each front-end has an additional test input which is connected to the CSA via a capacitor. For the investigations four test chips were used to measure the impact of the irradiation. Whereas chip 1 was not exposed to irradiation, the other chips were exposed to an X-ray source of 10keV with a radiation rate of 4 krad/min. Chip 2 was exposed to an irradiation for 200 min. resulting in radiation dose of 800krad while chip 3 was exposed for 500 min and thus a irradiation dose of 2Mrad. A fourth chip (chip 4) was irradiated by only 200krad and was used only to check the sensitivity limit of the proposed testing method.

V. Irradiation Effects on the Pixel Front-End

All chips were first tested by applying at the test input of the CSA a single pulse of width T=10ns and an amplitude of 80mV. The measured pulse responses for the first three chips at the output of the charge sensitive amplifier and the output of the shaper are shown in figure 5 and 6, respectively. From the above figures it is obvious that the pulse response of the chip 2 (800krad) only slightly deviates from the response of the non-irradiated chip 1. In contrast, in case of higher dose irradiation (chip 3), the deviation of the pulse response at both the charge sensitive amplifier and the shaper output is evident. Mainly there are two effects due to the irradiation in MOS transistors: first, a shift of the threshold voltage for both the n- and the p-channel transistors and second a decrease of the mobility, which is pretty large for nMOS transistors. In general the g_m is affected by mobility variation due to irradiation and thus, not depended from V_T , if the transistor has a constant bias current. However, in this circuit the bias current comes from pMOS mirrors which due to irradiation changes, resulting in a V_T dependency which in turn leads to a transconductance decrease.

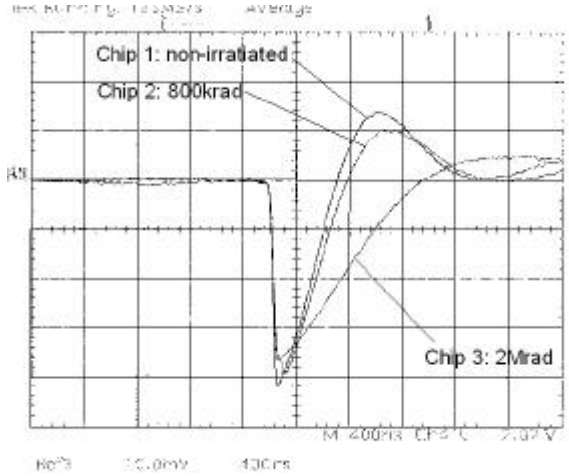

Fig. 5: Pulse response measured at CSA output (10mV/div, 400ns/div)

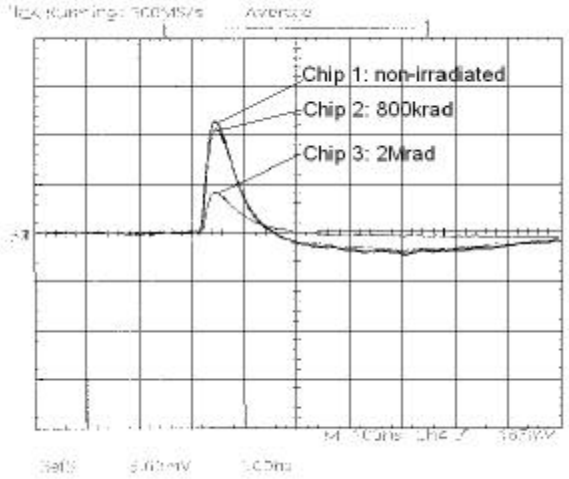

Fig. 6: Pulse response measured at shaper output (5mV/div, 100ns/div)

Therefore, in the CSA the deviation of the response could be explained by considering that the charges trapped in both the thin and the field oxides of the pMOS transistors M_{1a} and M_{1b} cause a decrease of the threshold in line with the relationship:

$$V_T = V_{TC} - \frac{Q_{ox}}{C'_{ox}} \qquad (7)$$

where: $$V_{TC} = \phi_{MS} + 2\psi_B + \frac{\sqrt{4\varepsilon_S q N_A \psi_B}}{C'_{ox}} \quad (8)$$

with V_T the threshold voltage after irradiation, V_{TC} the threshold voltage of the non-irradiated device, that is not affect by trapped charges, Q_{ox} the positive charge (holes) trapped in the oxide, C'_{ox} the oxide capacitance per unit area, ϕ_{MS} is the flat-band voltage, ψ_B is energetic gap between the Fermi level and the intrinsic Fermi level, q the electron charge, N_A the doping concentration and ε_s the semiconductor permittivity. The g_m reduction causes an increase in the feedback resistance $R_f = 1/g_{m1}$ which in turn yields a longer discharge time (cf. fig. 5). The same effect, namely the reduction of the transconductance, can be observed on the output of the pMOS shaper (fig. 4), with a clear reduction in the gain (fig. 6). The transfer function of the shaper reads:

$$\frac{i_{out}}{v_{in}} = \frac{g_m s\, t_o}{(1+s\, t_o)^2}$$

where $t_o = C/g_m$ and s is the complex frequency. From this equation it is evident, that a reduction in g_m directly translates into a lower output current.

VI. COMPSIG Testing Procedure For the Front-End

Beside the pulse as test stimulus, another test signal was applied, referred to as complementary signal or COMPSIG [4, 5] which is a piece-wise constant signal. As mentioned before this signal drives the circuit after a defined time T to the zero-state, i.e. the response vanishes. In fig. 8 the COMPSIG signal for the investigated circuit is depicted.

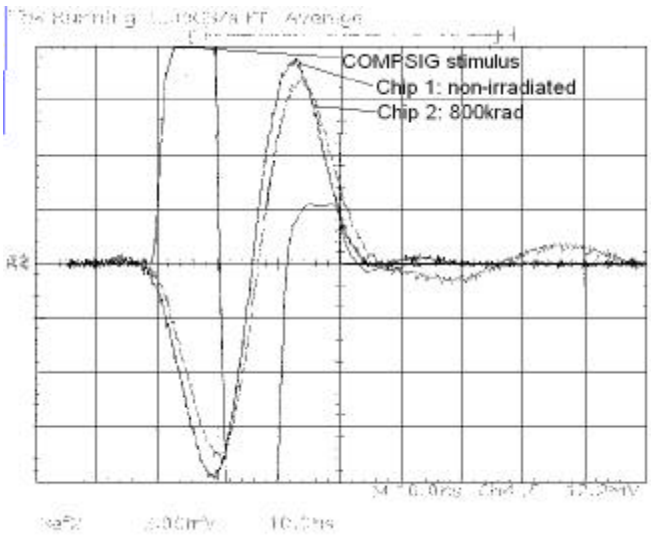

Fig. 7: The compsig response of chip1 and 2 at the CSA output. (compsig scale factor is 20mV/div, for the CSA it is 5mV/div)

Applying this type of test signal the difference between the responses of chip 2 (irrad. 800krad) and the non irradiated one becomes even more evident. In figure 7 and 8 the results of this test are shown again for the output on the CSA and the output of the shaper, respectively. The results show that, even in case of the 800krad dose, the above mentioned COMPSIG test is able to detect the degradations of the amplifier performances. This appears even more evident when applying the complementary signal to the high dose (2Mrad) irradiated chip. Measurements in the lab confirmed this. From those investigations it clearly turns out, that radiation hardened devices do not necessarily produce high circuit immunity to radiation and the proposed test methods provide a mean to detect performance deviations and allow to monitor the correct functionality of the circuit during its operating life, i.e. during the experiment when no direct access to the detector system is possible. Finally, summarising the results from the employment of the complementary signal method, the test procedures may still be improved to increase the discrimination capability in order to allow for an easier and faster check of the circuit quality. This work is currently ongoing. The effects of radiation induced faults in the analogue front-end of a pixel detector employed in high energy physics experiments has been investigated. A testing strategy formerly developed to detect hard and soft faults in linear analogue circuits has been successfully employed to detect most of specification deviations on test chips irradiated with 800krad and 2Mrad dose and the results are here reported. The results show that, even for the 800krad dose, the test devised is able to detect the degradations of the amplifier performances. These modifications become more evident by applying the complementary signal approach.

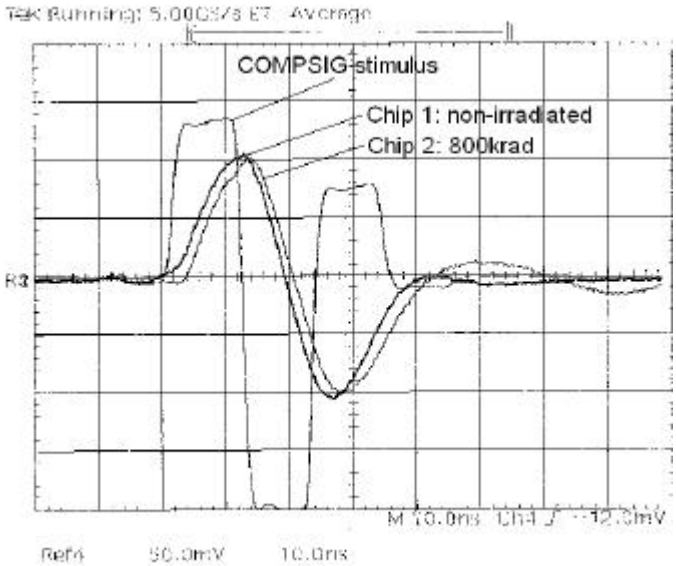

Fig. 8: Shaper responses (compsig 20mV/div, shaper 5mV/div)

VII. Sensitivity Of The COMPSIG Method To Low Dose Radiation Damages

Up to this the impact of moderate and high dose irradiation was considered. Now the previous methods will be considered for low dose irradiation. First, again for the application of the pulse stimulus and then for the COMPSIG stimulus. In figure 9 the measured responses for an non-

irradiated and a low dose irradiated chip (200krad) are depicted when the output of the CSA is observed. It can clearly be recognised that there is no difference between the two responses and thus appear like one waveform. Thus, either the impact was insignificant, or this method is not sufficient.

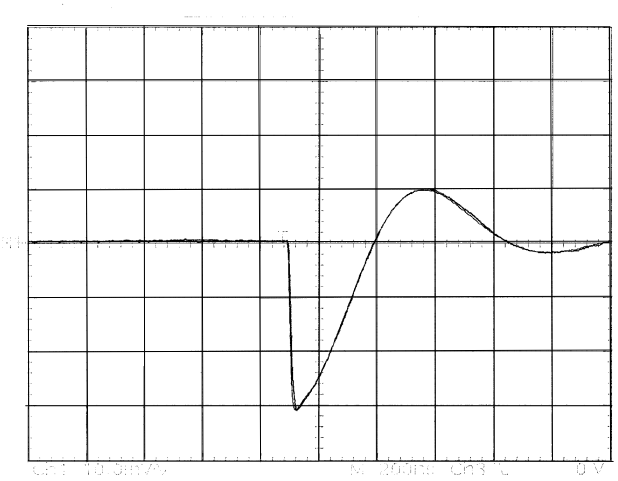

Fig. 9 CSA pulse response comparison between the chip 1 (non irradiated) and the chip 4 (200krad).

For this reason the pulse was applied again but now measured at the output of the shaper. The responses are shown in figure 10. Again the difference between the two responses is very low and only becomes visible in the tail of the waveform. This now gave rise to investigate the situation when applying the COMPSIG stimulus. The measured results are given in figure 11 showing the COMPSIG stimulus (light waveform line) and the two responses for a non-irradiated (waveform with the larger amplitude) and for a low dose irradiated one.

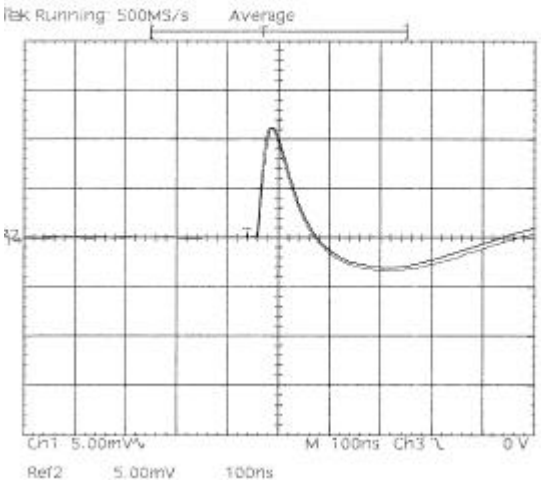

Fig. 10. Shaper pulse response comparison between chip 1 (non irradiated) and chip 4 (200krad).

Due to the expected higher sensitivity of the shaper response and the target to test the complete analogue part of the front-end the output of the shaper was measured.

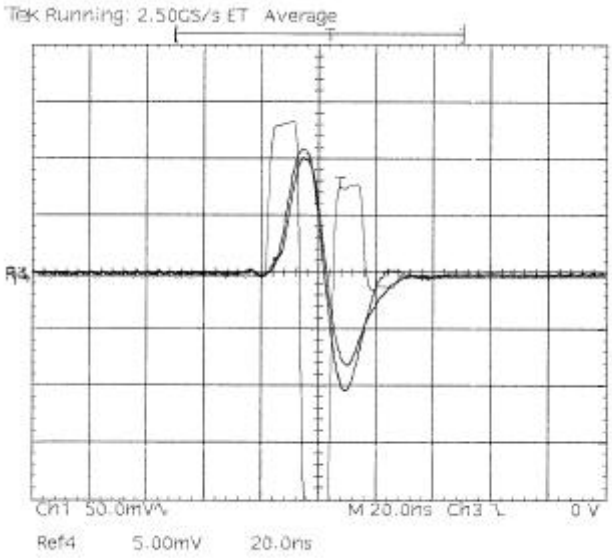

Figure 11: Compsig response at the shaper output of chip1 and chip 4. The compsig scale factor is 50mV/div, 20ns/div, the shaper output scale factor is 5mV/div.

As can be seen from fig. 11 the response of the irradiated chip crosses the zero line later then the response of the non-irradiated. However, in practice it turned out that it was difficult to exactly identify the difference of the zero-crossing for circuits with different irradiations. On the other hand it was always possible to use the attenuation of the amplitude as an indication for the impact of the irradiation.

Thus, from those measurements and practical experience we can conclude, that for low dose irradiation the COMPSIG stimulus is more appropriate then for higher doses of irradiation. Thus, this allows to use the above described method to distinguish between different irradiation doses.

Since for the test access to the pixel detector input as well as to the shaper output is necessary additional on-chip components are required. This also allows for an implementation of a GO/NOGO test implementation. In the following paragraph this on-chip hardware and procedure will be described.

VIII. On-Chip Hardware For The COMPSIG Method

As mentioned before, different test techniques can be easily applied if some moderate additional on-chip hardware is implemented, which is referred to as design-for-testability (DfT). In the recent years there has been much effort put into establishing a standard which now is known as the 1149.4 standard of a mixed-signal test bus [11]. Due to this fact, we were interested in evaluating the potential benefit of this test hardware for the purpose of our test. We will shortly describe the circuit as it can be used in our application. The circuit is shown in figure 12.

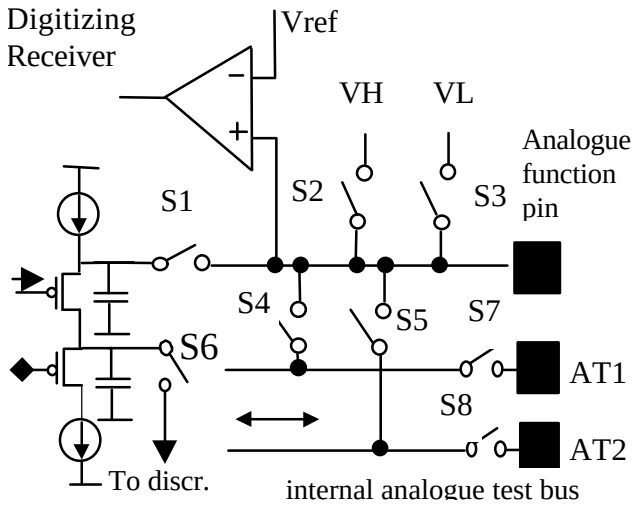

Fig. 12 Scheme for the design-for-testability of the the analogue front-end

On the left side the output of the shaper is shown (cf. fig.4). In the normal operation all switches are open except for S6 which is connected to the discriminator and then to the digital part of the pixel read-out. For the implementation of the complete standard three additional pins are required, i.e. the analogue function pin and two analogue test bus pins AT1 and AT2 to facilitate the external test. Furthermore an on-chip comparator is foreseen which can be connected to an output pin of the chip or to an on-chip flip-flop chain (scan path). This scan path allows to serially shift out the comparator captured output values synchronized on the scan path clock. This shown configuration is needed to also test the connections to the detector circuit for shorts and open. For the sake of calibration of the comparator all switches are open and a threshold Vref is applied on one input whereas on the other input either VH via S2 or VL via S3 are connected.

In the proposed DfT implementation, the circuit is inserted between the analogue part (output of the shaper as shown on the left side in fig.12) and the discriminator. The impact of the parasitic capacitance due to the inserted switch S6 in the signal path is negligible. In the test mode the shaper output is connected to AT1 by closing the switches S6 and S7. The test stimulus is fed to AT2 which is connected to the test input of the CSA (cf. fig.4) by closing S8. Now on AT2 the pulse or COMPSIG signal can be applied while on AT1 the response from the shaper can be measured. As pointed out before for the low irradiation only the evaluation of the amplitudes is practical. Thus, in this case as alternative the on-chip comparator (digitizing receiver) could be used to observe the shaper output. In this case S6 remains closed, but S7 is open and S4 is closed to connect the shaper output to the comparator. Now the COMPSIG is applied to AT2 whereas the output of the shaper is connected to the comparator. For this application the reference Vref has to be generated such, that it follows the good COMPSIG response of the circuit taking some defined margin above and below the good amplitude into account. If the amplitude deviation is larger than the applied Vref the comparator switches and thus gives an indication for an irradiation impact.

For the comparator in principle, a simple inverter could be used. However, as we are dealing with analogue signals which don't exhibit the required rise and fall times, this is not feasible for an accurate threshold detection. Moreover, due to the slow signals bouncing is likely to appear and corrupts the test scheme. Beside this, also a DC current will occur due to the on-switching of the p- and n-channel transistors. Therefore a real analogue comparator is needed.

Moreover using the COMPSIG as a test stimulus, means checking that the circuit output in some (low irradiation case) instances takes on a well defined level. Since the amplitude of the samples must be accurately evaluated, the comparator has to be clocked and connected at the shaper output, in compliance again with the IEEE1149.1-4 standard scheme.

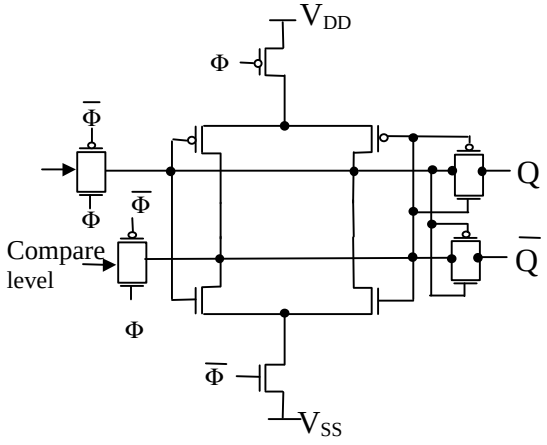

Fig. 13: Zero static power comparator

A possible scheme for the comparator is reported in figure 13, which shows a "zero static power analogue comparator" consisting of two input switches, a switched cross-coupled pair, and output isolators to balance the load on the cross-couple and to isolate the analogue signals from the digital circuitry downstream.

This circuit draws current from the supplies only briefly, when it changes from follow to latch mode. However, the signal-side storage node and sources of the transistors connected to it are a nonlinear parasitic load on the signal.

Also, the input switches will inject some charge into the input when the cell is latched. After latching, some time is required to settle from sample to latch mode, or offset may occur. This comparator may develop offsets from charge trapping in the cross-coupled transistors, so a third precharge state may be desirable for highest accuracy. The four isolation transistors minimize the output loading effects when the comparator is near balance.

IX. Conclusion

The effects of radiation induced faults in the analogue front-end of a pixel detector employed in high energy physics experiments has been investigated. A testing strategy formerly developed to detect hard and soft faults in linear analogue circuits, has been successfully employed to detect most of the specification deviations on test chips irradiated with 200krad and 2Mrad dose. The results show that, even

for the 200krad dose, the test devised is able to detect the degradations of the amplifier performances. These modifications become more evident by applying the complementary signal approach rather than applying the simple pulse. Summarizing the results from the application of the complementary signal method, the test procedure may still be improved to increase the discrimination capability in order to allow for an easier and faster check of the circuit quality. This work is currently ongoing. Also, the results show that hardened devices do not necessarily produce high circuit immunity to radiation and the proposed test method provides a mean to detect these performance deviations and to monitor them during the operating life of the chip. In compliance with the standard P1149.4, a possible scheme to make the output of the analogue part accessible without electrically loading the nodes of the circuit, has been suggested to simply check for radiation induced degradations in the analogue front-end even during the functionality of the whole system.

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