

1149.6 Test Chip Characterization Results

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Agilent Technologies

Overview

- Test chip overview
- 1149.6 features implemented
- Test setup and conditions
- Test results
 - Functional verification
 - Electrical verification
 - Defect injection
- Conclusions

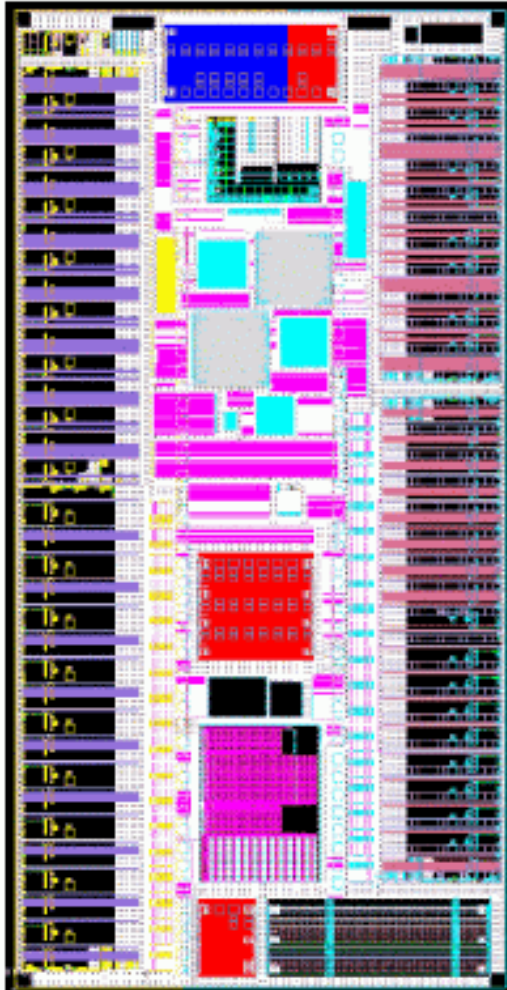


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Test Chip Context



- ❑ 2.5M gates + several RAMs
- ❑ 47 SerDes channels @3.125 Gb
- ❑ .13u, 1.2V, 8 metal layers
- ❑ 399 pins, 11.2mm x 5.6mm die
- ❑ **1149.6 AC EXTEST compliant**



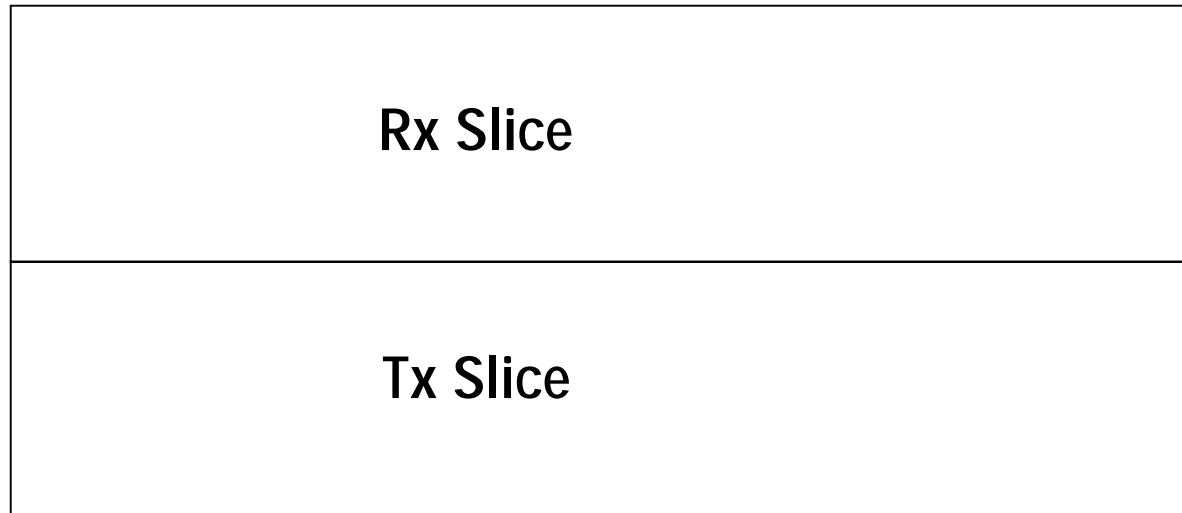
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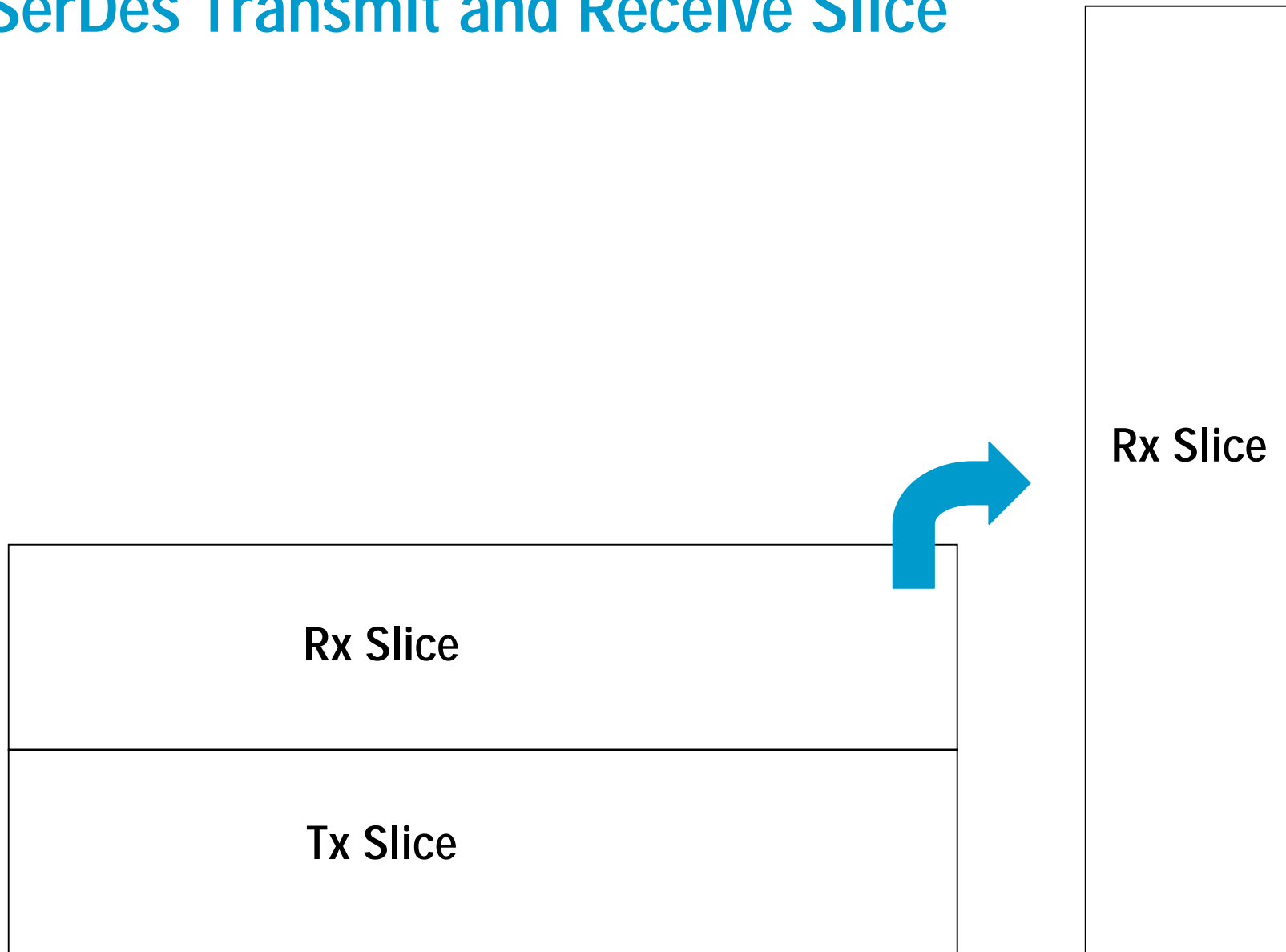
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SerDes slice (Tx and Rx)

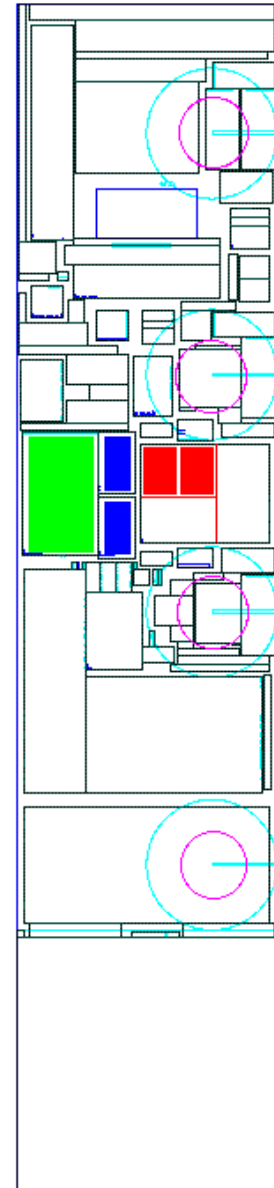
SerDes Transmit and Receive Slice



SerDes Transmit and Receive Slice



SerDes Receive Slice



1149.6 Test Receiver in SerDes Rx

- Two test receivers + SR flops:
1.2% of SerDes Rx slice area

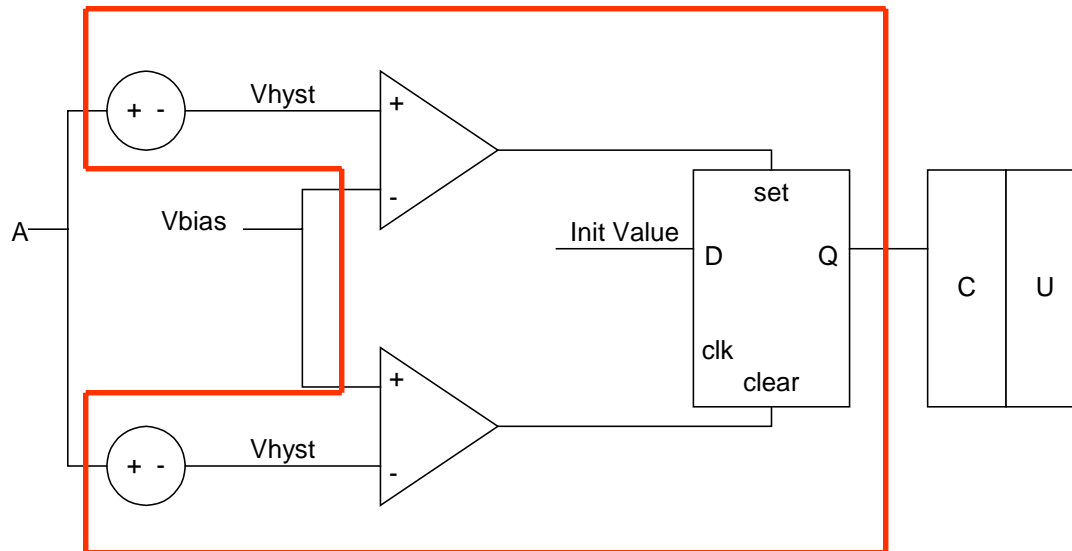
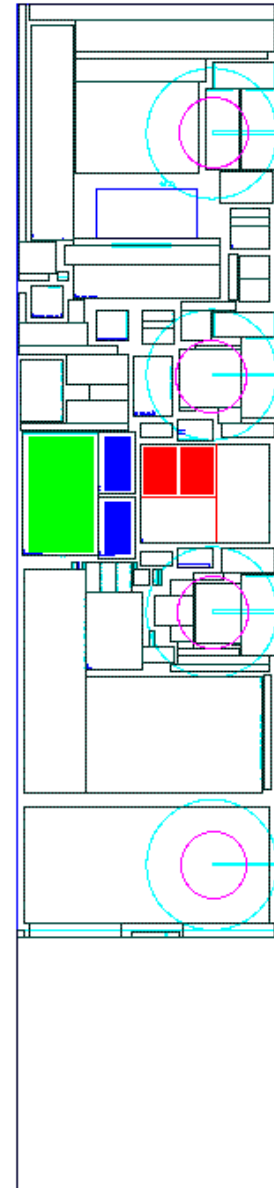
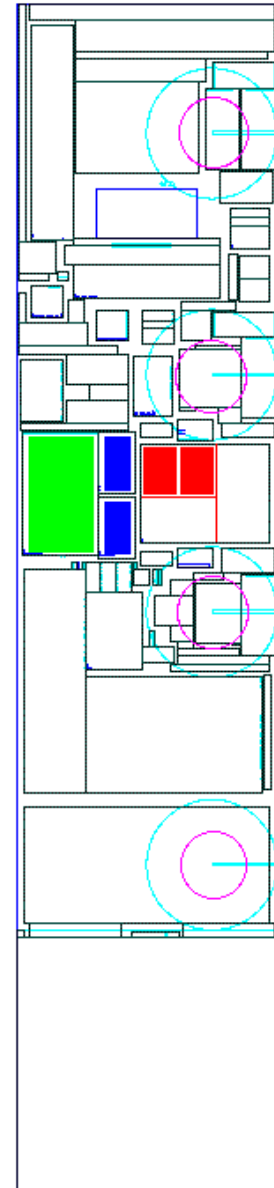


Figure 2: Test Receiver



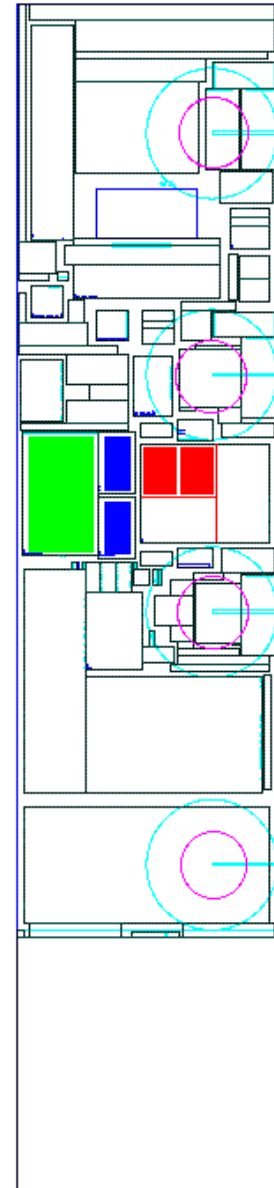
1149.6 Test Receiver in SerDes Rx

- ❑ **Two test receivers + SR flops:**
1.2% of SerDes Rx slice area
- ❑ **Two (metal) 5pF AC-coupling caps:**
1.6% of SerDes Rx slice area



1149.6 Test Receiver in SerDes Rx

- ❑ **Two test receivers + SR flops:**
1.2% of SerDes Rx slice area
- ❑ **Two (metal) 5pF AC-coupling caps:**
1.6% of SerDes Rx slice area
- ❑ **For LPF *estimation*: 50pF (FET) cap:**
3.1% of SerDes Rx slice area,
so a 5pF LPF cap would be .31%



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- ❑ Conclusions



1149.6 Features Implemented in Test Chip

Implemented:

- AC EXTEST PULSE instruction
- Interface with off-chip AC Coupling Caps
- Interface with on-chip AC Coupling Caps (Infiniband)

Not implemented:

- AC EXTEST TRAIN was not yet in the standard at design time
- Self-referencing front-end for test receiver (i.e. low-pass filter)
 - Always AC coupled: Vbias by Permission 6.2.3.2 (draft 2.3)



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Test Setup

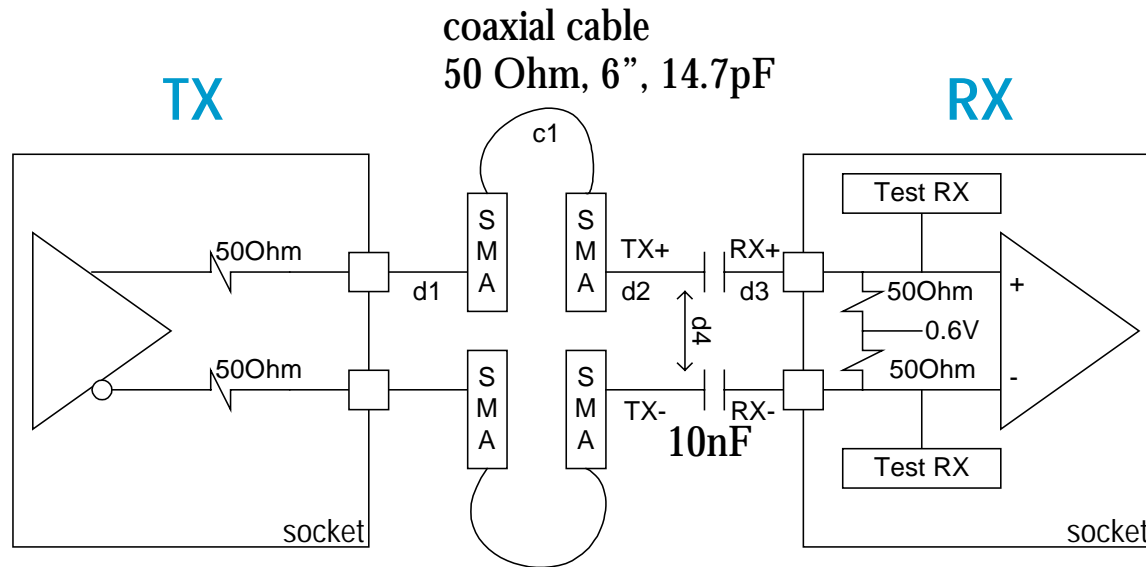


Figure 1: On board AC coupled TX/RX pair Test Setup

d1: 2889-9020 mils
d2: 343-375 mils
d3: 4804-8615 mils
d4: 50-500 mils

Test Conditions

- Process : nominal (.13u)
- Voltage : nominal (1.2 V)
- Temperature : 55 C
- 8 TX/RX pairs with AC coupling caps on PC board
- 1 TX/RX pair with AC coupling caps on chip



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Functional Verification Tests

DC EXTEST

AC EXTEST



(DC) EXTEST Results

V indicates that the Init Value is captured by the Test Receiver's JTAG flop.

| Test: driving TX+, TX- | DC Coupled Results: captured data | AC Coupled Results: captured data |
|-------------------------------|--|--|
| 00 | 00 | VV |
| 01 | 01 | VV |
| 10 | 10 | VV |
| 11 | 11 | VV |

Table 1 EXTEST Results

(DC coupling achieved by jumpers across board caps)



(DC) EXTEST Results

V indicates that the Init Value is captured by the Test Receiver's JTAG flop.

| | Test: driving TX+, TX- | DC Coupled Results: captured data | AC Coupled Results: captured data |
|---|-------------------------------|--|--|
| 1 | 00 | 00 | VV |
| 2 | 01 | 01 | VV |
| 3 | 10 | 10 | VV |
| 4 | 11 | 11 | VV |

Table 1 EXTEST Results

(DC coupling achieved by jumpers across board caps)

- **AC coupling really does block DC...**
- **1149.1 still works**



AC_EXTEST Results

Board-cap refers to on-Board AC Coupled Pairs, and Chip-cap refers to on-Chip AC Coupled Pairs

| | Driving TX+, TX- from vector_a to vector_b | Board-cap Results: captured data | Chip-cap Results: captured data |
|----|---|---|--|
| 1 | 00 to 01 | 11 | V1 |
| 2 | 00 to 10 | 11 | 1V |
| 3 | 00 to 11 | 11 | 11 |
| 4 | 01 to 00 | 00 | V0 |
| 5 | 01 to 10 | 10 | 10 |
| 6 | 01 to 11 | 11 | 1V |
| 7 | 10 to 00 | 00 | 0V |
| 8 | 10 to 01 | 01 | 01 |
| 9 | 10 to 11 | 11 | V1 |
| 10 | 11 to 00 | 00 | 00 |
| 11 | 11 to 01 | 00 | 0V |
| 12 | 11 to 10 | 00 | V0 |

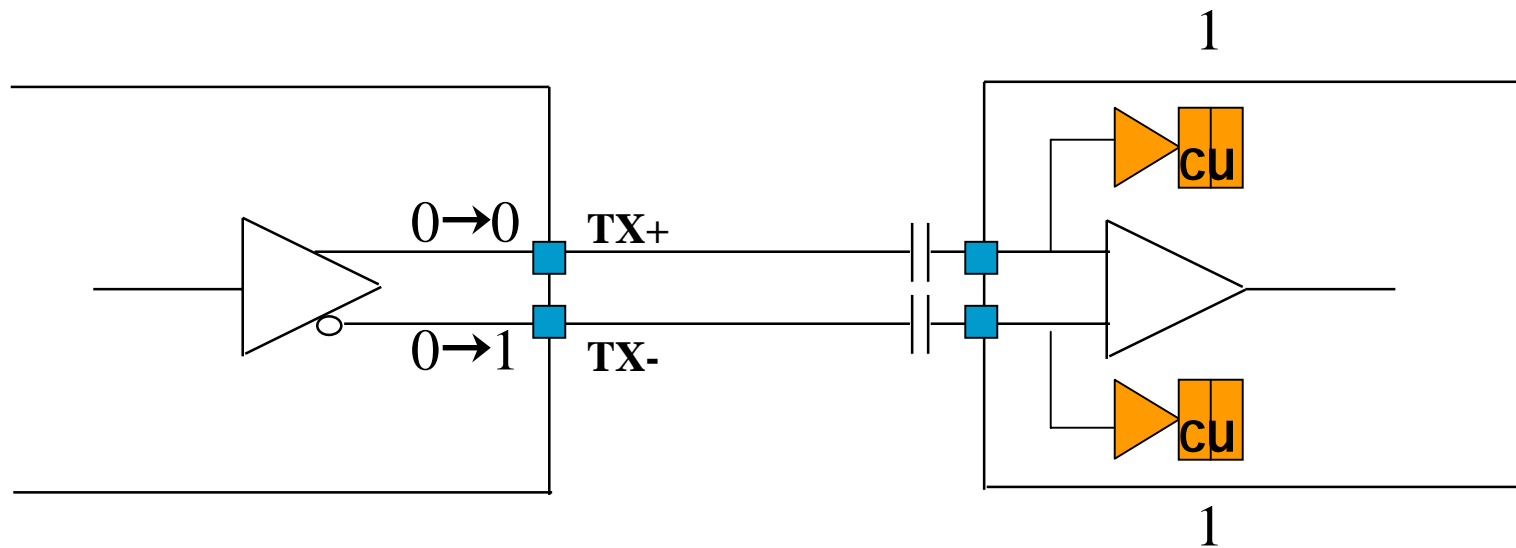
Table 2 ACExTEST Edge Detection Results

AC_EXTEST Results : how to read

Board-cap refers to on-Board AC Coupled Pairs, and Chip-cap refers to on-Chip AC Coupled Pairs

| Driving TX+,TX- from vector_a to vector_b | Board-cap Results: captured data | Chip-cap Results: captured data |
|--|-------------------------------------|------------------------------------|
| 1 00 to 01 | 11 | V1 |

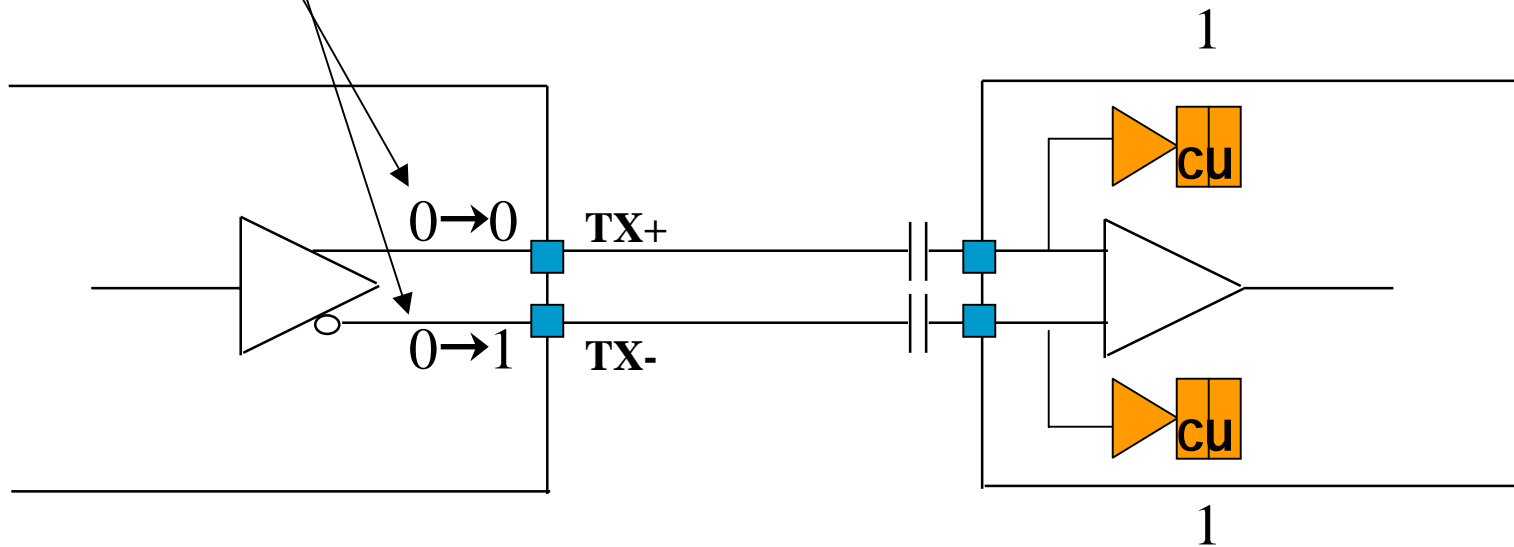
$TX_a^+TX_a^-$ to $TX_b^+TX_b^-$



AC_EXTEST Results : how to read

Board-cap refers to on-Board AC Coupled Pairs, and Chip-cap refers to on-Chip AC Coupled Pairs

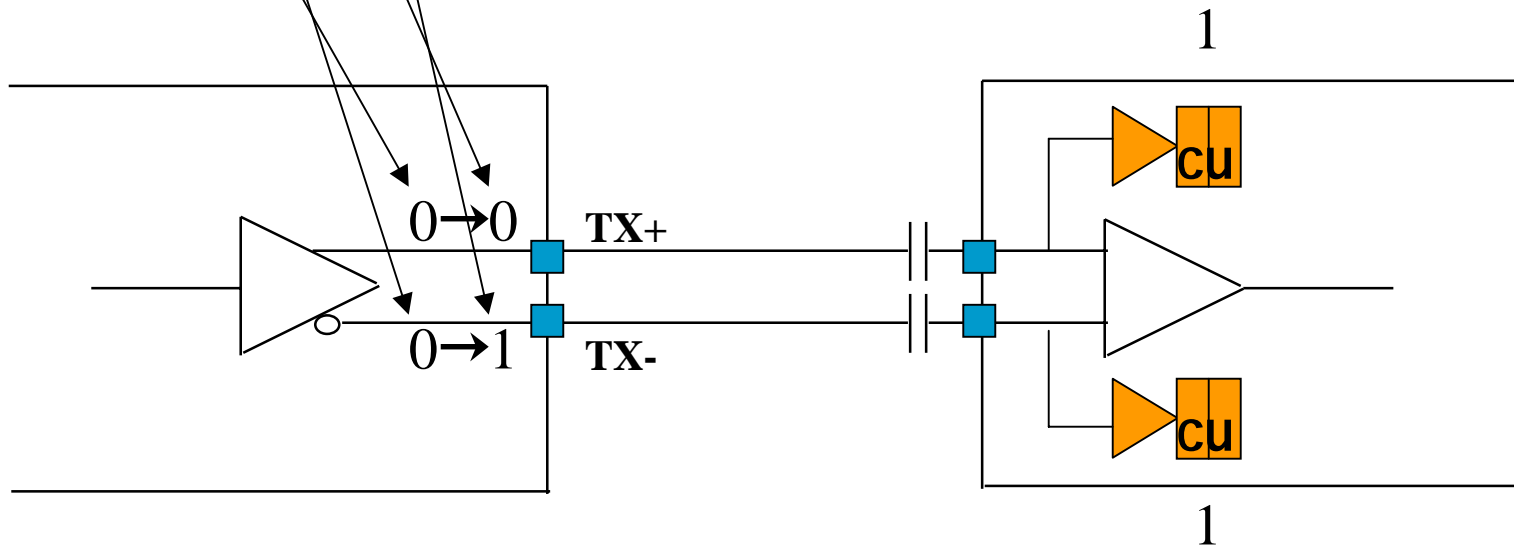
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| 00 to 01 | 11 | V1 |



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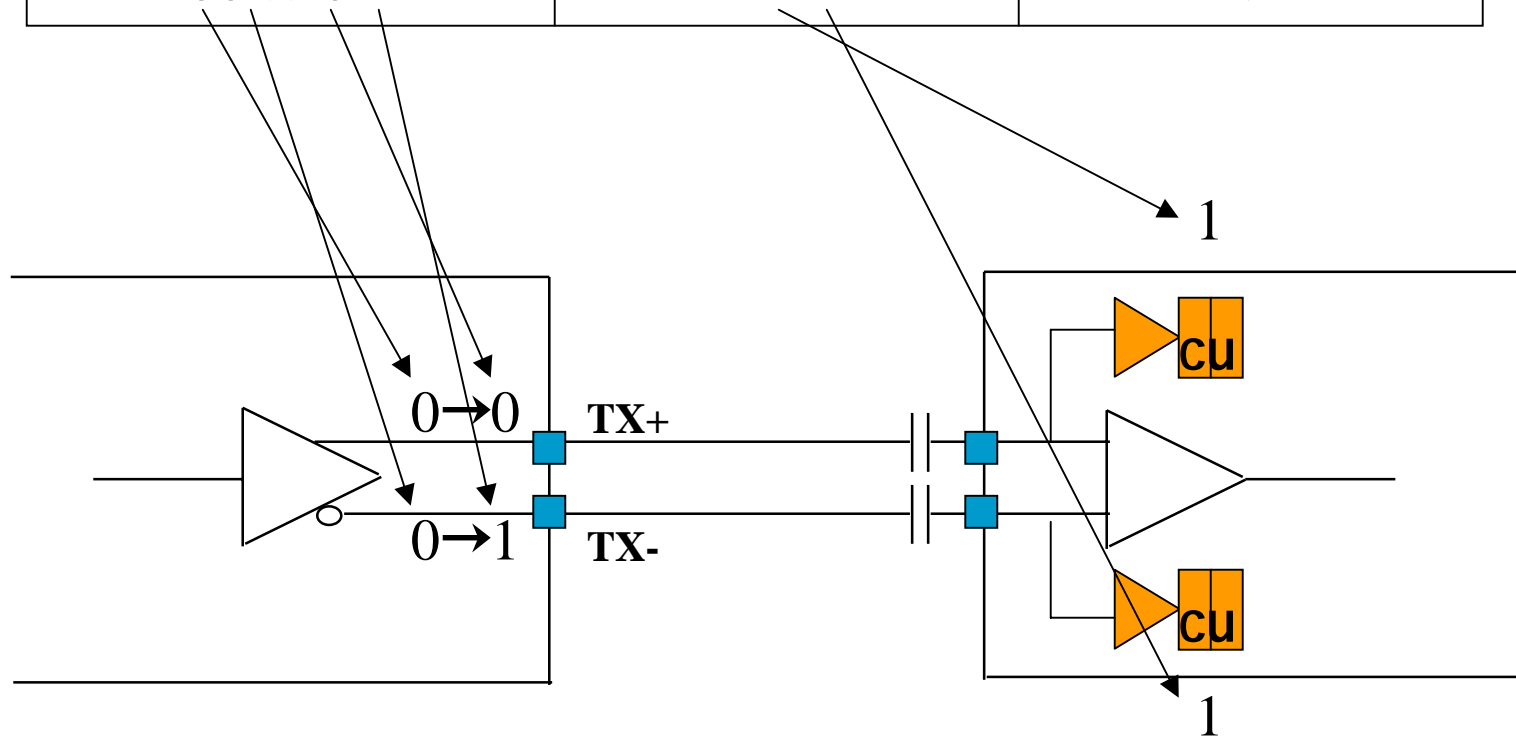
| Driving TX+,TX- from vector_a to vector_b | Board-cap Results: captured data | Chip-cap Results: captured data |
|--|-------------------------------------|------------------------------------|
| 00 to 01 | 11 | V1 |



AC_EXTEST Results : how to read

Board-cap refers to on-Board AC Coupled Pairs, and Chip-cap refers to on-Chip AC Coupled Pairs

| Driving TX+,TX- from vector_a to vector_b | Board-cap Results: captured data | Chip-cap Results: captured data |
|--|-------------------------------------|------------------------------------|
| 00 to 01 | 11 | V1 |



AC_EXTEST Results (normal operation)

Board-cap refers to on-Board AC Coupled Pairs, and Chip-cap refers to on-Chip AC Coupled Pairs

| | Driving TX+, TX- from vector_a to vector_b | Board-cap Results: captured data | Chip-cap Results: captured data |
|----|---|---|--|
| 1 | 00 to 01 | 11 | V1 |
| 2 | 00 to 10 | 11 | 1V |
| 3 | 00 to 11 | 11 | 11 |
| 4 | 01 to 00 | 00 | V0 |
| 5 | 01 to 10 | 10 | 10 |
| 6 | 01 to 11 | 11 | 1V |
| 7 | 10 to 00 | 00 | 0V |
| 8 | 10 to 01 | 01 | 01 |
| 9 | 10 to 11 | 11 | V1 |
| 10 | 11 to 00 | 00 | 00 |
| 11 | 11 to 01 | 00 | 0V |
| 12 | 11 to 10 | 00 | V0 |

Table 2 ACExTEST Edge Detection Results

AC_EXTEST Results (transitioning final values)

Board-cap refers to on-Board AC Coupled Pairs, and Chip-cap refers to on-Chip AC Coupled Pairs

| | Driving TX+, TX- from vector_a to vector_b | Board-cap Results: captured data | Chip-cap Results: captured data |
|----|--|--|---|
| 1 | 00 to 01 | 11 | V1 |
| 2 | 00 to 10 | 11 | 1V |
| 3 | 00 to 11 | 11 | 11 |
| 4 | 01 to 00 | 00 | V0 |
| 5 | 01 to 10 | 10 | 10 |
| 6 | 01 to 11 | 11 | 1V |
| 7 | 10 to 00 | 00 | 0V |
| 8 | 10 to 01 | 01 | 01 |
| 9 | 10 to 11 | 11 | V1 |
| 10 | 11 to 00 | 00 | 00 |
| 11 | 11 to 01 | 00 | 0V |
| 12 | 11 to 10 | 00 | V0 |

Table 2 AC_EXTEST Edge Detection Results

AC_EXTEST Results (transitioning final values)

Board-cap refers to on-Board AC Coupled Pairs, and Chip-cap refers to on-Chip AC Coupled Pairs

| | Driving TX+, TX- from vector_a to vector_b | Board-cap Results: captured data | Chip-cap Results: captured data |
|----|---|-------------------------------------|------------------------------------|
| 1 | 00 to 01 | 11 | V1 |
| 2 | 00 to 10 | 11 | 1V |
| 3 | 00 to 11 | 11 | 11 |
| 4 | 01 to 00 | 00 | V0 |
| 5 | 01 to 10 | 10 | 10 |
| 6 | 01 to 11 | 11 | 1V |
| 7 | 10 to 00 | 00 | 0V |
| 8 | 10 to 01 | 01 | 01 |
| 9 | 10 to 11 | 11 | V1 |
| 10 | 11 to 00 | 00 | 00 |
| 11 | 11 to 01 | 00 | 0V |
| 12 | 11 to 10 | 00 | V0 |

Table 2 ACExTEST Edge Detection Results

AC_EXTEST Results (non-transitioning final values)

Board-cap refers to on-Board AC Coupled Pairs, and Chip-cap refers to on-Chip AC Coupled Pairs

| | Driving TX+, TX- from vector_a to vector_b | Board-cap Results: captured data | Chip-cap Results: captured data |
|----|---|---|--|
| 1 | 00 to 01 | 11 | V1 |
| 2 | 00 to 10 | 11 | 1V |
| 3 | 00 to 11 | 11 | 11 |
| 4 | 01 to 00 | 00 | V0 |
| 5 | 01 to 10 | 10 | 10 |
| 6 | 01 to 11 | 11 | 1V |
| 7 | 10 to 00 | 00 | 0V |
| 8 | 10 to 01 | 01 | 01 |
| 9 | 10 to 11 | 11 | V1 |
| 10 | 11 to 00 | 00 | 00 |
| 11 | 11 to 01 | 00 | 0V |
| 12 | 11 to 10 | 00 | V0 |

Table 2 AC_EXTEST Edge Detection Results

AC_EXTEST Results (non-transitioning final values)

Board-cap refers to on-Board AC Coupled Pairs, and Chip-cap refers to on-Chip AC Coupled Pairs

| | Driving TX+, TX- from vector_a to vector_b | Board-cap Results: captured data | Chip-cap Results: captured data |
|----|---|-------------------------------------|------------------------------------|
| 1 | 00 to 01 | 11 | V1 |
| 2 | 00 to 10 | 11 | 1V |
| 3 | 00 to 11 | 11 | 11 |
| 4 | 01 to 00 | 00 | V0 |
| 5 | 01 to 10 | 10 | 10 |
| 6 | 01 to 11 | 11 | 1V |
| 7 | 10 to 00 | 00 | 0V |
| 8 | 10 to 01 | 01 | 01 |
| 9 | 10 to 11 | 11 | V1 |
| 10 | 11 to 00 | 00 | 00 |
| 11 | 11 to 01 | 00 | 0V |
| 12 | 11 to 10 | 00 | V0 |

Table 2 ACExTEST Edge Detection Results

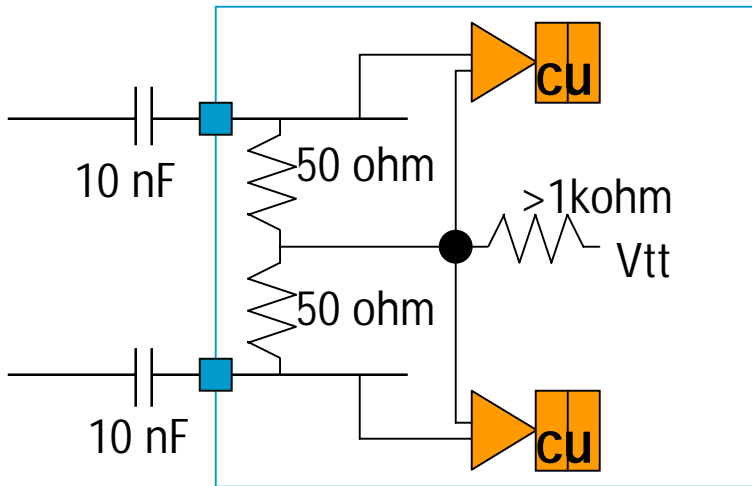
Same as mate

Retains initial value

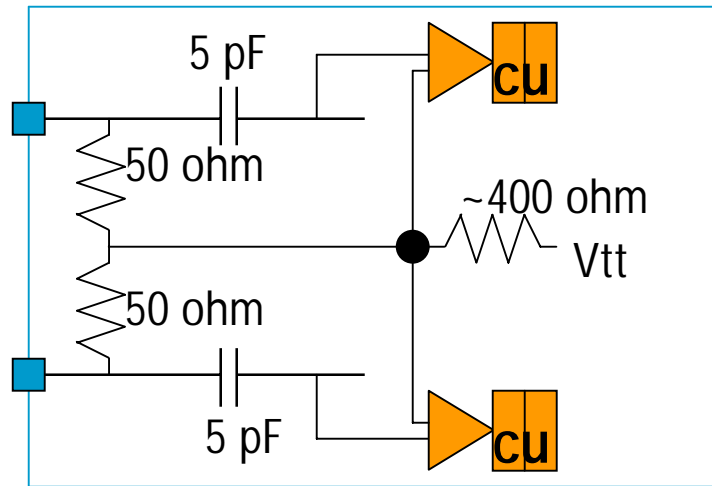


Two Termination Schemes

❑ Board AC-coupling caps

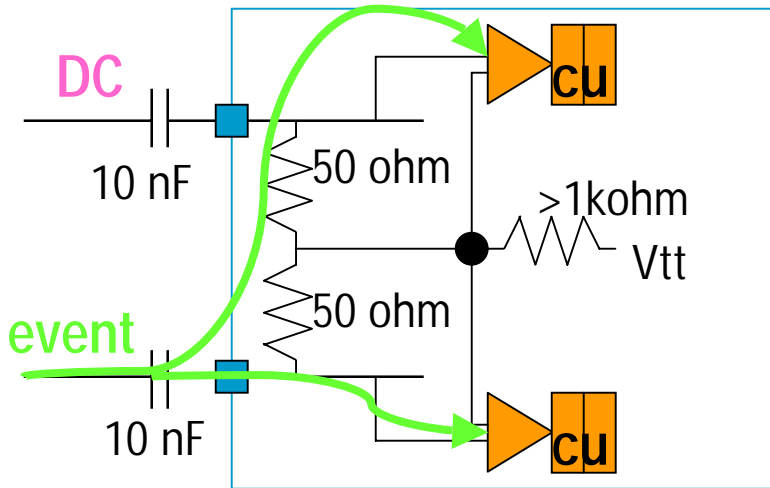


❑ On-chip AC coupling caps



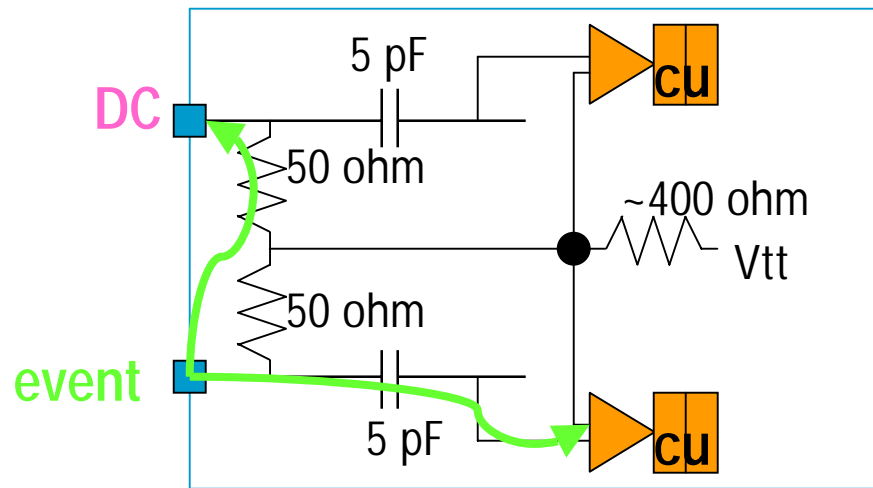
Two Termination Schemes

❑ Board AC-coupling caps



Same as mate

❑ On-chip AC coupling caps



Retains initial value

AC_EXTEST Results

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|----|--|--|---|
| 1 | 00 to 01 | 11 | V1 |
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| 3 | 00 to 11 | 11 | 11 |
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| 5 | 01 to 10 | 10 | 10 |
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| 7 | 10 to 00 | 00 | 0V |
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| 10 | 11 to 00 | 00 | 00 |
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Table 2 ACExTEST Edge Detection Results

➤ **Expected behavior in all cases: 1149.6 is functional**

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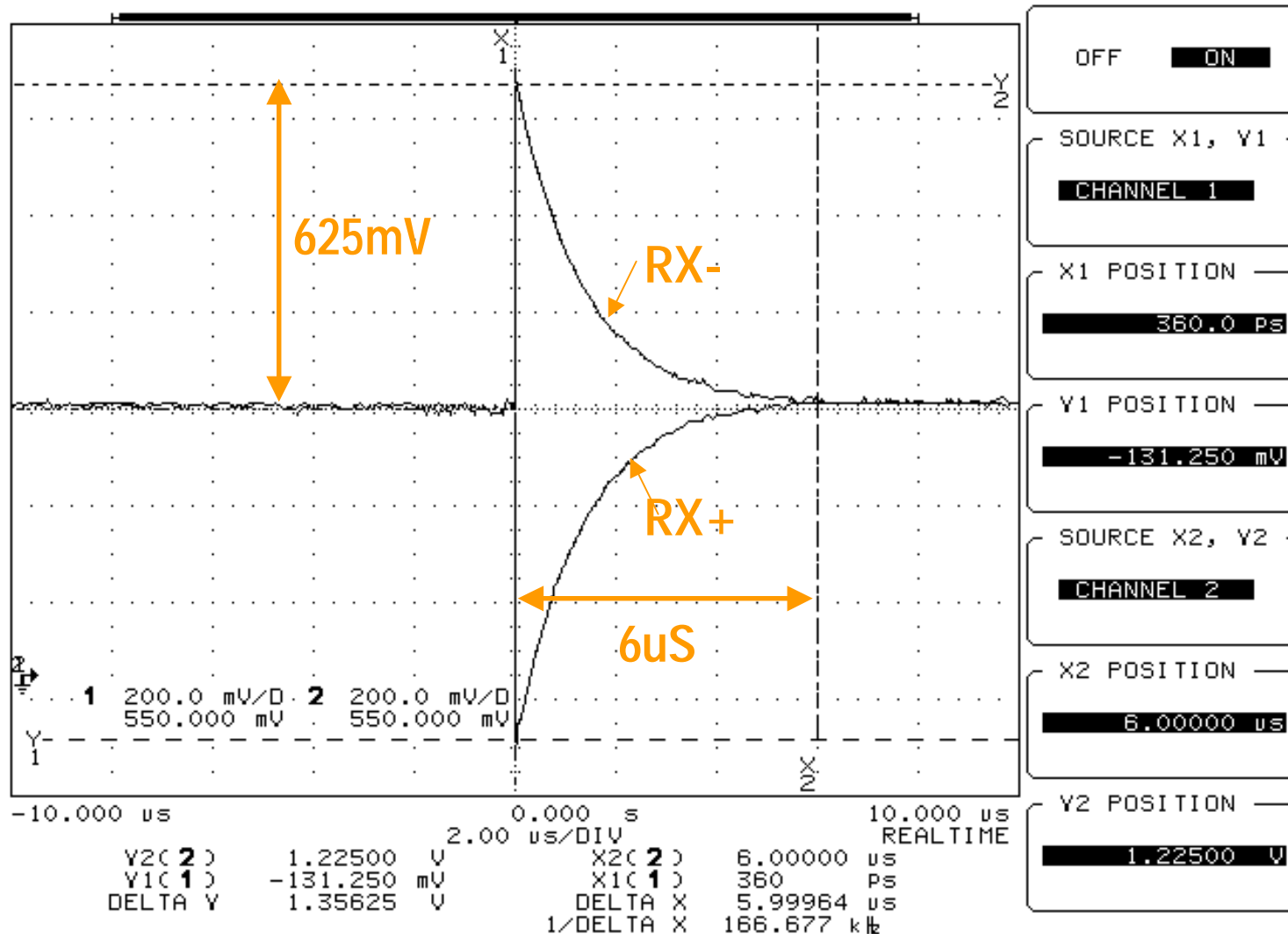
Electrical Verification Tests

- Passing edges
- Vhyst threshold measurement
- Thyst threshold measurement
- Robustness during heavy switching

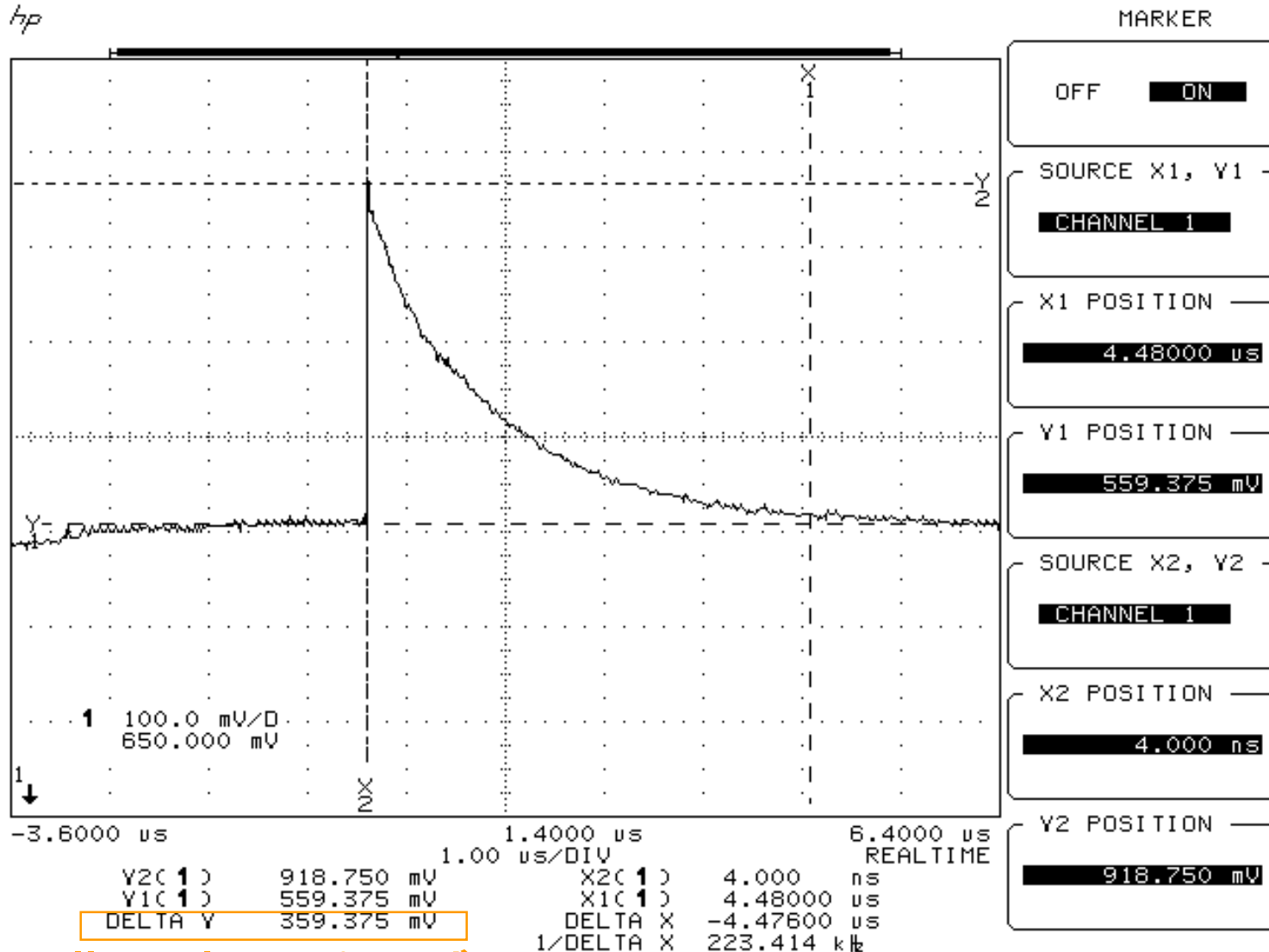


Passing Edges: RX+, RX-, board caps

hp STOPPED



Vhyst Threshold Measurement : 359 mV Captured



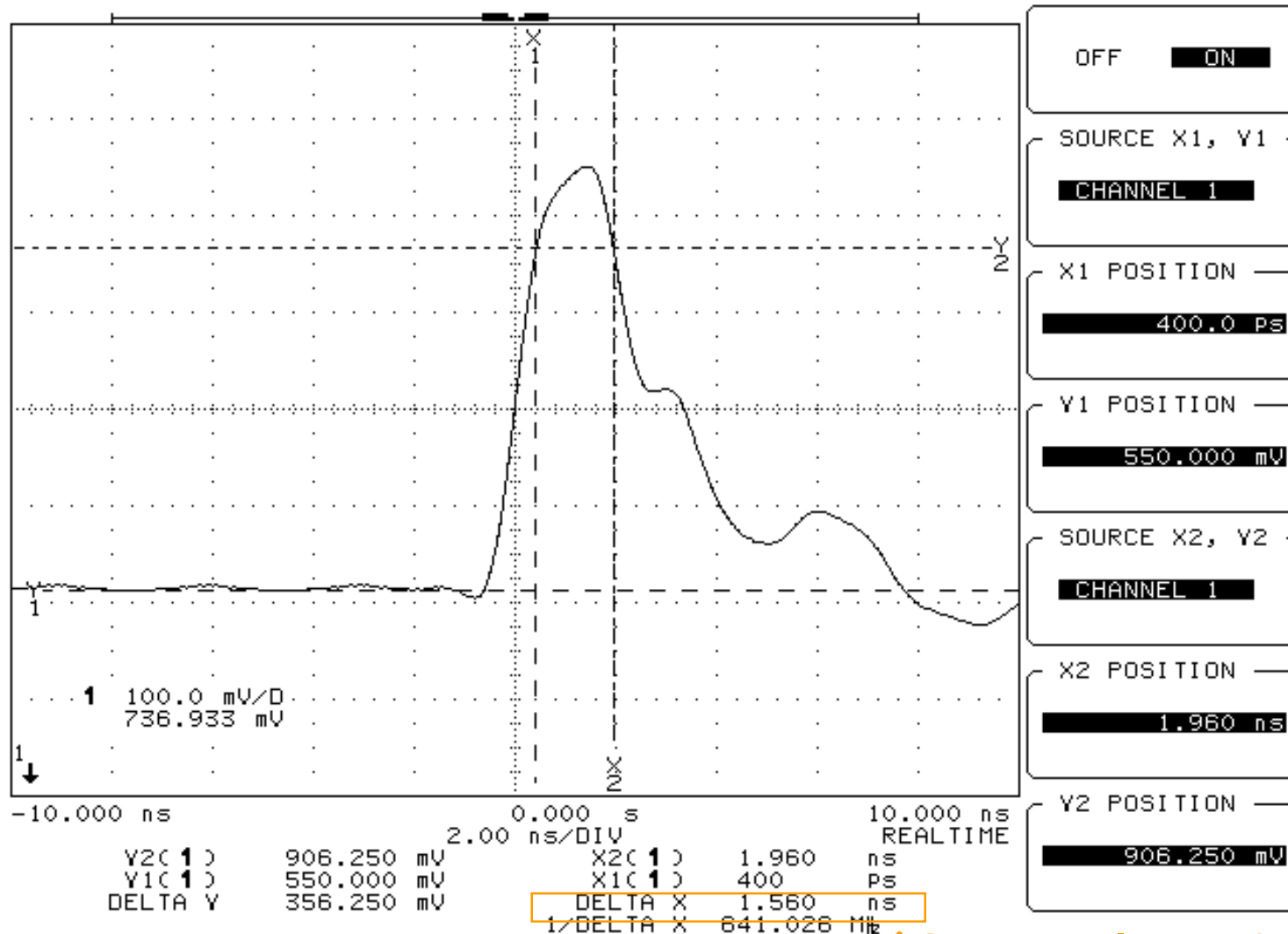
(smaller pulses rejected)



Thyristor Threshold Measurement: 1.56nS Captured

hp STOPPED

MARKER



(shorter pulses rejected)



Robustness During Heavy Switching

Table 3 EXTEST PULSE Heavy Switching Results

| Test | Reception Verified? |
|--|---------------------|
| a) hold one signal static, rest rising | CAN'T TEST * |
| b) hold one signal static, rest falling | CAN'T TEST * |
| c) drive one rising edge, rest falling | YES |
| d) drive one falling edge, rest rising | YES |
| e) drive half signals falling, half rising | YES |
| f) drive half signals rising, half falling | YES |
| g) repeat e) and f) with a log-n checkerboard sequence | YES |

* Note: All channels perform the same TAP instruction. It is not possible to perform EXTEST on some channels while performing EXTEST PULSE on others.

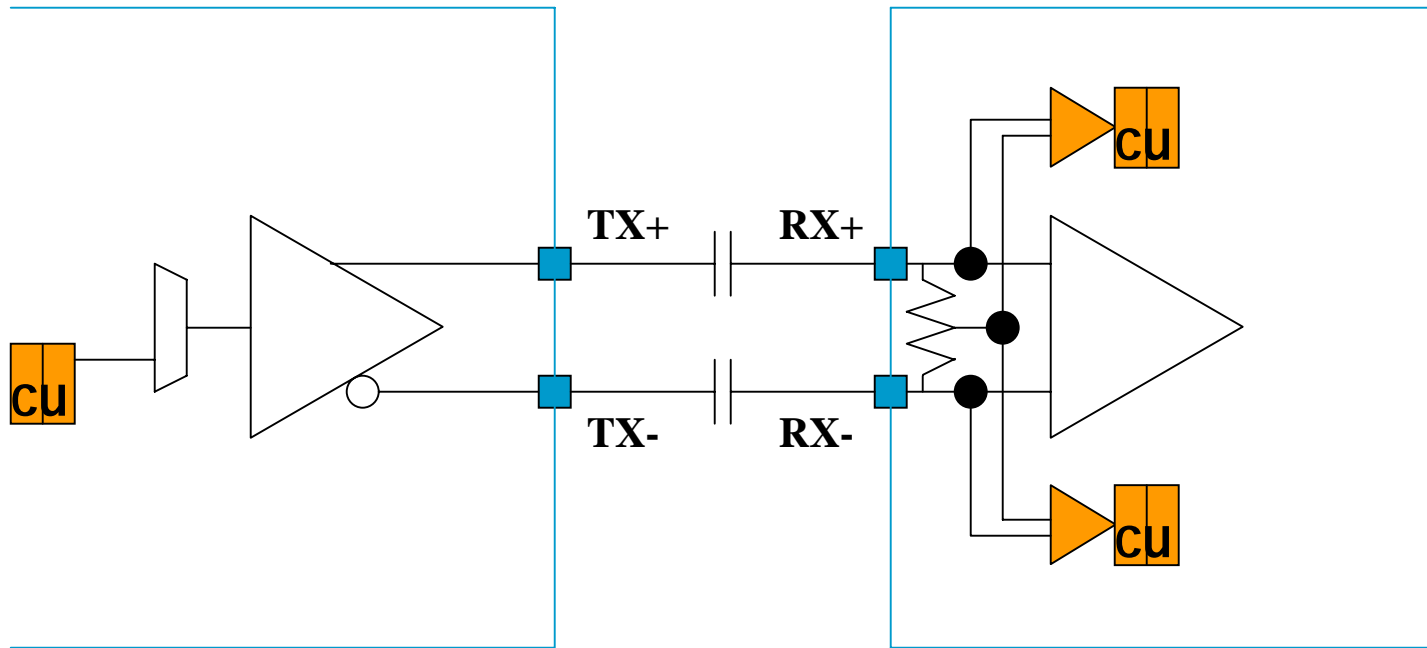


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Defect Injection points: TX+, TX-, RX+, RX-



Note: all 4 points accessible on board-cap SerDes channels;
only TX+ and TX- accessible on chip-cap channels.

Defects Injected

| Defect Injected |
|-----------------------------|
| a. TX+ open |
| b. TX+ short to TX- |
| c. TX+ short to GND |
| d. TX+ short to Vdd |
| e. TX+ short to another TX+ |
| f. TX- open |
| g. TX- short to GND |
| h. TX- short to Vdd |
| i. TX- short to another TX- |
| j. RX+ open |
| k. RX+ short to RX- |
| l. RX+ short to GND |
| m. RX+ short to Vdd |
| n. RX+ short to another RX+ |
| o. RX- open |
| p. RX- short to GND |
| q. RX- short to Vdd |
| r. RX- short to another RX- |
| s. TX+ short to RX+ |
| t. TX- short to RX- |
| u. TX+ short to RX- |
| v. TX- short to RX+ |

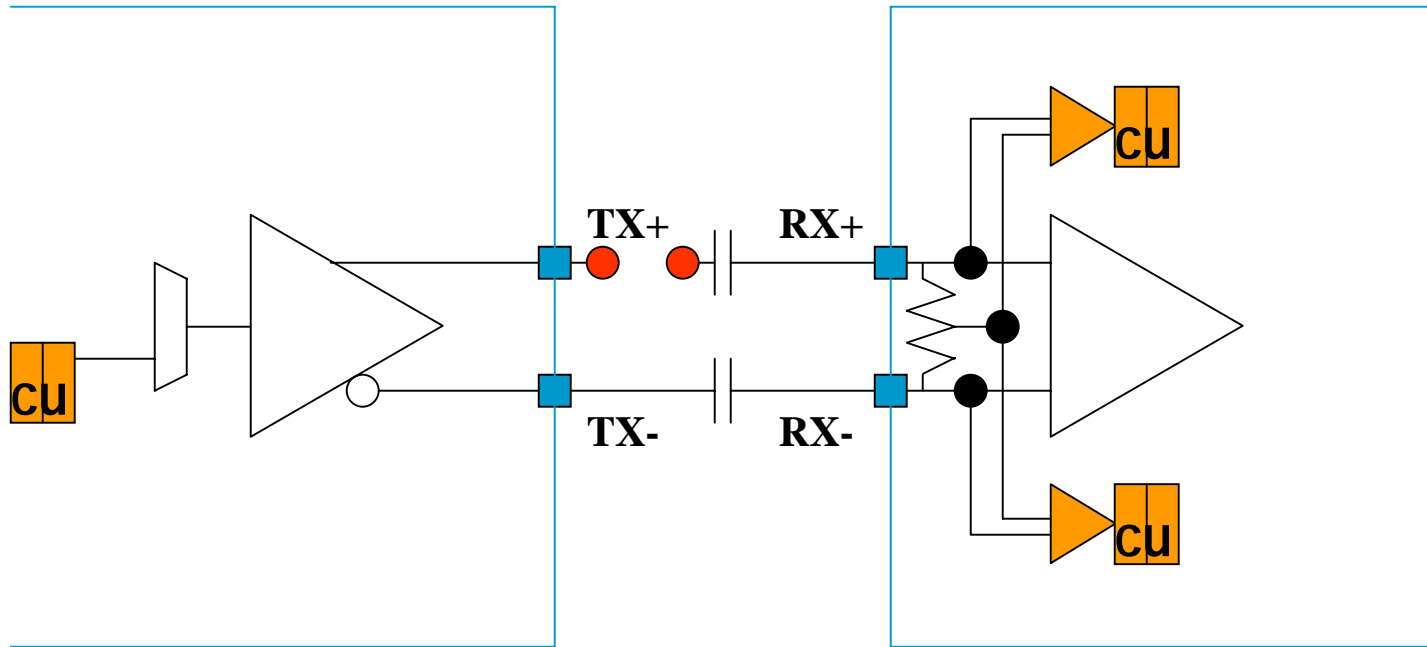


Defects Detected

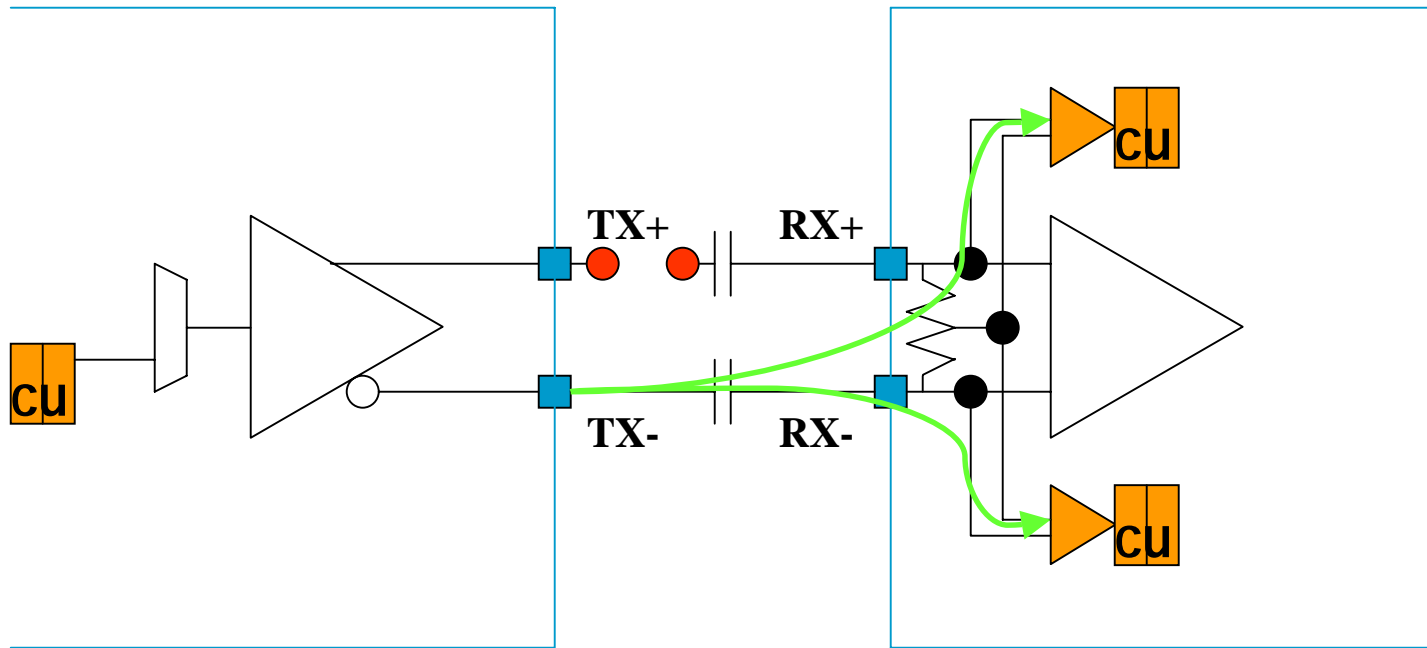
| Defect Injected | Status |
|-----------------------------|----------|
| a. TX+ open | detected |
| b. TX+ short to TX- | detected |
| c. TX+ short to GND | detected |
| d. TX+ short to Vdd | detected |
| e. TX+ short to another TX+ | detected |
| f. TX- open | detected |
| g. TX- short to GND | detected |
| h. TX- short to Vdd | detected |
| i. TX- short to another TX- | detected |
| j. RX+ open | detected |
| k. RX+ short to RX- | detected |
| l. RX+ short to GND | detected |
| m. RX+ short to Vdd | detected |
| n. RX+ short to another RX+ | detected |
| o. RX- open | detected |
| p. RX- short to GND | detected |
| q. RX- short to Vdd | detected |
| r. RX- short to another RX- | detected |
| s. TX+ short to RX+ | detected |
| t. TX- short to RX- | detected |
| u. TX+ short to RX- | detected |
| v. TX- short to RX+ | detected |



Defect a. TX+ open

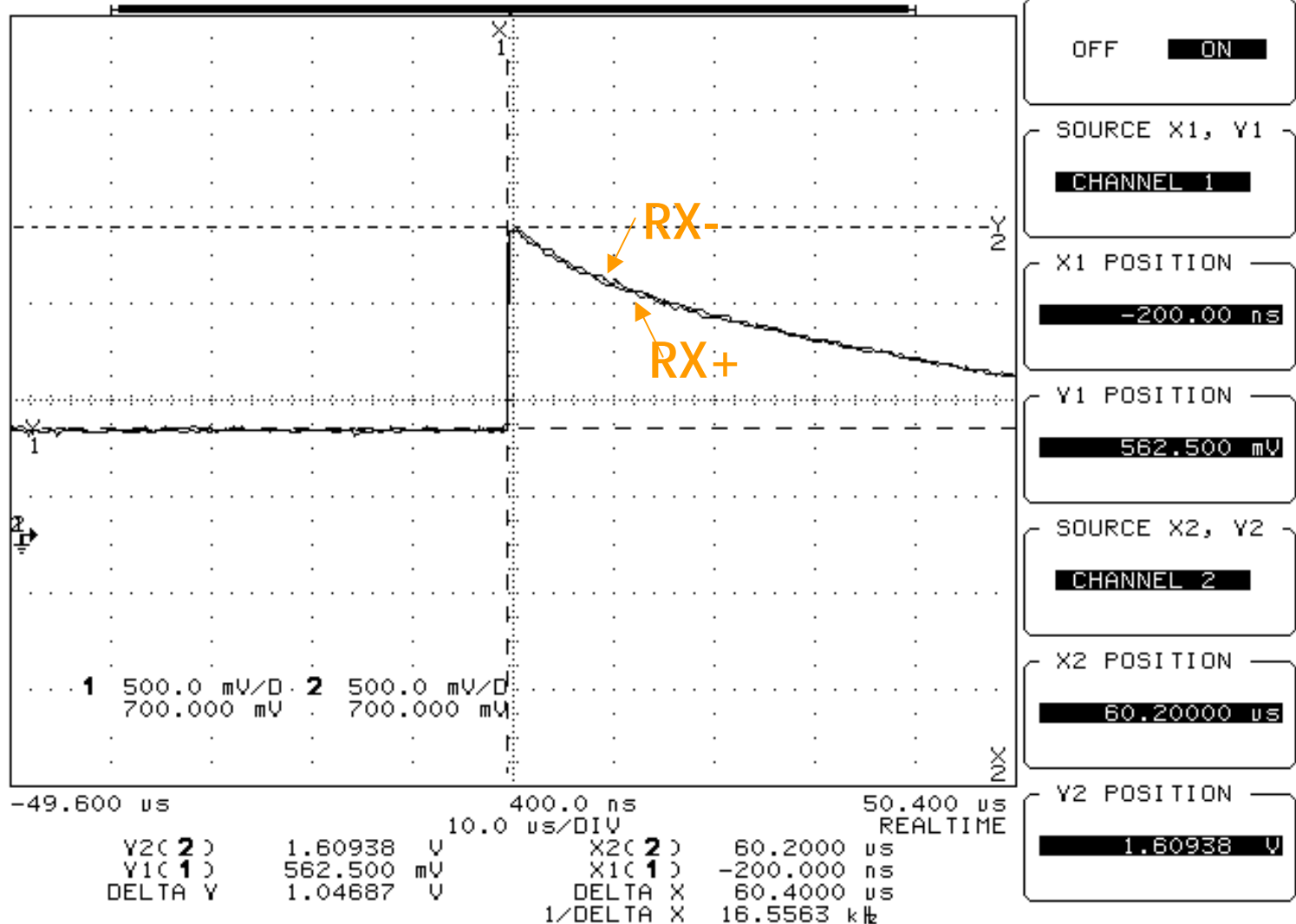


Defect a. TX+ open; Syndrome: $RX+ = RX-$

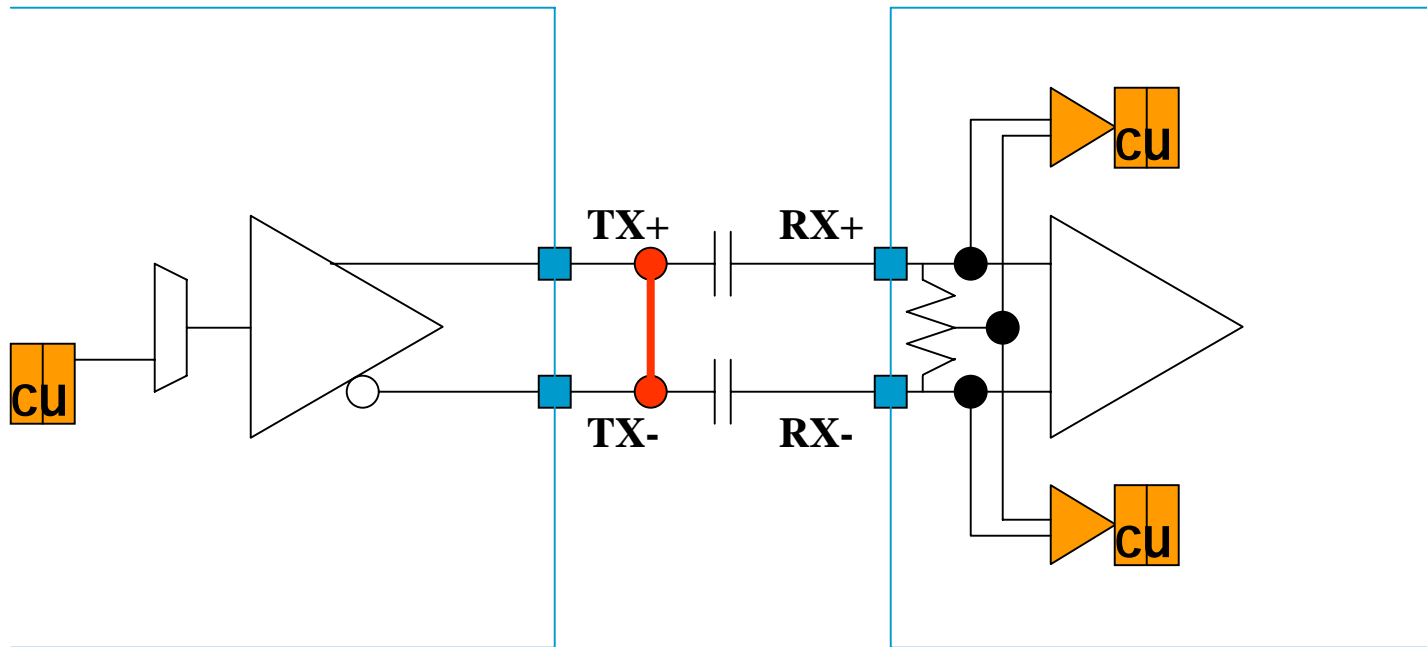


Defect a. TX+ open: Waveforms

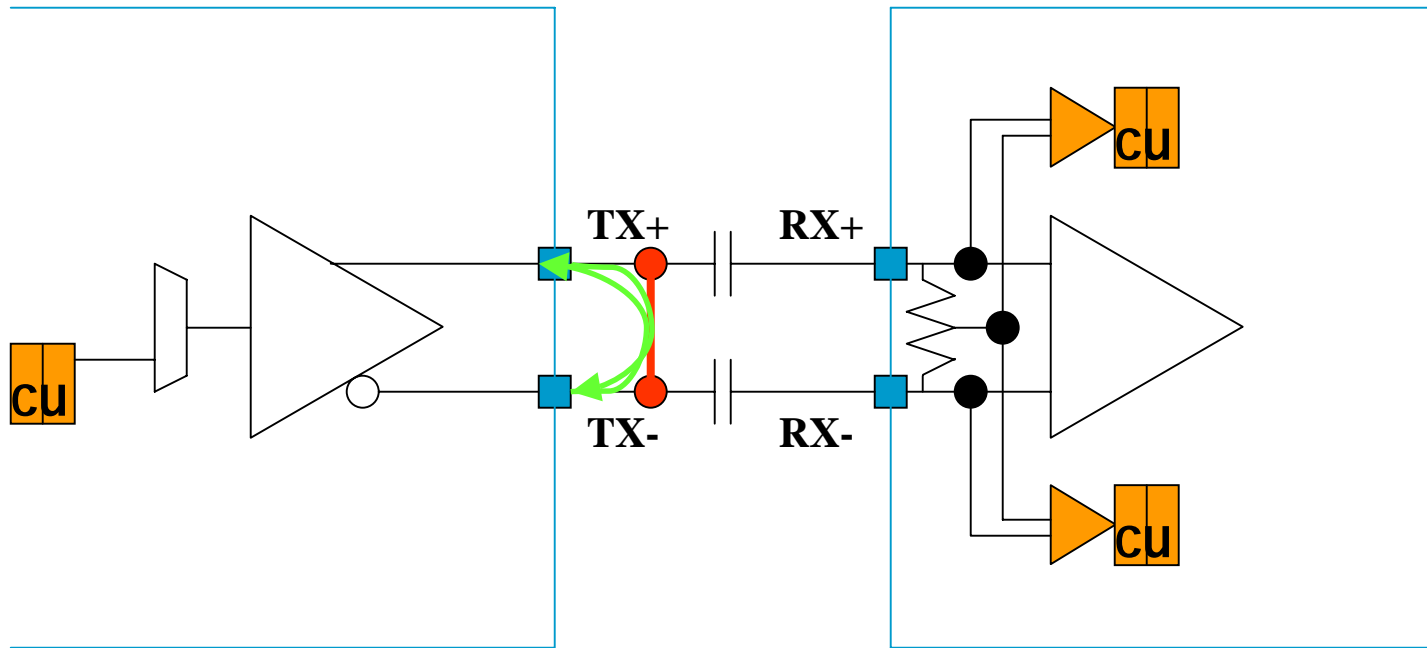
hp STOPPED



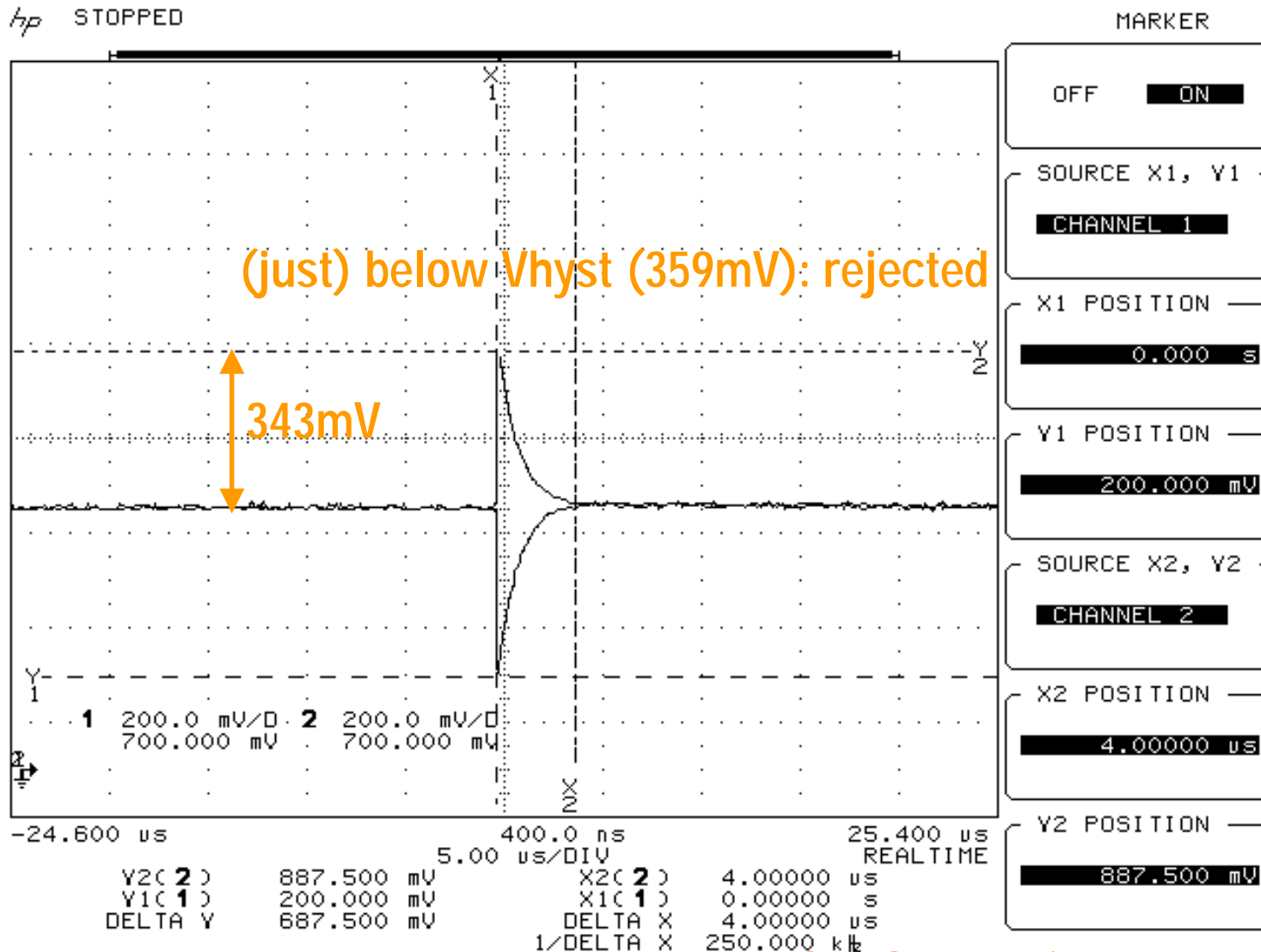
Defect b. TX+ shorted to TX-



Defect b. TX+ shorted to TX-; Syndrome: $RX^* == V$



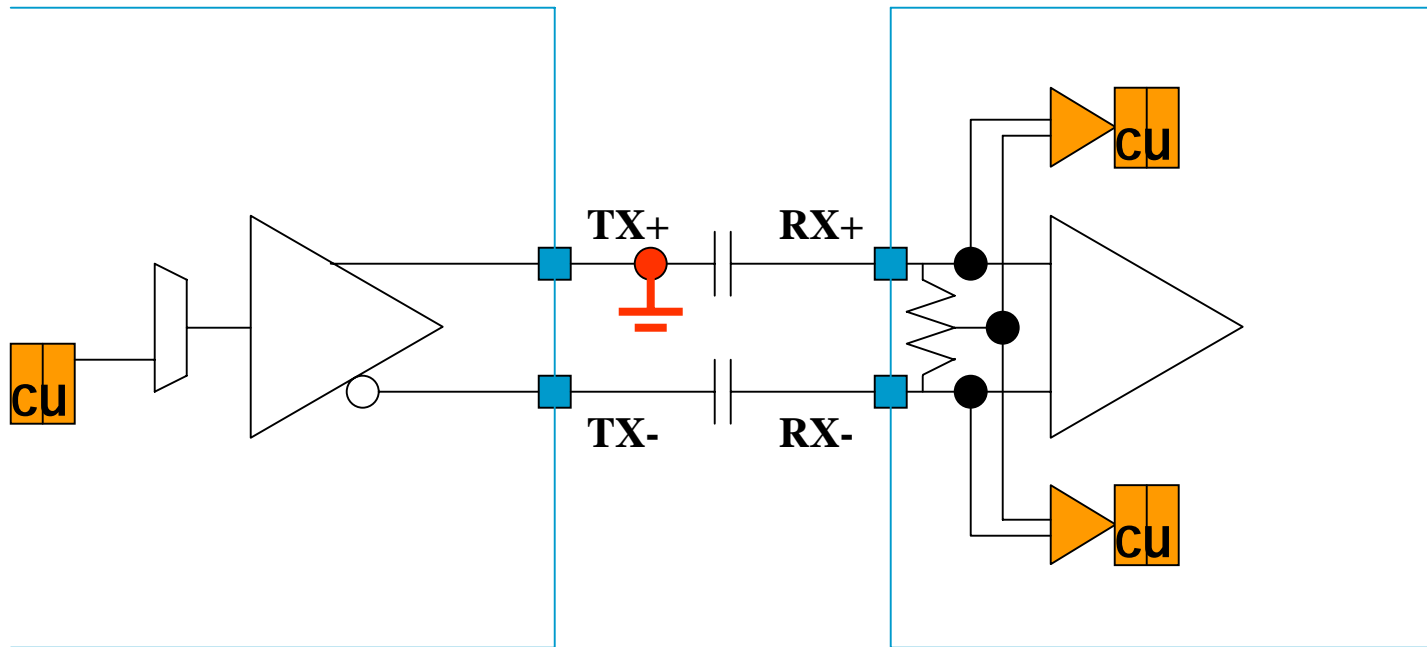
Defect b. TX+ shorted to TX-: Waveforms



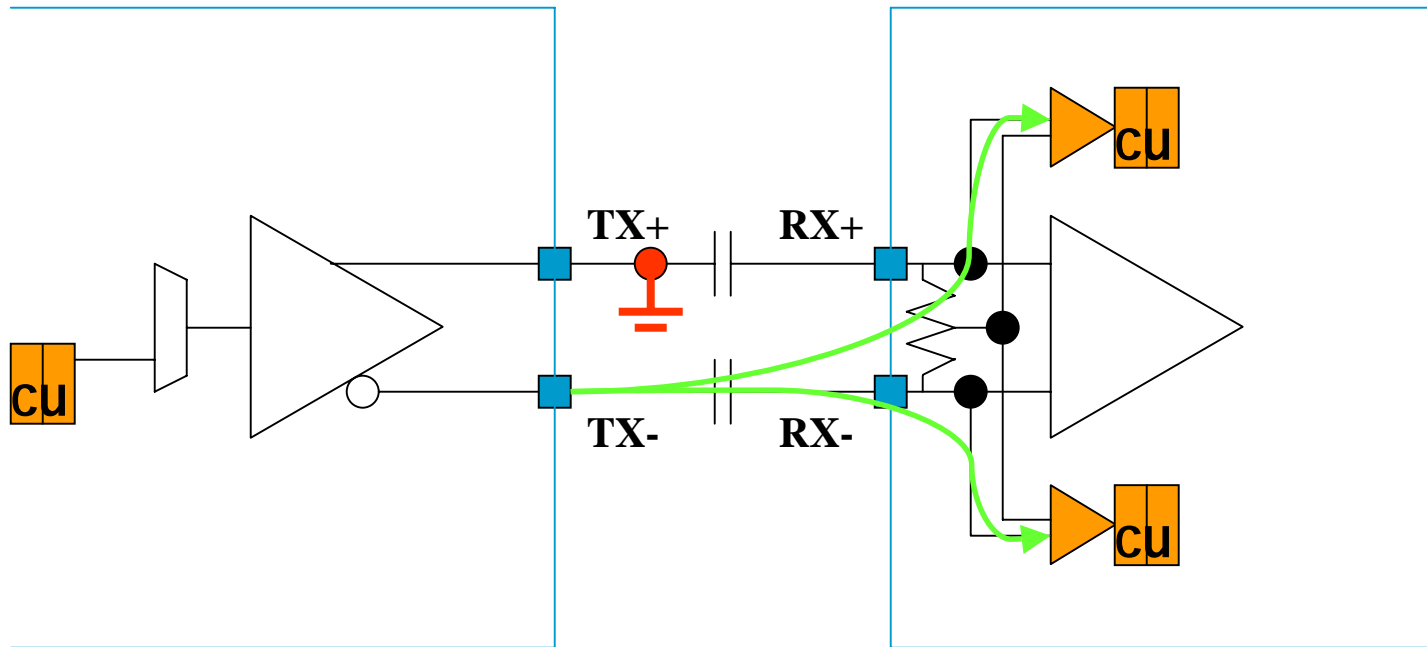
Is the short acting as a splitter?



Defect c. TX+ shorted to GND

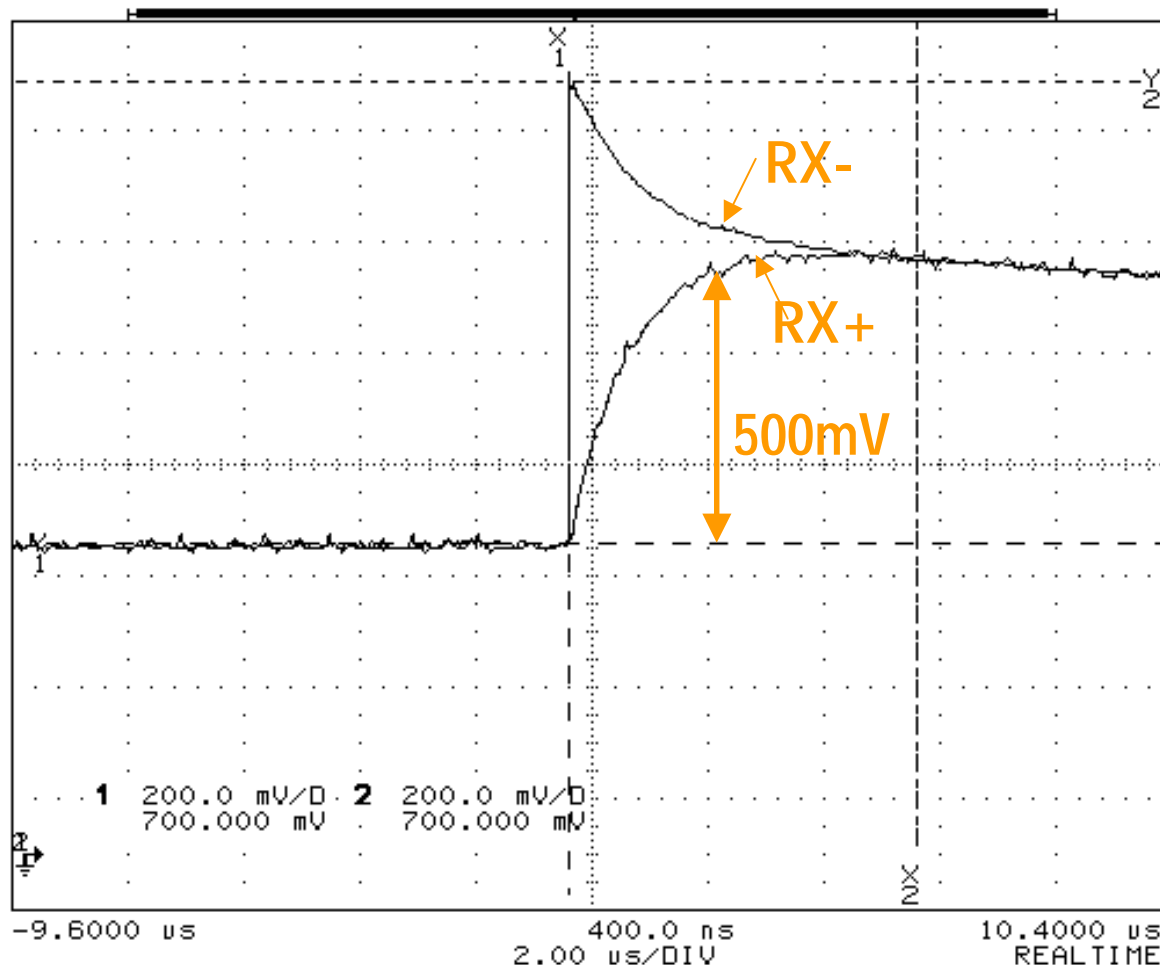


Defect c. TX+ shorted to GND; Synd.: RX+ = RX-



Defect c. TX+ shorted to GND: Waveforms

hp STOPPED



MARKER

OFF ON

SOURCE X1, Y1
CHANNEL 1

X1 POSITION
360.0 ps

Y1 POSITION
562.500 mV

SOURCE X2, Y2
CHANNEL 2

X2 POSITION
6.00000 us

Y2 POSITION
1.39375 V

RX+ is a valid edge: rise time > 1.95uS (slowest captured by TR)



Summary of Failure Syndromes

Table 3 Test Receiver Injected Defects Results

| Injected defect | Board-cap AC coupled results | Chip-cap AC coupled results | Detected? |
|-----------------------------|------------------------------|-----------------------------|-----------|
| a. TX+ open | RX+ captures RX- value | RX+ captures RX- value | Yes |
| b. TX+ short to TX- | RX+/- capture V | RX+/- capture V | Yes |
| c. TX+ short to GND | RX+ captures RX- value | RX+ captures V | Yes |
| d. TX+ short to Vdd | RX+ captures RX- value | RX+ captures V | Yes |
| e. TX+ short to another TX+ | see Table 4 | see Table 4 | Yes |
| f. TX- open | RX- captures RX+ value | RX- captures RX+ value | Yes |
| g. TX- short to GND | RX- captures RX+ value | RX- captures V | Yes |
| h. TX- short to Vdd | RX- captures RX+ value | RX- captures V | Yes |
| i. TX- short to another TX- | see Table 4 | see Table 4 | Yes |
| j. RX+ open | RX+ captures RX- value | can't test | Yes |
| k. RX+ short to RX- | RX+/- capture V | can't test | Yes |
| l. RX+ short to GND | RX+/- capture 0 | can't test | Yes |
| m. RX+ short to Vdd | RX+/- capture 1 | can't test | Yes |
| n. RX+ short to another RX+ | see Table 5 | can't test | Yes |
| o. RX- open | RX- captures RX+ value | can't test | Yes |
| p. RX- short to GND | RX+/- receive 0 | can't test | Yes |
| q. RX- short to Vdd | RX+/- receive 1 | can't test | Yes |
| r. RX- short to another RX- | see Table 5 | can't test | Yes |
| s. TX+ short to RX+ | RX+ captures RX- value | can't test | Yes |
| t. TX- short to RX- | RX- captures RX+ value | can't test | Yes |
| u. TX+ short to RX- | RX- captures RX+ value | can't test | Yes |
| v. TX- short to RX+ | RX+ captures RX- value | can't test | Yes |

TX to Another TX Short Behavior

Table 4 Results for tests e. and i. in Table 3

| TX1 +/- Transitions | TX2 +/- Transitions | e. TX+s shorted board-cap AC coupled results RX1 RX2 | e. TX+s shorted chip-cap AC coupled results RX1 RX2 | i. TX-s shorted board-cap AC coupled results RX1 RX2 | i. TX-s shorted chip-cap AC coupled results RX1 RX2 |
|------------------------|------------------------|---|--|---|--|
| 01 to 10 | 01 to 10 | 10 10 | 10 10 | 10 10 | 10 10 |
| 10 to 01 | 10 to 01 | 01 01 | 01 01 | 01 01 | 01 01 |
| 01 to 10 | 10 to 01 | 00 11 | 10 11 | 11 00 | 11 00 |
| 10 to 01 | 01 to 10 | 01 10 | 01 10 | 01 10 | 00 10 |

Asymmetry: must test both transition directions



RX to Another RX Short Behavior

Table 5 Results for tests n. and r. in Table 3

| TX1 +/- Transitions | TX2 +/- Transitions | n. RX+s shorted board-cap results | | n. RX+s shorted chip-cap * CAN'T TEST* | r. RX-s shorted board-cap results | | r. RX-s shorted chip-cap *CAN'T TEST* |
|------------------------|------------------------|---|-----|--|---|-----|---|
| | | RX1 | RX2 | | RX1 | RX2 | |
| 01 to 10 | 01 to 10 | 10 | 10 | | 10 | 10 | |
| 10 to 01 | 10 to 01 | 01 | 01 | | 01 | 01 | |
| 01 to 10 | 10 to 01 | 10 | 01 | | 11 | 01 | |
| 10 to 01 | 01 to 10 | 11 | 10 | | 01 | 11 | |

Asymmetry: must test both transition directions

Overview

- ❑ Test chip overview
- ❑ 1149.6 features implemented
- ❑ Test setup and conditions
- ❑ Test results
 - ❑ Functional verification
 - ❑ Electrical verification
 - ❑ Defect injection
- ❑ **Conclusions**



Remaining Tasks

- Margin characterization
 - Process (skew lot : fast, nominal, slow parts)
 - Voltage
 - Temperature
- More aggressive noise injection environment needed
- More realistic defect injection
- Next chip: add missing features
 - EXTEST_TRAIN instruction
 - Self-referencing (LPF) circuit if not guaranteed to be AC coupled



Summary of 1149.6 Test Chip Results

- ❑ 1149.6 is functional
 - ❑ DC EXTEST still works
 - ❑ AC EXTEST_PULSE works
 - ❑ Board-caps with post-cap termination
 - ❑ Chip-caps with pre-cap termination
- ❑ 1149.6 electrical robustness is an issue
 - ❑ Whyst and Thyst confer some noise immunity, but enough?
- ❑ 1149.6 detects all injected defects
 - ❑ Syndromes depend on termination scheme
 - ❑ Detection asymmetric; run both polarities of transitions



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