

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

Robert J. Schuelke
Carl F. Barnhart

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

Team Mission Statement

To recommended an IC level hardware implementation that is compatible with the existing IEEE1149 test standard and that enables the identification of manufacturing defects in interconnects that are differential and either AC or DC coupled or are single-ended and AC coupled

Scope of Document

The scope of this document applies to the transport layer of the IC that would generate and recover the test signals, the encoding of the information into and out of the scan chain, and to how the AC test mode would interact with the TAP

References

IEEE 1149 Spec

Etc.

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

1 Introduction

Background and problem statement

Evaluate caps on and off-chip

2 Defects and Fault Models

2.1 Defects

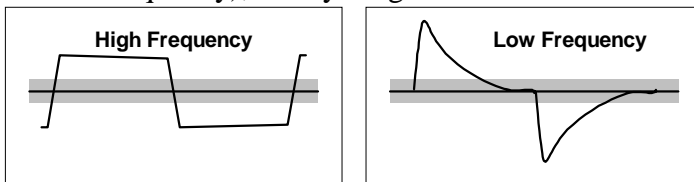
Reference “official” defect list

2.2 Fault and Fault Syndrome Descriptions.

This document describes, to the current level of our understanding, the faults and fault syndromes expected for the defects enumerated by the Board Tiger Team. It will be updated with simulation results as they become available.

2.2.1 Definitions (and assumptions):

- An AC-coupled differential **signal** consists of two **legs**, each leg consisting of two **nets** connected by a capacitor, the first from the driver to the capacitor (Tx), the second from the capacitor to the receiver (Rx).
- A DC-coupled differential **signal** consists of two **legs**, each leg consisting of a single **net** connecting driver to receiver (TxRx).
- **Transition:** when the receiver input voltage traverses a "normal" voltage swing with a "normal" slew rate, in either direction, at the time of the corresponding transition in the driving signal. The transition may be centered on a level established by a receiver bias circuit, referenced termination, driver output, or short to a voltage source, which may range from Vdd to Gnd, and may be changing slowly. The transitions may be the edges of a square wave (DC-coupled or high frequency) or pulses decaying to a float (AC-coupled and low frequency), or anything in between.



- **Float:** receiver net (Rx) is undriven in an AC sense, and there are no detectable transitions other than noise (which may be significant at the normal transition times). The level may be set by any receiver bias circuit, referenced termination, driver output, or short to a voltage source, and may be any value from Vdd to Gnd, and may be changing slowly.
- **Null:** both receiver inputs (Rx+ and Rx-) have transitions that track each other instead of being opposite polarity, as if driven from the same source.
- **Referenced Termination:** center tapped termination (usually two 50 ohm resistors), with the center tap taken to a low impedance reference voltage (Vref, Vcom, Vtt, or other names). Low impedance source implies that values on one leg will not be significantly affected by the values on other legs or signals sharing the same reference voltage.

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

- **Un-referenced Termination:** single (usually 100 ohms) resistor between the receiver inputs.
- **High Frequency:** Cycle time much less than leg RC time constant. This results in transitions that are effectively square waves.
- **Low Frequency:** Cycle time much greater than leg RC time constant. This results in transitions that are essentially pulses decaying to the float condition.
- **Bias:** A high impedance voltage source ($> 1\text{Kohm}$) imposed on differential receiver inputs, usually to permit a disconnected link to report a predetermined value. It has negligible affect on the value of a net driven by a direct connection to an active driver..

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

2.2.2 AC-Coupled Fault Summary.

In the Board Tiger Team defect list, indistinguishable defects were listed as faults. This is a summary of the faults that they listed, cross-checked against the Cisco simulation fault model and list. All faults are for an AC-coupled differential net. Terminology is based on the Board Tiger Team document, and the number in parenthesis is the number of faults where I have grouped them:

Leg1+/- Open (2)

Tx1+ shorted to: Other (9), Rail (3), Rx1-, Tx1-, Rx1+

Rx1+ shorted to: Other (9), Rail (3), Rx1-, Tx1-

Tx1- shorted to: Other (9), Rail (3), Rx1-

Rx1- shorted to: Other (9), Rail (3)

Where Rail (3) represents Rail+, Rail-, and Rail? (Rail? needs to be added to the Board Tiger Team document, and represents some intermediate voltage source.)

And where Other (9) represents:

other AC-differential signals Tx2+, Rx2+, Tx2-, and Rx2-;

other DC-differential signals TxRx3+, TxRx3-;

other AC-single-ended signals Tx4, Rx4; and

other DC-single-ended signal TxRx5.

The Board Tiger Team document also listed as a fault the case where an open in a leg combined with an un-referenced termination causes the signals on the two receiver inputs to follow each other (Cisco "null"). This is a syndrome rather than a fault, so will be dealt with below and is not included in the above list.

This gives a total of 56 simulatable and distinguishable faults.

If I use symmetry to eliminate faults on the minus leg that should give symmetrical simulation results to faults on the positive leg (dropping the Tx1- and Rx1- shorts, plus Leg1- open), then we have 30 remaining faults to simulate or otherwise determine the fault syndrome, considering both un-referenced and referenced termination schemes in each case.

Over half of these (18) are the shorts to "other", which could lead to a lot of simulation since each of these could be spawned off into variations of technology and I/O protocol for each "other". But we should run enough simulations to make sure we are not missing any new syndromes.

The Board Tiger Team did not include the termination resistor open or missing defects (Res1+/- open). The board team discounted these, saying that this would not be detected in normal 1149.1 single-ended testing. Since these terminators are required, the situation is analogous to the 1149.1 open-drain type output where the termination is required, and there is a reasonable probability of detecting that it is open or missing. These defects will be listed here to determine if there is a detectable syndrome.

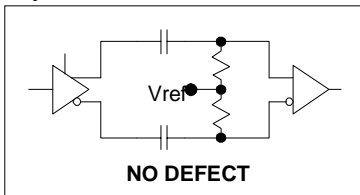
AC_EXTTEST CHIPS TIGER TEAM RECOMMENDATIONS

2.2.3 AC-Coupled Fault Syndrome Analysis

This lists the expected syndrome for each of the faults in the above list, all for the AC-coupled case. We assume steady state (power-up initial conditions have died out.) These were checked against the Cisco simulations posted, and the Cisco simulation figure number is listed where it exists.

2.2.3.1 No Defect

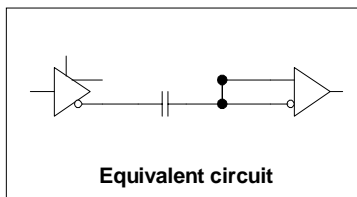
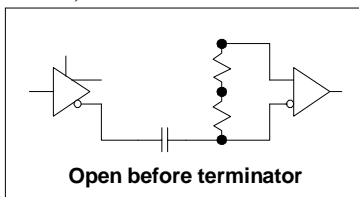
For high frequency, any termination, both receiver inputs see signals similar to a DC coupled differential signal, essentially square waves, out of phase. For low frequency, any termination, each receiver sees a pulse, of opposite polarity, approximately equal in amplitude to the normal swing of the signal, that decays to a float condition at the receiver V_{ref} , if any, or bias, if any. Thus the syndrome is transitions on both legs, correctly out of phase, for any frequency and for any termination.



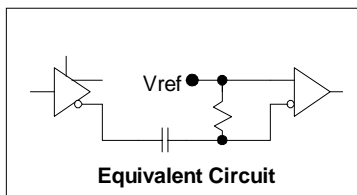
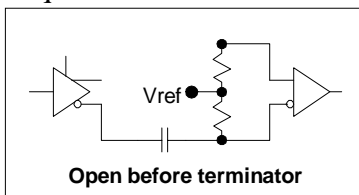
2.2.3.2 Open Leg

(See Cisco Figures 3.2-3.5 for un-referenced termination and high frequency.)

- An open in a leg, other than between the terminator and the receiver, with un-referenced termination, for any frequency, gives the null condition (the two receiver inputs track each other.)

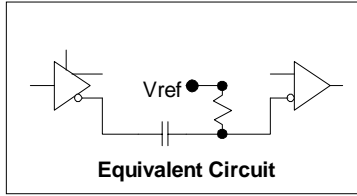
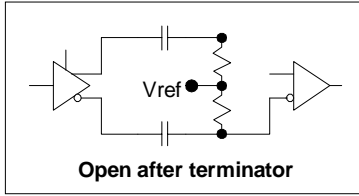


- For referenced termination, any frequency, the receiver input on the open leg floats at V_{ref} , and the receiver on the other leg gets good transitions, with a decay to V_{ref} at low frequencies.



AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

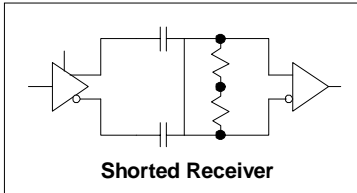
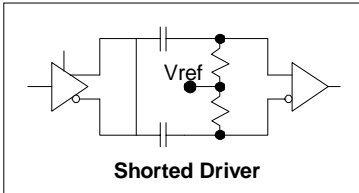
- For an open between the terminator and the receiver input, any termination, any frequency, the receiver input on the open leg gets a float at the bias level, if any, and the other receiver input gets transitions, with a decay to V_{ref} at low frequencies. (This defect need not be considered for on-chip termination resistors.)



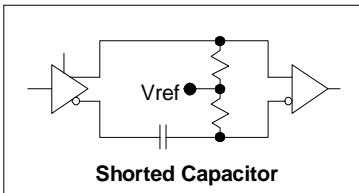
2.2.3.3 Shorts within the signal

Note: this assumes the driver and receiver are sufficiently compatible that they could be DC-coupled and still work, even if not optimally. If the driver and receiver are totally incompatible, then these defects fall under the "shorted to rail" category and discussion.

- Shorted driver ($Tx1+ \leftrightarrow Tx1-$) or receiver ($Rx1+ \leftrightarrow Rx1-$), any frequency, any termination, both receiver inputs get a float with possibly significant glitches at transition points. (Cisco Figures 3.8, 3.9 for high frequency, un-referenced termination).



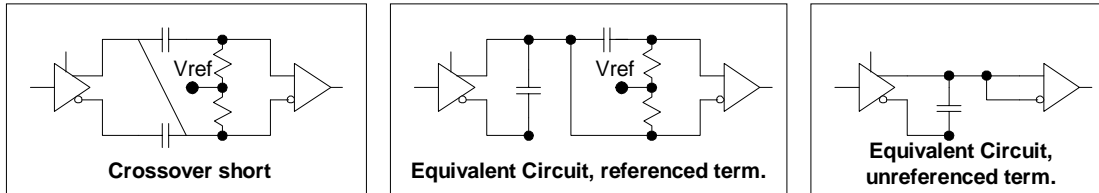
- Shorted cap on a single leg, $Tx1+ \leftrightarrow Rx1+$ or $Tx1- \leftrightarrow Rx1-$ (Note, this defect should be detectable in DC EXTEST, if there is a referenced termination or a receiver bias. This defect need not be considered if the coupling capacitors are on chip.)



- high frequency, any termination, gives apparently normal transitions at both receiver inputs.
- low frequency, un-referenced termination ($V_{ref} = 'Z'$, in diagram), the receiver input on the shorted leg gets apparently good transitions which do not decay to a float, and the receiver input on the good leg gets a good transition which decays to a null condition at the driven level on the shorted leg.

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

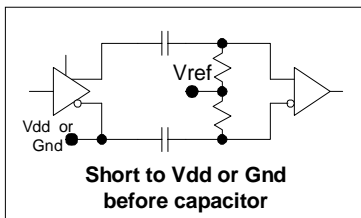
- low frequency, referenced termination, the receiver input on the shorted leg gets good transitions which do not decay to a float, and the receiver input on the good leg gets good transitions which decay to a float condition at V_{ref} .
- Short from before cap of one leg to after cap of other leg, $Tx1+ \leftrightarrow Rx1-$ or $Tx1- \leftrightarrow Rx1+$ (Note, this defect should be detectable in DC EXTEST, if there is a referenced termination or a receiver bias. This defect need not be considered if the coupling capacitors are on chip.)



- high frequency, any termination, both receiver inputs get a float with possibly significant glitches at transitions. (The glitches are apparently due to charging and discharging the capacitor across the driver outputs.) (Cisco figures 3.6, 3.7)
- low frequency, un-referenced (and bypass referenced) termination ($V_{ref} = 'Z'$ in diagram), both receiver inputs get a null with significant glitches at the transition, with the voltage decaying from the previous driven value to the new driven voltage of the shorted driver net.
- low frequency, referenced termination ($V_{ref} = V_{tt}$ in diagrams), both receiver inputs get significant glitches at transition times, and the receiver input not connected to the shorted receiver net gets a slower, flatter than normal transition decaying to a float at V_{ref} , and the other receiver input gets a voltage decaying from the previous driven value to the new driven voltage of the shorted driver net.

2.2.3.4 Shorts to Rails (+, -, V_{ref})

- Short to Gnd or Vdd, before coupling capacitor, $Tx1+ \leftrightarrow Rail+$, $Tx1- \leftrightarrow Rail+$, $Tx1+ \leftrightarrow Rail-$, or $Tx1- \leftrightarrow Rail-$,



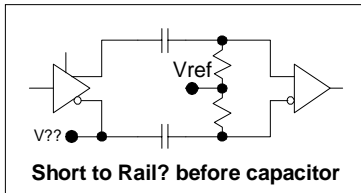
- any frequency, un-referenced termination ($V_{ref} = 'Z'$ in diagram), the receiver input on the unshorted leg should get transitions, but the other receiver input could see different conditions depending on frequency and on the technology and I/O

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

protocol used. There may or may not be signal voltage crossover at the two receivers.

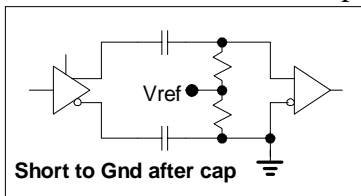
Note: In the Cisco simulations (figure 3.10, 3.11.2, 3.14, 3.15.2), the short on one driver output severely affected the DC level of the other output. Also, the "initial condition transition" of these simulations did not have time to wear off, and was swamping many of the results.

- high frequency, referenced termination, the receiver input on the unshorted leg gets transitions, and the receiver input on the shorted leg gets a float at V_{ref} .
- low frequency, referenced termination, the receiver input on the unshorted leg gets transition pulses decaying to a float at V_{ref} , and the receiver input on the shorted leg gets a float at V_{ref} .
- Short to V_{ref} or other intermediate voltage, before the coupling capacitor, $Tx1+ \leftrightarrow Rail?$ Or $Tx1- \leftrightarrow Rail?$, any termination, any frequency, the receiver input on the shorted leg gets a float at V_{ref} , and the receiver input on the unshorted leg gets transitions around the receiver V_{ref} .



Note: In the Cisco simulations (figures 3.11.1 and 3.15.1), the short to V_{ref} had no discernable effect. This implies relatively high impedance for V_{ref} , we think.

- Short to Gnd, after the coupling capacitor, $Rx1+ \leftrightarrow Rail-$ or $Rx1- \leftrightarrow Rail-$,



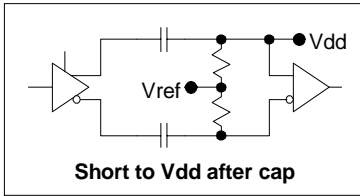
- any frequency, un-referenced termination ($V_{ref}='Z'$ in diagram): the receiver input on the shorted net gets a float at $Rail-$, and the receiver input on the other net gets transitions around $Rail-$.

Note: the Cisco simulations (3.12, 3.16) seemed to be swamped by initial conditions.

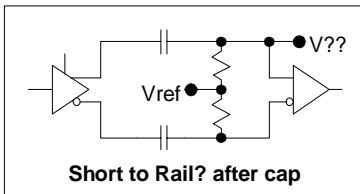
- any frequency, referenced termination; the receiver input on the shorted net gets a float at $Rail-$, and the receiver input on the other net gets transitions around V_{ref} .

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

- Short to Rail+, after the coupling capacitor, $R_{x1+} \leftrightarrow \text{Rail+}$ or $R_{x1-} \leftrightarrow \text{Rail+}$,



- any frequency, un-referenced termination ($V_{\text{ref}} = 'Z'$ in diagram) (Cisco figures 3.13.2, 3.17.2), the receiver input on the shorted net gets a float at Rail+, and the receiver input on the other net gets transitions around Rail+.
 - any frequency, referenced termination, the receiver input on the shorted net gets a float at Rail+, and the receiver input on the other net gets transitions around Vref.
- Short to Vref or other intermediate voltage, after the coupling capacitor, $R_{x1+} \leftrightarrow \text{Rail?}$ Or $R_{x1-} \leftrightarrow \text{Rail?}$,



- any frequency, un-referenced termination ($V_{\text{ref}} = 'Z'$ in diagram) (Cisco figures 3.13.1, 3.17.1), the receiver input on the shorted net gets a float at Rail?, and the receiver input on the other net gets transitions around Rail?.
- any frequency, referenced termination, the receiver input on the shorted net gets a float at Rail?, and the receiver input on the other net gets transitions around Vref.

2.2.3.5 Shorts to "other" nets, DC or AC coupled, single-ended or differential.

This category has too many possibilities to enumerate them, but we make the following observations:

- Shorts to a typical CMOS driver will look like a resistive short to a rail. The resistance is within a small factor of the differential termination resistance. So the discussions of shorts to a rail may apply here.
- There are single-ended (and possibly AC-coupled) I/O protocols that have small voltage swings and require a Vref: HSTL, SSTL, and GTL, for instance. These would appear the same as a short to another differential net.

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

- If two nets of two different differential drivers are shorted, before the cap, then, as today, relative common mode voltages, strengths, etc will determine the results.
- If two nets of two different differential ac-coupled receivers are shorted, then the results will depend on termination, bias, phase, etc.
- If a driver is shorted to the receiver net of an AC-coupled signal, results will depend on the voltage being driven, and may appear to be a short to Gnd, Vdd, or a Vref (within a single pattern), depending on the termination and the common mode range of the receiver. This should be detectable with DC EXTEST, if the differential receivers have a bias, or a referenced termination.
- Shorts to the receiver need not be considered if the coupling capacitors are on-chip.

2.2.4 DC-Coupled Fault Summary.

The Board Tiger Team defect list did not list DC-coupled defects. This is an attempt to extend their list to the DC-Coupled case. Terminology is based on the Board Tiger Team document, and the number in parenthesis is the number of faults where I have grouped them:

TxRx1+ Open
TxRx1- Open

TxRx1+ shorted to: Other (9), Rail (3), TxRx1-
TxRx1- shorted to: Other (9), Rail (3)

Where Rail (3) again represents Rail+, Rail-, and Rail? (Rail? needs to be added to the Board Tiger Team document, and represents some intermediate voltage source.)

And where Other (9) again represents:

other AC-differential signals Tx2+, Rx2+, Tx2-, and Rx2-;
other DC-differential signals TxRx3+, TxRx3-;
other AC-single-ended signals Tx4, Rx4; and
other DC-single-ended signal TxRx5.

This gives a total of 27 simulatable and distinguishable DC coupled faults.

If I use symmetry to eliminate faults on the minus leg that should give symmetrical simulation results to faults on the positive leg (dropping the TxRx1- shorts and TxRx1- open), then we have 14 remaining faults to simulate or otherwise determine the fault syndrome, considering both un-referenced and referenced termination schemes in each case.

There is no frequency dependency in this case, so high versus low frequency is not considered.

The Board Tiger Team did not include the termination resistor open or missing defects (Res1+/- open). The board team discounted these, saying that this would not be detected in normal 1149.1

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

single-ended testing. Since these terminators are required, the situation is analogous to the 1149.1 open-drain type output where the termination is required, and there is a reasonable probability of detecting that it is open or missing. These defects will be listed here to determine if there is a detectable syndrome.

2.2.5 DC-Coupled Syndrome Analysis

2.2.5.1 Open Leg

This is the same as the corresponding AC-coupled defect for each of the three listed cases, except that the signals will not decay after any transitions (it looks like the high frequency case.)

2.2.5.2 Shorts within Signal

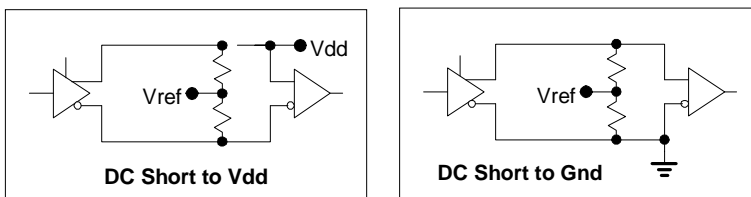
Leg to Leg short, TxRx1+↔TxRx1-, this is the same as the AC-coupled Tx1+↔Tx-1 or Rx1+↔Rx1- defects, for all terminations, and results in a float with probable glitches at the transition times.

2.2.5.3 Shorts to Rails (+, -, Vref)

- Leg shorted to ground or Vdd, TxRx1+↔Rail-, TxRx1+↔Rail+, TxRx1-↔Rail-, or TxRx1-↔Rail+, will give a syndrome that is based as much on the I/O protocol being implemented, and the technology details of the implementation itself, as on the external equivalent circuit.

Typically, the shorted output will not transition. The other output may transition, but will also typically see a significant shift in the common-mode level due to internal circuit implementation. The result may be outside the common mode range of the receiver, or there may not be crossover of the differential signals. In general, there will either be two floats, not necessarily at the same level, or a single float on the shorted leg and transitions on the unshorted leg, but not necessarily at or about the same level.

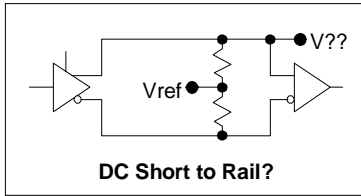
Note that some protocols use Vdd as the reference voltage (Vref), so in those cases the results may be less drastic than in the case of the short to ground, and might be equivalent to a shorted termination resistor in the case of referenced termination.



- Leg shorted to Vref or other intermediate voltage source, TxRx1+↔Rail? Or TxRx1-↔Rail?, will again depend in part on the I/O protocol and the implementation details of the driver. Certainly, the leg that is shorted will give a float condition to its receiver. The other leg will give transitions, which may or may not cross over within the common-mode range of the receiver. In general, we would expect a single float on the shorted leg and

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

transitions on the unshorted leg, but not necessarily at or about the same level.



2.2.5.4 Shorts to “Other” Nets.

This category, again, has too many possibilities to enumerate them, but we make the following observations:

- Shorts to a typical CMOS driver will look like a resistive short to a rail. The resistance is within a small factor of the differential termination resistance. So the discussions of shorts to a rail may apply here.
- There are single-ended (and possibly AC-coupled) I/O protocols that have small voltage swings and require a V_{ref} : HSTL, SSTL, and GTL, for instance. These would appear the same as a short to another differential net.
- If two nets of two different differential drivers are shorted, then, as today, relative common mode voltages, strengths, terminations, etc will determine the results.
- If a DC coupled differential net is shorted to the receiver net of an AC-coupled signal, results will depend on the driver voltage, termination on both nets, and common mode range of the receiver. This should be detectable with DC EXTEST, if the differential receivers have a bias or a referenced termination. Shorts to an AC coupled receiver need not be considered if the coupling capacitors are on-chip.

2.2.6 Syndrome Summary.

To summarize, we came up with the following tentative list of syndromes for AC and DC coupled nets. We will require simulation to verify these. They are in rough order of frequency.

1. Transitions on both receiver inputs, out of phase (no or undetectable defect).
2. Transitions on both receiver inputs, in phase (null). (This only happens with un-referenced termination.)
3. Float on one receiver input, transitions on the other. This usually involves a voltage switchover at the differential receiver, but not always. See definitions for the range of possibilities on the two inputs.
4. Float (with glitches) on both receiver inputs. They may be at a common value or different.

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

There are some strange syndromes that occur when a driven net is shorted to an AC coupled receiver net (shorted cap, crossover short, short to other driver, etc.) We assume that these defects are caught with DC EXTEST, and so the syndromes are not listed here.

2.2.7 Conclusions

1. We came up with many more situations than the Board Tiger Team where the type of termination determined the fault syndrome.
2. Because AC_EXTEST must deal with such a wide range of frequencies, relative to the RC time constant of the coupled net, we conclude that we need to detect the transitions, both amplitude and phase, and ignore any decay behavior after the transitions. With significant additional complexity, we could detect both the initial transition and the value on the net “later”. In low frequency tests, this would yield additional information, but how would that information be used?
3. If the circuits for AC_EXTEST are sensitive to transitions and their phase, as opposed to levels, then even DC coupled differential nets should be tested with the AC_EXTEST instruction, since the test receiver circuits are designed to expect transitions rather than levels.
4. Detected transitions may be used to reconstruct the transmitted digital values in order to maintain the data mapping used by the test software, but there is an essential difference in the way the transmitted data are detected in order to determine faulty or fault-free conditions. Thinking in terms of digital values only makes the problem much more difficult to solve.

3 Method Assessment Criteria

The following is a list of criteria by which the team believes the merits of each method of AC coupled differential and single-ended and DC coupled differential net testing should be evaluated:

1. The proposal is capable of what defect coverage?

Criteria: The defect coverage for both AC coupled differential and single-ended, and DC coupled differential, signals should be compliant with the official team defect list (e.g., the same as 1149.1 provides today - shorted, open, "stuck-at", etc.- on single-ended DC coupled nets).

2. The proposal is capable of what diagnostic resolution?

Criteria: Provide diagnostic capability to the failing net(s) and potential defect type(s).

3. Does the proposal provide sufficient requirements with sufficient flexibility for circuit designers to easily implement compliant analog portions of the structure?

Criteria: This standard may require some analog circuitry (typically included in the receiver I/O book). Implementation of this circuitry will have to be done for every type of interface and every technology. The requirements must be clear and yet provide flexibility to allow the designers to optimize their design.

4. Does the proposal provide adequate control over the operation of the output driver and input receiver?

Criteria: In many instances it has been noted that it is desirable to have flexibility over the operation of a pin by being able to specify if the pin participates in the DC or the AC EXTEST mode. This may be necessary to accommodate devices with several different frequency capable I/O for example.

5. What is the power consumption overhead of the proposal?

Criteria: The proposal should implement a solution that consumes "reasonable" power in operation and, preferably, one that has a power down mode so that no power is consumed when the test circuitry is not used.

6. What is the silicon area overhead of the proposal?

Criteria: The proposal should specify a solution that requires a "minimal" amount of silicon area. It should be possible that the implementation is self-contained and does not require bias currents or reference voltages that would not normally be readily available in any given design.

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

7. What level of parasitic loading does the proposal add to high-speed pins?

Criteria: In normal operation the AC EXTEST circuitry will present itself as a parasitic load to the normal high-speed data path. This amount of parasitic loading should be “minimal” so as to not compromise or to provide a challenge to realizing the desired speed performance of the design.

8. Does the proposal embody any characteristics that limit its applicability to specific IC technologies?

Criteria: The proposal must not impose any particular requirements that will limit its applicability to any particular IC technology (e.g., CMOS versus bipolar versus BiCMOS etc.)

9. What range and type of coupling capacitor values (e.g., high pass corner frequencies) can the proposal accommodate?

Criteria: The range of corner frequencies that may be encountered in practice is almost infinite. It also involves the possibility that the coupling capacitors may either be off-chip discrete components or integrated on-chip. The proposed solution should be capable of accommodating either discrete or integrated capacitors and must be scalable to all ranges of frequencies.

10. Does the proposal require an AC test signal (frequency) source other than TCK, and how is it provided (i.e., does it require extra pins on the IC)?

Criteria: Presumably an AC test signal source must be provided to the transmitting IC to allow it to generate a test signal that is passed through the coupling capacitor and detected by the receiving IC. This signal source could either be a dedicated signal, fg, or is could be the existing TCK clock signal. The use of the existing TCK signal to minimize pin count is preferable. Current testers provide TCK in many ways, it may be free running, in bursts, stopped at arbitrary times and for arbitrary periods, have an arbitrary duty cycle, and run at different rates at different times. There should not be any dependency on TCK characteristics in order to support AC_EXTEST. .

11. The proposal will have what impact on test time?

Criteria: The presence of AC_EXTEST devices should not appreciably increase the interconnect test time. AC-coupled and DC-coupled, Single-ended and differential nets should all be testable concurrently.

12. Is the proposal backward compatible with 1149.1?

Criteria: Nothing in the proposal should break any traditional 1149.1 tools, methodology, or test. Changes to 1149.1 infrastructure required by AC_EXTEST should be transparent to existing tools, and the tools should be able to safely ignore them with no penalty other than not achieving the new capabilities (enhanced defect detection for AC and differential signals). In other words, an AC test capable board should be testable on an 1149.1 tester with essentially the same coverage as achieved today.

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

13. Is compliance with the proposal verifiable from behavior at the chip pins?

Criteria: Compliance testing is currently done for 1149.1 by verification of behavior at the chip pins. This behavior is strictly defined by the rules, permissions and recommendations of the Standard, and not by the implementation examples.

14. Can the proposed structures be modeled as digital logic for verification (simulation)?

Criteria: Compliance verification tools, and simulation tools in general, require gate-level or RT-level simulation models, such as Verilog or VHDL. Any analog structures that could not be easily modeled with digital behavior would have significant impact on chip design and verification methodologies.

15. Does the proposal provide sufficient description in extended BSDL and a Package file for the new Standard to permit insertion tools to insert the test structures, and test generation tools to generate tests, and test and diagnostic tools to detect and resolve defects? How much change is required to these tools to read and use the BSDL extensions?

Criteria: There will probably be at least one new predefined instruction (AC_EXTEST), probably some new standard boundary cell (BC_x) definitions, and a new Package file that provides the CELL_INFO data for both the new instruction and the new cells. There may be BSDL_EXTENSION attributes also defined in the Package. None of this should break today's BSDL parsers and syntax checkers.

16. Are the proposed structures compatible with current chip manufacturing testers and test processes?

Criteria: What is the impact of AC_EXTEST on production test of the chips. What needs to be tested, are there any analog testing requirements, are there any specific frequency testing requirements, etc. These issues have an impact on DFT for the chip, choice of chip manufacturing tester, cost of test, defect detection and test quality, and on ATPG tools.

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

4 Methods of Detection

Propose idea of transmitting an AC signal and detecting something at other side for AC coupled circuits – both differential and single-ended

Propose idea of using EXTEST for DC coupled differential signals

4.1 Contrast different encoding and decoding methods

All proposals currently work during AC_EXTEST transmission of values by edge-detecting the received signals and using those edges to reconstruct the value transmitted, or to reconstruct an analog of the driven signal from which the value transmitted can be sampled. (This section assumes adoption of the recommendation of using TCK as the test frequency.)

4.1.1 Timing (phase) based

The MSA timing (phase) based proposal uses the edges detected to reconstruct the square wave transmitted by the driver, and then samples that reconstructed waveform in the center of a half cycle to determine the phase. This separates, in time, the sampling window from the window within which the signals are transitioning, avoiding any transitional effects due to signal skew, or other normal timing glitches. When supplemented by a “test buffer” such as the AMCC proposal, additional appropriate fault syndromes are also detected and can be used to force the reconstructed signal to a logic zero prior to the sampling circuit. Again, the fact that the sampling window is separated in time from the signal transition window makes some of this fault detection and signal suppression easier and more robust.

This proposal has potential skew issues between chips, but as long as it is TCK based, TCK can probably simply be slowed down to eliminate such problems at the tester.

4.1.2 Frequency based

The Agilent frequency based proposal counts the detected rising edges in order to discriminate one of two frequencies. As currently proposed, all such detection is per pad, and there is no attempt to look at conditions on both pads simultaneously. The encoding and decoding scheme is phase insensitive by design, has no significant skew or other timing issues between components on a board, and can even tolerate minor frequency differences between chips (not an issue if TCK is used.) The encoding and decoding scheme is very noise insensitive, even to the point of being tolerant of missing some transitions.

As a result of the phase insensitivity, the “null” fault syndrome cannot currently be detected.

(There is a recommendation that a third frequency discrimination cell be added at the output of the differential receiver, and if no transition glitches pass the differential receiver, this could

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

provide detection of the “null” fault syndrome. This, however, is potentially very noise and skew sensitive. Other solutions to detecting the “null” fault syndrome need to be proposed.)

4.1.3 Edge based

The Philips edge based proposal essentially just transmits and detects a single edge. This is currently then captured in a special “internal” boundary cell. Failure to detect the transition could also be used to force the signal captured in the normal boundary cell to zero, eliminating the special boundary cell. This proposal is extremely simple and easy to implement.

This proposal is more sensitive to noise than the other proposals, due to the lack of signal redundancy during the transmission of the test value. This proposal also does not detect the “null” fault syndrome.

4.2 Satisfaction of Evaluation Criteria

How do we determine which approach is best?

5 Implementation Recommendations

5.1 Pin Recommendations

5.1.1 Edge-detection at TCK vs. High-Frequency detection.

There are both analog and digital circuits that are capable of detecting a series of edges transmitted at a frequency well below the corner frequency of the hi-pass filter inherent in an AC coupled net. There are also distinct advantages to not having to supply a separate frequency for AC testing during board test.

We therefore recommend that whatever encoding and decoding scheme is adopted be designed to use TCK as the AC test frequency source.

Edge detection should probably be performed with a TCK that has a cycle time on the close order of 10 times the RC time constant of the high-pass filter on the net. This ensures that the capacitor is close to being fully charged for the current signal value prior to a transition, and that charge then adds to the amplitude of the transmitted edge when the next transition occurs, making the edge easier to detect.

Edge detection also removes the requirement that the test signal be a 50% duty cycle square wave, or even a constant frequency. This removes any potential constraints above those in 1149.1 on the behavior of TCK.

It should be noted in the text of the standard that edge detection does require a fast rise and fall time from the driver on the AC coupled net. This will require the chip designer and the designer of the driver boundary scan cells for AC test, to ensure that the output from the boundary cell to the input of the driver meets the timing requirements of the driver for functional operation. This requirement exists, and should be noted in the standard, regardless of whether edge detection or a higher frequency is used.

5.1.2 Providing a high-frequency, when required.

There may be situations we are not now aware of where the maximum TCK frequencies specified in component BSDL files may be inadequate to test a particular AC coupled interface.

We therefore recommend that the proposed standard should permit the tester, during the RTI TAP state, to raise the TCK frequency above the maximum frequency specified in the BSDL for the components on the board.

This permitted change in frequency may only be done after the chips participating in the AC test have entered the RTI TAP state, and the TCK frequency must be reduced to its normal frequency prior to the exit of that state. All other chips on the board or system must be placed in one of the six stable tap States prior to changing the TCK frequency and left there until the TCK frequency

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

is returned to normal. In other words, TMS may not change while the TCK frequency has been raised.

To support this, there may need to be a BSDL extension attribute that can be attached to specific ports to define a minimum and maximum frequency required for that port. Most ports should be able to use normal TCK frequencies and would not require this attribute.

5.1.3 Controlling AC_EXTEST behavior

There are situations, such as a commodity component with two or more interfaces designed to support AC_EXTEST, but used on a board where one of those interfaces is DC coupled to a chip that does not support AC_EXTEST.

We therefore recommend that a new type of optional control cell be defined for the boundary register that will determine whether a boundary cell (input or output) that is capable of supporting AC_EXTEST will behave as an AC_EXTEST boundary cell or an EXTEST boundary cell for a particular pattern when the AC_EXTEST instruction is loaded.

All AC_EXTEST boundary cells behave as EXTEST boundary cells (in accordance with the definition of EXTEST and boundary cell behavior in 1149.1) when the EXTEST instruction is loaded. This control cell simply allows a finer resolution for dynamically selecting which ports shall behave in compliance with the requirements of the AC_EXTEST instruction.

We recognize that the description of this control cell in the BSDL will be a particular challenge. This will need to be explored. The MSA proposal has this type of control cell, but the BSDL coding shown initially appears to be excessive and awkward.

5.2 TAP Recommendations

We have not seen any reason to believe that having an AC testable signal toggling at CaptureDR will in any way enhance defect detection or diagnosis.

We therefore recommend that the transmission of the AC test signal be restricted to the Run_Test/Idle (RTI) TAP controller state, and that outside of the RTI state all signals should perform in accordance with 1149.1.

This will enable the permission to shift TCK frequency during RTI; and it will enable skipping the RTI state to perform the equivalent of an EXTEST without reloading the instruction register. In either case, at CaptureDR all signals will be statically driven at the values in their respective Update latches.

ACEXTEST instruction description

AC_EXTEST CHIPS TIGER TEAM RECOMMENDATIONS

5.3 Transport Layer Recommendations

5.3.1 Stimulus Method

5.3.1.1 DC Coupled

5.3.1.2 AC Coupled

5.3.2 Detection Method

5.3.2.1 DC Coupled

5.3.2.2 AC Coupled

5.3.3 Data encoding Method

5.3.3.1 DC Coupled Differential

5.3.3.2 AC Coupled Differential

5.3.3.3 AC Coupled Single-ended

5.4 Scan Cell Recommendations

5.4.1 Banking I/O for frequency specific testing

5.4.2 Holding ACExTEST Data for Scan Out

5.5 BSDL Extentions

AC coupled pin identification

Differential pin identification

Frequency bank identification

AC test control cell

Minimum/Maximum frequency specification

6 Conclusion