



# **AC coupled interconnect test using a peak detector**

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## AC coupled interconnect test using a peak detector

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### 1. Introduction

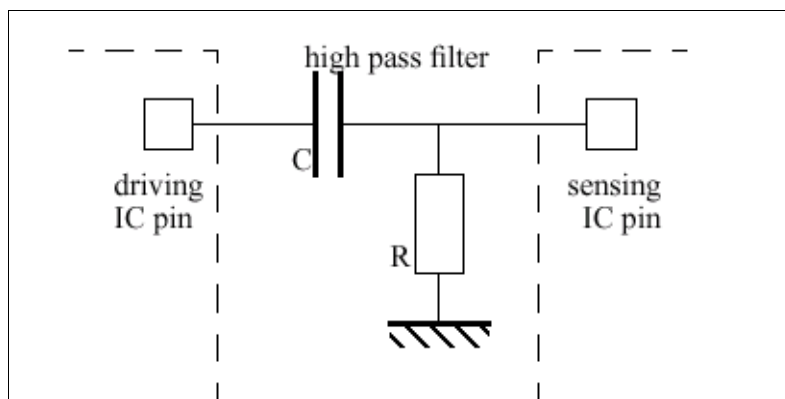
Testing digital interconnections can be done using 1149.1. Some high speed or analog pins are DC decoupled using a capacitor. In those cases the normal 1149.1 can not be used. These nets can be tested using the analog test bus, 1149.4. An implementation of 1149.4 only for testing these nets creates considerable overhead. A solution to tackle this problem that integrates easily within 1149.1, with very low overhead is presented in the following chapters.

### 2. Testing AC coupled nets

AC coupled nets are used to separate transmitter and receiver DC levels, for two major reasons:

1. Decoupling between two different DC levels in a signal path (e.g. audio)
2. Complete isolation between electrical circuits (e.g. telecom)

A decoupling capacitor  $C$  placed between transmitter and receiver together with a resistance  $R$  forms a high pass filter. See Figure 1.



**Figure 1: RC filter**

The resistive element  $R$  may be a termination resistor or the input impedance of the receiver circuit, or a combination of both.

The value of this resistance  $R$  is chosen to match the typical board line impedance, typically a value of  $50 \Omega$ .

To test the interconnection one can think of several different methods that can be applied.

The requirements for a solution are:

- simple test patterns



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- low silicon overhead / easy to implement
- robust
- valid for a wide range of applications
- technology independent

Each method contains stimuli signal generation and a detection circuit.

Test signals can be

1. AC signal (e.g. a sine wave)
2. DC signal (e.g. a 0 to 1 transition).

For detection of these signals

1. AC detection requires the verification of the repetitive nature of the signal.
2. DC detection requires a single level change detection.

A DC step is also used for the 1149.1 EXTEST instruction.

Using AC signals for interconnect test requires some sort of signal generation circuit on the transmission side and a detection circuit on the receiving side. Such a test scheme could be implemented and controlled by the 1149.1 TAP controller. This will require some sort of synchronisation between the 1149.1 TCK and the AC test signal. Implementing such synchronisation requires some circuitry as well.

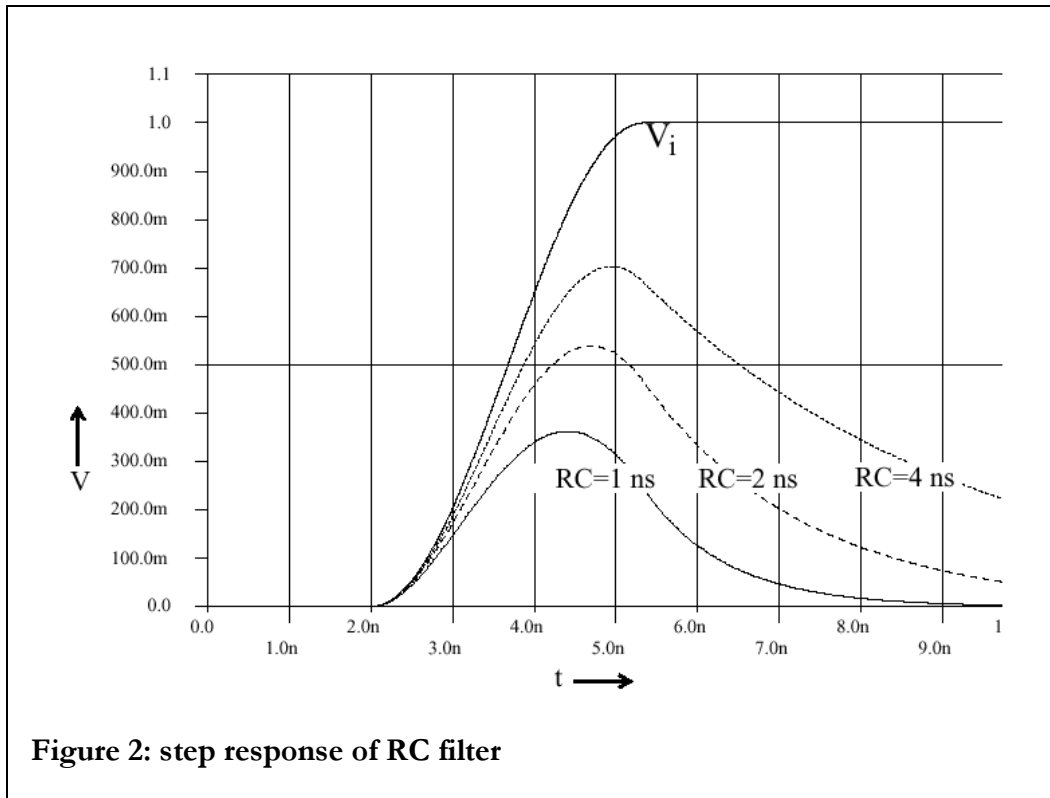
Using DC signals avoids the requirements for synchronisation and AC signal generation. It is possible to use an approach that is very close to the existing 1149.1 implementation. Such an implementation, using a peak detector will be described below.

### **3. AC coupled net response of a DC step**

If digital boundary scan would be used to test the interconnection between the 2 IC pins the applied voltage step at the driving pin will be differentiated. The result of the applied step will be a peak which magnitude depends on the slope of the driving signal, the RC value and the voltage difference between the low and high level of the driving signal.

See Figure 2, where the 10%-90% rise time is 2 ns and for RC values of 1, 2 and 4 ns the step response is plotted. The input step ( $V_i$ ) is 1 V.

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It can be seen that in this case RC values above 2ns result in a peak that exceeds 50% of the input level which is the threshold level of “a standard technology”.

Note that if the RC value is very large, there is sufficient time to capture the response using a normal boundary scan cell.

$V_i$  is the input step voltage, which changes from a lower to a higher voltage at time  $t=0$  s. For large values of RC the output voltage of the filter  $V_o$  will be close to  $V_i$  for a relatively long period of time. At time  $t=0.7*(RC)$  it will have dropped to 50% of the input level, if the slope of the input step is much smaller than RC.

With a digital boundary scan implementation the earliest possible capture moment is 2.5 TCK periods following the update state that causes the voltage step on the driving pin. This means that using digital boundary scan, the following relation holds:

$$0.7*RC > 2.5*TCKperiod$$

The output level of the RC filter will be higher than 50% of the input level when satisfying this relation.

So, in the case of a continuous TCK speed of 10 MHz an RC filter with time constant sufficiently larger than 360 ns. the interconnection can be tested using digital boundary scan. The vector needs to be applied twice with the same value. This does not introduce an edge, so the second capture should return a low value again for the faultfree situation.

To have a solution that is more generally valid we need to go a step further. Capacitors smaller than 7.2 nF, (with an input impedance of  $50\Omega$  and TCK speed of

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10 MHz) require some additional detection circuit.

From Figure 2 it can be seen that using a peak detector on the receiving side we can verify the presence of an RC filter with very small time constants. A normal boundary scan cell can monitor the peak detector output.

A peak detector implementation can be very simple, think of it as a D type flip-flop where the clock input is used as peak detection input.

Using  $50\ \Omega$  for the R value in the example, this means that a C value of 40 pF and above can be detected, even in this case with the relatively slow rising time of 2 ns. If the step rise time is shorter it will be possible to detect lower values of C. Lower C values will typically be used for high frequency systems, where the rise time is expected to be far below 2 ns. Lowering the peak detection threshold level also will result in lower values of C that will be detectable.

Verifying the presence is somewhat different from detecting defects but the difference is not that big, as will be discussed further on.

## 4. Fault model

### 4.1. Single nets

For a single connection as shown in Figure 1 the defects as shown in Figure 3 can occur.

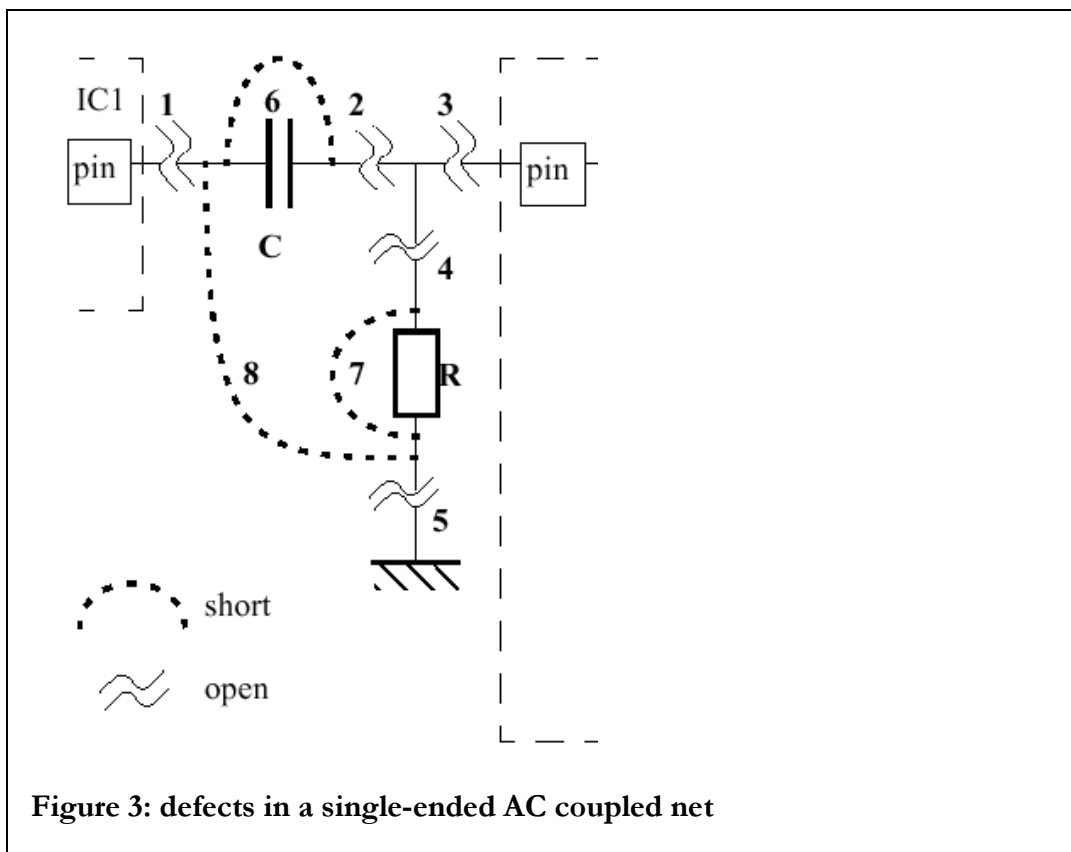
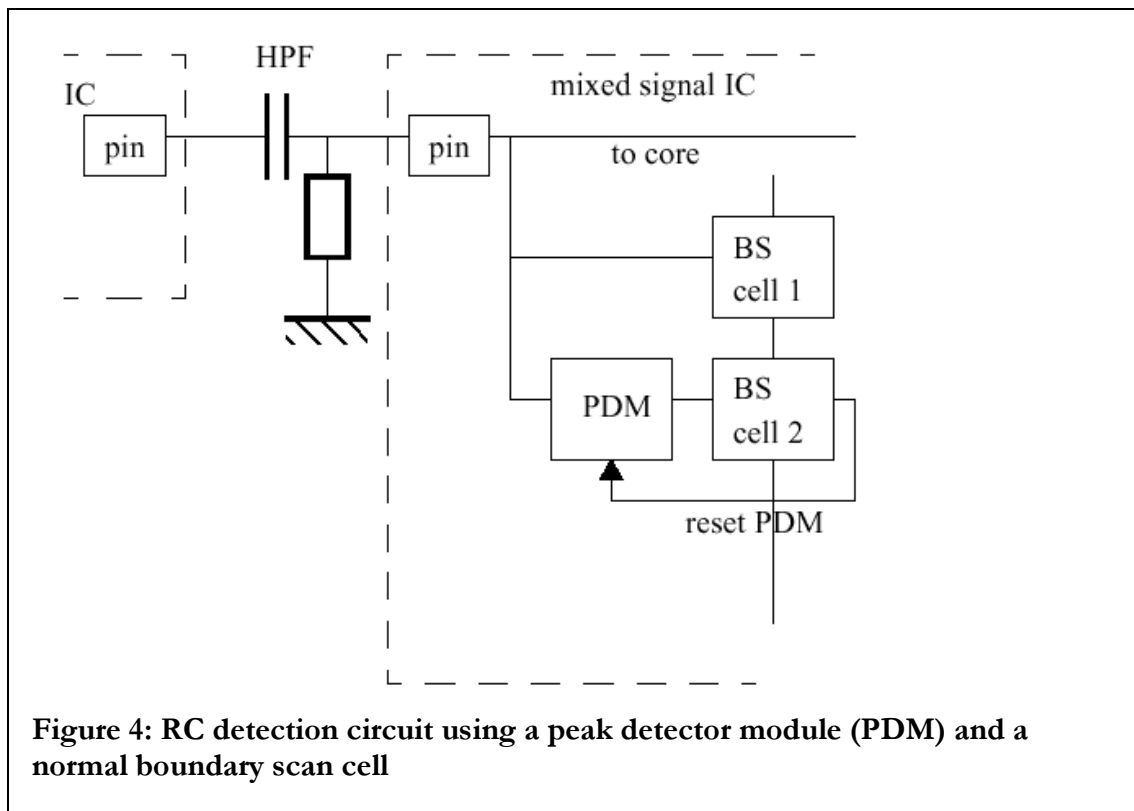


Figure 3: defects in a single-ended AC coupled net

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If only a peak detector is used on the receiving pin defects 4, 5 and 6 (i.e. open R and shorted C) will not be detected since the resulting signal follows the input step, which peak level is obviously higher than the peak detector threshold level.

To be able to detect these defects as well an additional normal boundary scan cell can be used to monitor the signal level (See Figure 4) for example 2.5 TCK periods after the applied step. Dependent on the RC value and the TCK frequency, the input pin voltage level should have returned to the ground level by then. Unless the input pin follows the output pin step, which happens to be the case for defects 4, 5 and 6. .



These defects translate into faults, including SA0, SA1, open and short. A combination of a peak-detector and a normal boundary scan cell is able to detect all stuck-at faults as well, as can be seen in the table below. The contents of the peak detector is read by BS cell 2 and BS cell 1 monitors the input net directly. The combination of these two completes the detection and allows diagnosis. The table below gives the contents of the BS cells when  $0.7 \cdot RC < 2.5 \cdot TCK \text{ period}$



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**Table 1: fault coverage table for single AC coupled net**

Defect/ fault nr in Figure 3	BS cell 1 (direct at input pin) 0 to 1 step response	BS cell 2 (peakdetector) 0 to 1 step response
Faultfree	0	1
1	0	0
2	0	0
3	(Drift to) 1 or 0	<b>Same</b> as BS cell 1
4	1	1
5	1	1
6	1	1
7	0	0
8	0	0
Output pin SA0	0	0
Output pin SA1	1	1
Input pin SA0	0	0
Input pin SA1	1	1

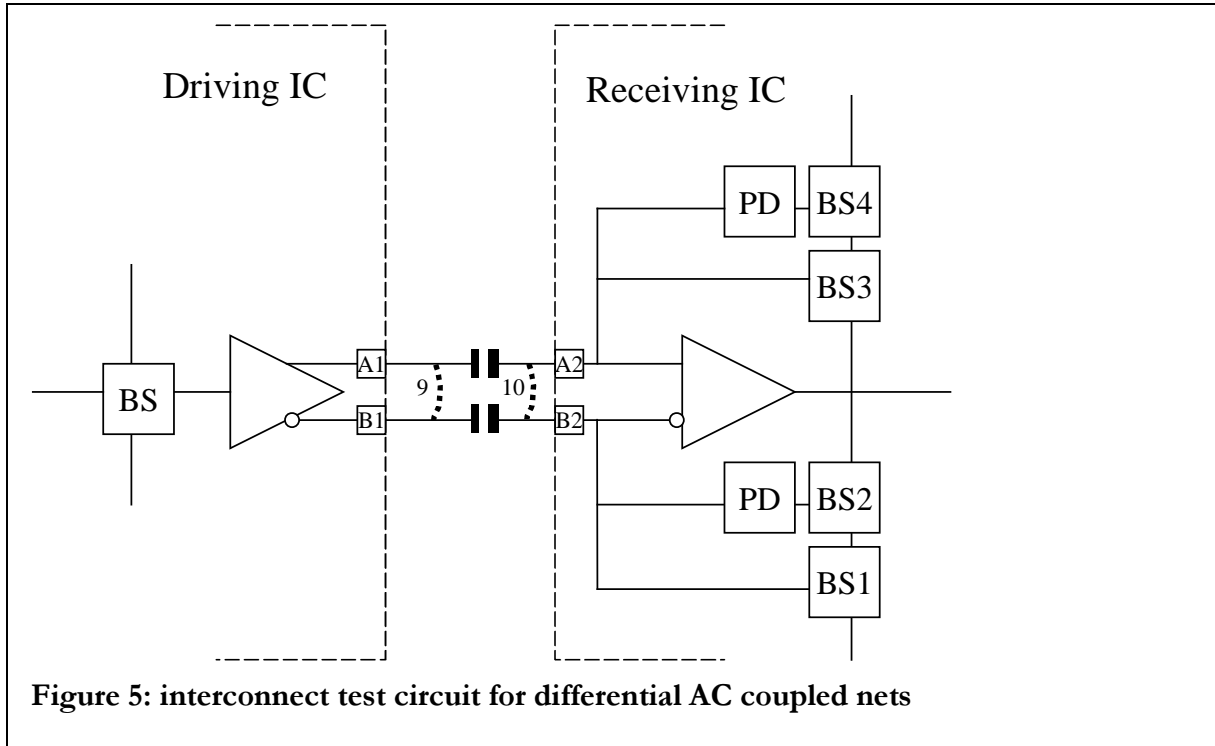
In all cases the faulty circuit response differs from the faultfree response, so all modelled faults are detectable.

### **4.2. Differential nets**

The RC network shown above in Figure 1 shows the connection for a single net. For differential nets it is possible to add the driving BS cell to both nets and consider the tests as a single net. In some cases the design cannot tolerate insertion of a BS cell after the differential driver. In that case a BS cell can be added before the driver, see Figure 5.

A peak detector only detects the 0 to 1 transition step response. The inverted differential net undergoes a 0 to 1 step during a 1 to 0 transition from the driving buffer. Defects can be detected by applying both a 0 to 1 transition, read out the captured results, followed by a 1 to 0 transition and capturing the results.

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In the implementation (shown in Figure 5) 2 additional realistic defects need to be taken into account. These defects, shown as defects 9 and 10, are shorts between the two differential nets. In the case of these shorts three situations are possible:

- Case 1. the not-inverted net and the inverted net are equally strong and as a result no or only a small peak is present on the receiving inputs, or
- Case 2. the not-inverted net is stronger and forces its signal on the inverted net, or
- Case 3. the other way around: the inverted net is stronger and forces its signal on the not-inverted net.

Since a negative peak resulting from a 1 to 0 step is not detected by the peak detectors these defects will be detectable, as shown in table 2.



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**Table 2: Fault coverage table for differential nets**

Case and Defect nr	Stimulus	BS cell 1	BS cell 2	BS cell 3	BS cell 4
Faultfree	0->1	0	0	0	1
Faultfree	1->0	0	1	0	0
Case 1, defects 9 & 10	0->1	(Possible drift to) 0 or 1	<b>Same</b> as BS cell 1	(Possible drift to) 0 or 1	<b>Same</b> as BS cell 3
Case 1, defects 9 & 10	1->0	(Possible drift to) 0 or 1	<b>Same</b> as BS cell 1	(Possible drift to) 0 or 1	<b>Same</b> as BS cell 3
Case 2, defects 9 & 10	0->1	0	1	0	1
Case 2, defects 9 & 10	1->0	0	0	0	0
Case 3, defects 9 & 10	0->1	0	0	0	0
Case 3, defects 9 & 10	1->0	0	1	0	1

For all modelled faults the table indicates full detection.

## 5. Robustness

The circuits have to operate in a non-ideal environment. The main electrical sources for functional mis-behaviour are found in ground bounce, common mode levels and random noise. The functional design of the board or system must be robust enough to deal with these effects. For testing we assume the same or better conditions (e.g. during boundary scan the processor is not running and the outputs are controlled).

The same requirements for ground bounce during test

As an example, if the ground level of the driving IC is affected by ground bounce, this falls within the functional levels and does not hamper testing. However, when many connections are tested simultaneously with boundary scan the known restrictions apply in order to prevent excessive bounce levels.

For common mode effects and random noise the test conditions should be controlled and resulting voltage levels are assumed to be well below the peak detector thresholds during testing.



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## **6. Pattern generation and BSDL requirements**

The difference with the digital EXTEST is that we have 2 cells on the receiving pin with capture values that do not coincide with the static value of the pin.

Pattern generation is straight forward but for the receiving side different from digital EXTEST. For automation of this process we require the description of the peakdetector cells as a special internal cell in BSDL.