

***ACJTAG
MSA Implementation
Proposal***

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Agenda

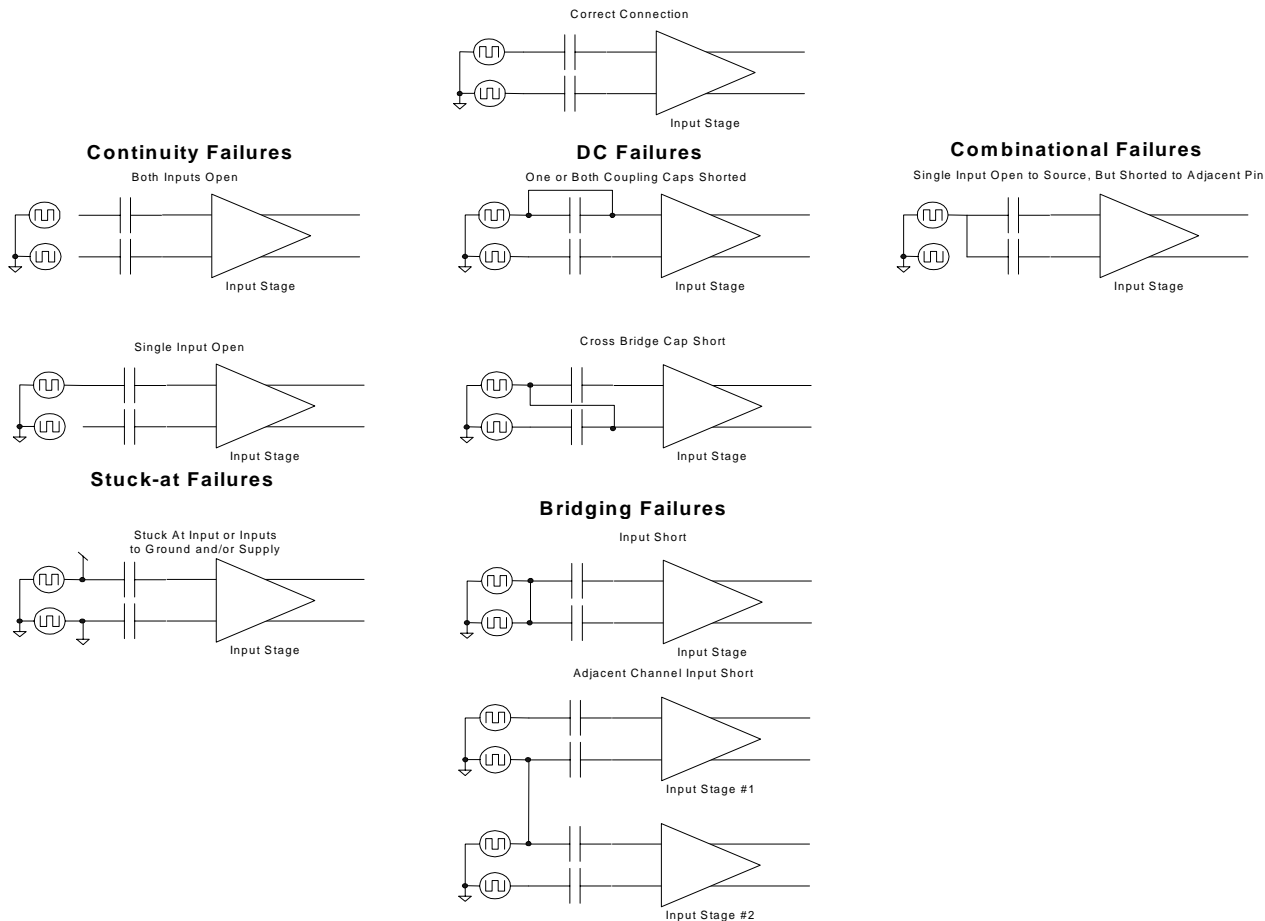
- Objectives of Implementation
- Fault Model
- Proposed Timing Based Solution
 - TX Implementation
 - RX Implementation
 - Signal Sampling Timing
 - Activity Detection Circuit
- Coupling Capacitor Value Selection
 - Consider Significance of Jitter as Compared to Droop as Defining Factor
- Comparison with Alternative Implementations
 - Frequency Based Approach
- Conclusion, Recommendations, and Issues

Objectives

- Implement JTAG/IEEE1149 Compliant Test Capability to Accommodate AC Coupled Signals
 - Utilize Existing Test Interface Pins (TCK, TMS, TDI, TDO)
 - Additional Pins Viewed as Undesirable Overhead
 - Implementation Should be Compatible with Existing Test Development Programs and Testers
 - Augment Existing TAP Controller Designs as a Means to Rapid Introduction and Compatibility
 - Minimize IC Area and Power Overhead
- Accommodate Verification of High-Speed AC Coupled Differential Data Lines
 - AC Coupling is Prevalent as Simple “Level Shift” Between Circuits Referenced to Different Power Domains and Common Mode Voltages
 - e.g., 1.8V Referenced PHY with 3.3V Referenced PMD
 - e.g., Different DC Common Mode between Different Vendor Parts
 - Differential Signals Prevalent in High-Speed Data Transmission Systems to Provide Improved Signal Integrity

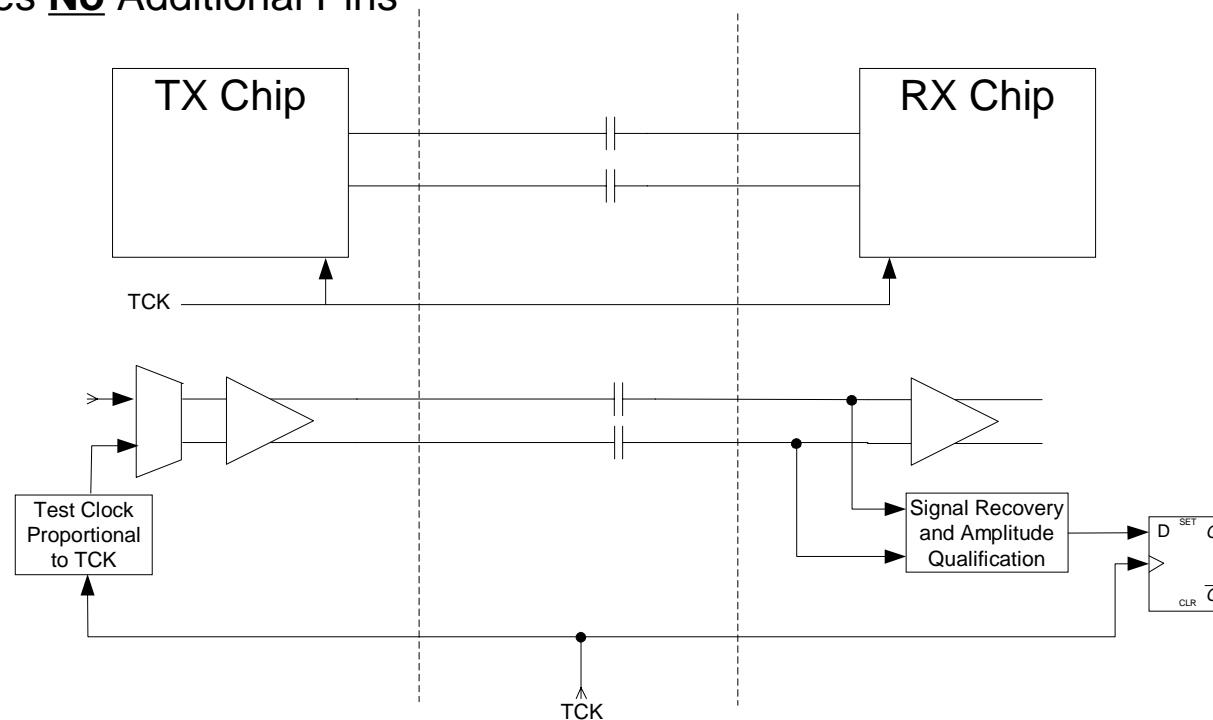
Fault Models

- AC Coupled Differential Signals Pose Several Classes of Potential Faults that Must be Detected



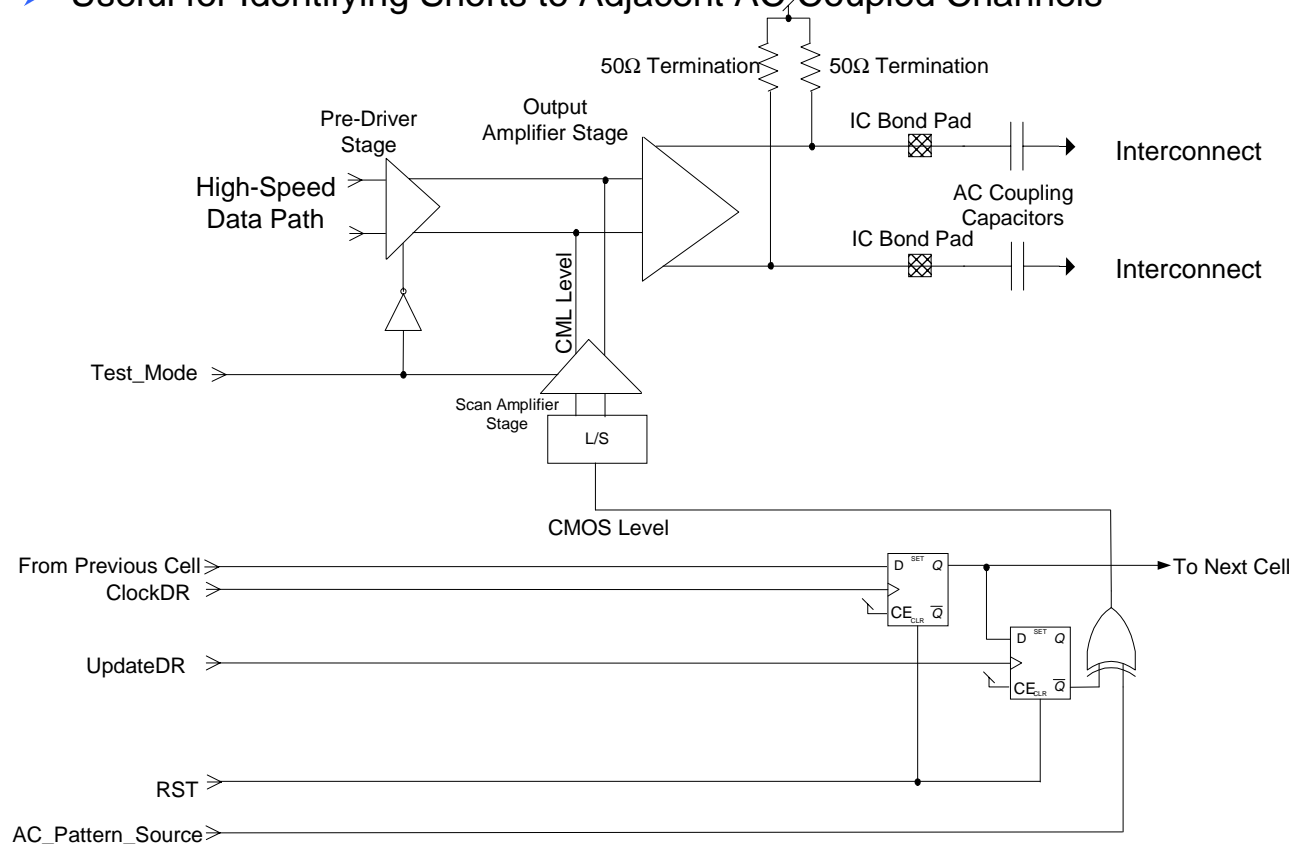
Proposed Solution

- Based on Cisco MSA Requirements for ACJTAG
- Timing Based Capture of Test Signal
 - Transmitter Generates an AC Test Signal
 - Receiver Captures and Recovers a Specific State of Transmitted Signal
 - Connectivity Verified by Pattern Matching
 - Requires **No** Additional Pins



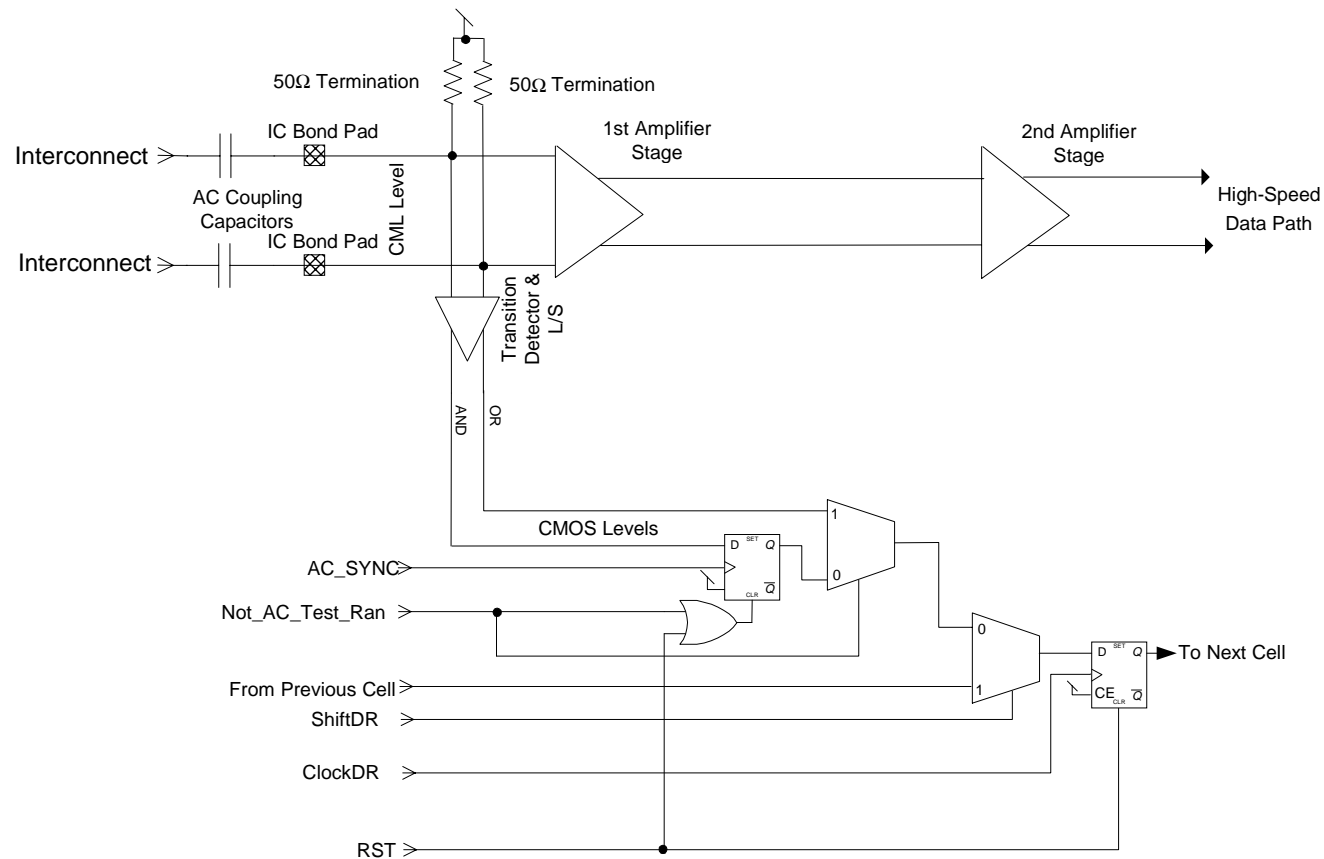
Proposed TX Solution

- TX Test Frequency (AC_PATTERN_SOURCE) is 1/2 TCK
 - Data Changes on Rising Edge of TCK
 - Data Register can be Preloaded to Define Starting State of Pattern
 - Useful for Identifying Shorts to Adjacent AC Coupled Channels



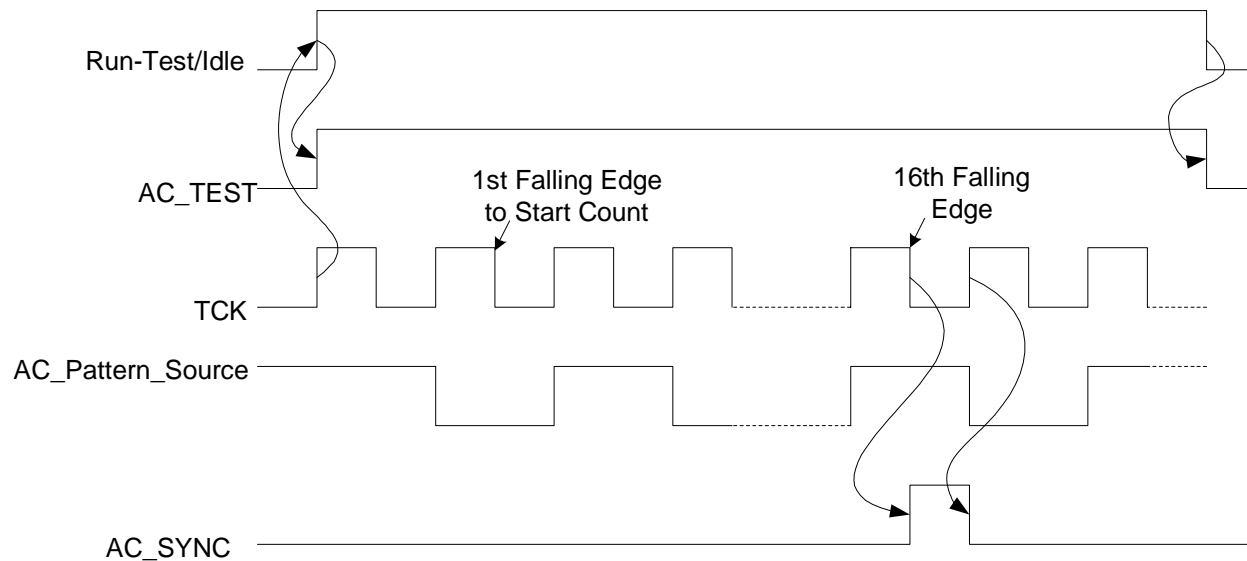
Proposed RX Solution

- RX Periodically Latches in Recovered Data via AC_SYNC
 - Data Latched on Falling Edge of Every 16th TCK
 - NOT_AC_Test_Ran Clears Sampled Data After Reading into Scan Chain



Proposed Solution Timing

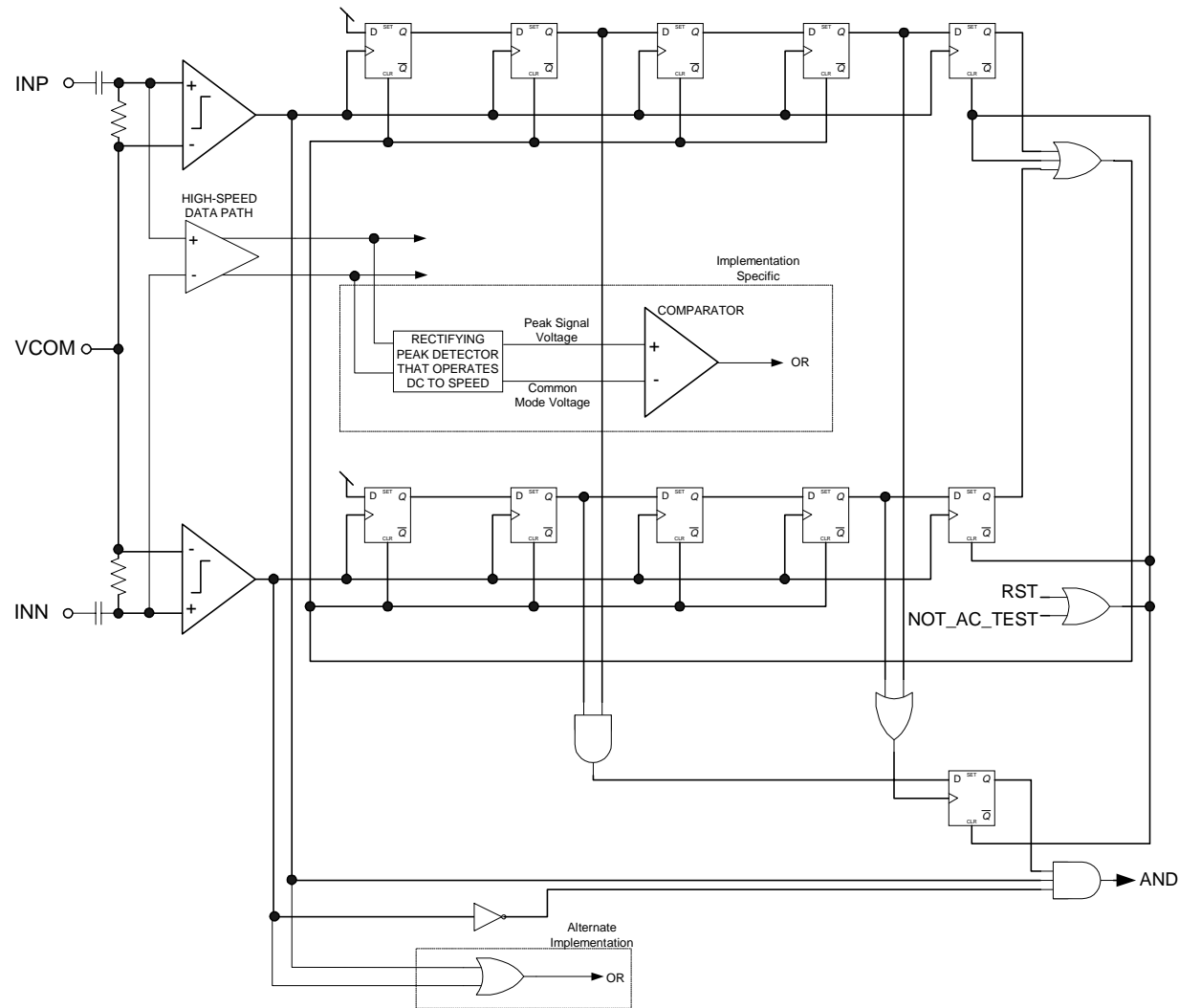
- ACEXTEST Operates During Run-Test/Idle State
 - Data Latched on Falling Edge of Every 16th TCK
 - Allows for Capacitor Settling Time
 - NOT_AC_Test_Ran Clears Sampled Data After Reading into Scan Chain



Proposed Activity Detector

- Activity Detector on RX Recovers Test Signal
 - Uses Comparators with Hysteresis on Each Input to Amplitude Qualify Test Signal
 - Counters Used to Qualify Transitional Activity on Either Half of Differential Signal
 - Provides 'AND' Output for ACEXTTEST Mode
 - $AND = Activity_on_noninverting_input \& Activity_on_inverting_input \& Input_equivalent_logical_state$
 - Activity Combined with Current State to Yield Interconnect Verification Result
 - Output will be Alternating Series of 1's and 0's that will Follow Input Data
 - Logical Output Stuck at Zero will Indicate Presence of Fault
 - Provides 'OR' Output for EXTEST Mode
 - $OR = Activity_on_noninverting_input + Activity_on_inverting_input$
 - Current Implementation Uses Rectifying Peak Detector to Form 'OR' Function
 - An Alternate Implementation would be to Logically Combine the Individual Comparator Outputs
 - Absence of Input Signal will Cause Logical Zero Output
 - Desired Result
 - Presence of Signal will Cause Logical One Output
 - Indicate DC Short Around Coupling Capacitors

Proposed Activity Detector

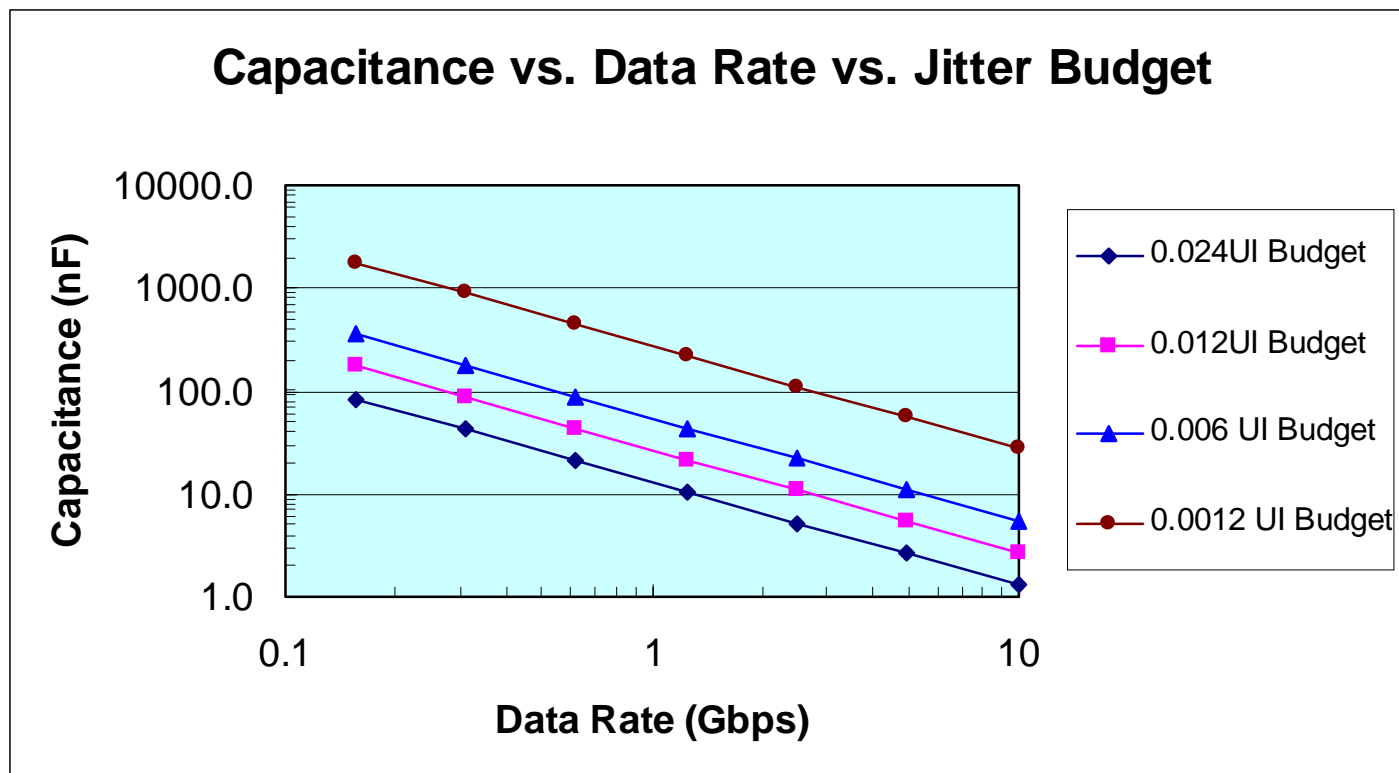


Coupling Capacitor Values

- It has Been Indicated that Timing Based Approach is Not Compatible with Industry Wide Move to Smaller Value Coupling Capacitors
 - Not Possible to Pass Low Frequency (i.e., 10's of MHz) Test Signals
- Previous White Papers have Examined Capacitance Value as a Function of Signal Droop
 - “Coupling Capacitors,” Ken Parker, http://www.employees.org/~acjtag/Coupling_Caps_200104261.pdf
 - The Potential for the Use of Very Small Coupling Capacitors was Indicated Based on this Analysis
 - pF Range!
- Droop, However, is NOT Directly Significant for Data Transmission Systems
- Jitter IS Significant for Data Transmission Systems
 - Jitter Manifested by Droop on Input
 - Recast Capacitor Value Selection as a Function of Jitter to Specify Required Capacitor Values
 - Analysis Based on Maxim Application Note (<http://pdfserv.maxim-ic.com/arpdf/AppNotes/hfan11v2.pdf>)

Jitter Based Capacitor Values

- Assume Maximum Run Length of 80 and 50 Ω Termination Resistance
- Assume 20-80% Rise Time = 25% of UI
- Assuming Typical 0.12UI DJ Budget Calculations are Shown for 20, 10, 5, and 1% of Budget Devoted to Coupling Capacitor Jitter



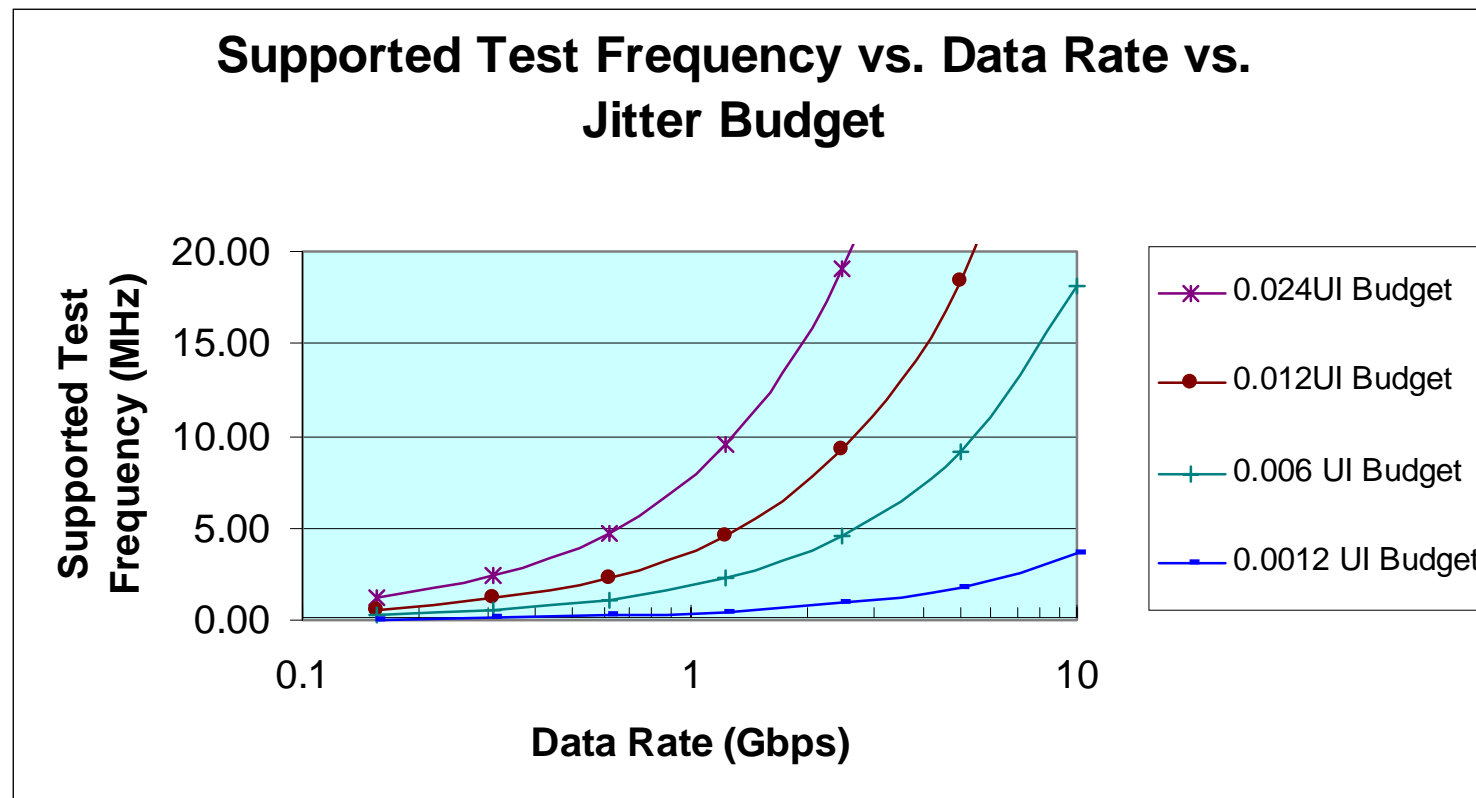
Capacitor Value and Test Clk

- Required Coupling Capacitor Value to Achieve Jitter Performance
 - 20% of the Total Jitter Budget to the Coupling Capacitor at 2.5Gbps Requires a 5nF Coupling Capacitor!
 - 20% of the Total Jitter Budget to the Coupling Capacitor at 10 Gbps Requires a 1.3nF Coupling Capacitor!
 - Typically we would Budget Far Less than 20% to the Coupling Capacitor
 - 1% would be More Likely
 - 2.5Gbps => 111nF Capacitor
 - 10Gbps => 28nF Capacitor

- Range of Capacitances Required for Adequate Jitter Performance are Significantly Larger than Indicated by 10% Droop Criteria!

Capacitor Value and Test Clk

- Using 10% Droop Criteria and Jitter Selected Capacitance Values a Lowest Supported Square Wave Test Frequency can be Calculated
 - Timing Based Solution will Require 1-10MHz Test Frequencies
 - Timing Based Solution Supported for Most of Jitter Budget and Data Rate Range!



Capacitor Value and Test Clk

- CONCLUSION: If Coupling Capacitor Values are Chosen for Adequate Jitter Performance They will NOT be an Impediment to the Timing Based ACXTEST Proposal

Comparison to Other Proposals

- Peak Detection Based Approach from Philips
 - “AC Coupled Interconnect Test Using a Peak Detector,” Schuttert and de Jong, http://www.employees.org/~acjtag/AC_coupled_interconnect_test_using.pdf
- Frequency Detection Based Approach from Agilent
 - “AC EXTEST Preliminary Specification,” Agilent Technologies, 5/11/01, http://www.employees.org/~acjtag/AC_Extest_Spec_20010509.pdf
- Current Proposal has Several Similarities with these Previous Proposals
 - Frequency Approach
 - Dual Comparators for Signal Recovery and Amplitude Qualification
 - Previous Comments Regarding the Comparators are Applicable Here
 - Choice of Hysteresis and Overdrive Levels Critical to Detecting Bridge Faults
 - Processing of Recovered Signal is Radically Different
 - Current Approach should have Significantly Lower Overhead
 - Peak Detector
 - Used Only for DC Detection in this Implementation
 - Removes Constraint on Time Constant Definition
 - Alternative Logical Implementation is Lower Overhead and Implementation Independent

+/- of Frequency Based Approach

- +
 - Attractive Due to the Independence of Phase
 - Skew Issues are Removed
 - Capable of Operating at Near-Speed
 - This may not Necessarily Add Test Coverage
- -
 - Requires an Extra Pin
 - More Pins on a PMD for Test than for Intrinsic Function
 - PMD's Demand Low Pin Count for Die Size/Proximity Placement to Optics
 - Unattractive Due to Independence of Phase
 - Not Clear if Bridge Faults Can Necessarily be Detected if Test Signals in Phase
 - Cannot Detect Combinational Fault
 - High Digital Implementation Overhead?
- Advantage of Timing Based Solution Over Frequency Based Approach
 - No Extra Pin and Less Silicon Overhead
 - Better Fault Coverage
 - Detects All Fault Conditions
 - Lower Test Frequencies Reduce Skew and High-Speed Board Routing Issues

Conclusion, Recommendations, and Issues

- A Low Overhead Extension to the Standard JTAG Interface has been Proposed
 - Timing Based
 - No Extra Test Pins
 - Detects All Faults
- Jitter Based Coupling Capacitor Value Selection Reviewed
 - Required Capacitance Value Significantly Larger than Droop Model!
 - Supported Test Frequency Derived
 - Coupling Capacitor Value is NOT an Impediment to Timing Based Solution
- Comparison of Timing Solution to Other Proposals Made
 - Numerous Similarities
 - Peak Detector Not Used at Speed So Time Constant Issue Removed
 - Frequency Based Solution has Implementation and Pin Overhead
 - Frequency Solution Does Not Identify All Faults

Conclusion, Recommendations, and Issues

- Timing Solution has Advantages Over Other Approaches
 - Better Fault Detection with Lower Overhead
 - Edge Qualification has Many of the Advantages Embodied in Frequency Approach
- Frequency Based Solution Requires Augmentation for Improved Fault Coverage
 - Identify Bridge and Combinational Faults
- Skew Management Guidelines Need to be Developed for Timing Solution
- Requirements for Signal Recovery Comparators Needs to be Developed
 - Distinguish Bridge Faults
 - Different Signal Level Standards
 - Sensitivity and Signal Attenuation
- Preliminary Recommendation Required for Preferred Solution Approach
 - Allow Early Adoption of Standard