



Cisco Input Test Buffer Design Examples for AC Boundary-Scan

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This paper presents Cisco input test buffer design examples that can be used in combination with the MSA AC Boundary-scan proposal [4]. Fault coverage discussed in this paper is based on fault syndromes observed at the input buffer.

1 Input Test Buffer Description

Figure 1 shows the physical connection of differential input and output buffers and building blocks used in the Cisco input buffer. Note that an analog input signal interface to the boundary-scan domain is assumed. Six different building blocks are used in the buffer and listed below. Each component in the buffer plays either unique or multiple roles in detecting and identifying various faulty input signal conditions.

- Null Receiver
- Technology Mapper
- Signal Recover
- Short and Null Detector
- AC detector
- Integrator

The six blocks are discussed in the rest of this section. If the signal passes through the test buffer section of input amplifier, the signal is translated into the digital domain and is further processed by following digital test circuits.

1.1 Overview

For the purpose of simplicity, Figure 1 shows only the test buffer and related sections of differential receiver, the mission logic buffer and amplifier are omitted. The “Physical Link” layer represents physical connection between two devices [5]. When DC boundary-scan is selected, a driver takes a logical value from logical link, which is not shown in Figure 1 and puts it on the physical link. The receiver does the same but in reverse order. Note that the values in the physical link are same as in the logical link. When AC boundary-scan is selected, it takes a logical value from the logical link layer, translates it into an AC signal, and drives the actual physical link. The receiver monitors the AC signal and translates it back to a

logical value, and then it is passed to the logical link layer. The “Transmission Layer” between the Differential Driver and Null Receiver forms signal transmission media, which carries signals from the driver to the receiver. For the DC boundary-scan, it is a set of differential signal wires with or without termination resistor network. For the AC boundary-scan, it contains a set of differential signal wires and AC coupling capacitors with or without termination resistor networks. It may contain common mode reference voltage bias network. The “Input Test Buffer” consists of 6 functional blocks and links test signals between the physical link and the logical link.

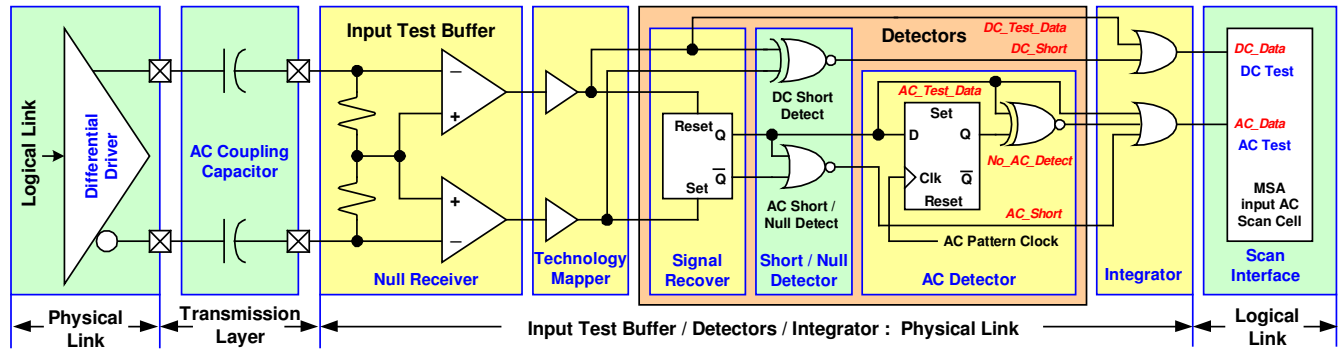


Figure 1: Example Input Test Buffer for MSA AC Boundary-scan proposal

1.2 Null Condition

Null is an analog level where a given receiver technology neither defines the voltage level as logic 1 nor as logic 0. It is a logically indeterminate level and will be referred to as “Null Condition” throughout this paper. A receiver may or may not translate such a null condition into fixed logic 1 or logic 0 state. A receiver, however quite often performs forced translation of this condition and thus creating “Fault Masking” condition during boundary-scan test. Due to a built-in input buffer hysteresis or fixed voltage bias, conventional DC boundary-scan sees a null condition as a consistent and repeatable logic state at the single ended receiver. Therefore, when the test is conducted on the single ended signal line, both DC and AC Boundary-scan test do not impose a coverage loss due to the null condition.

However, for differential signal lines, there are more possible cases of null conditions due to non-complementing signal conditions, where differential signal pair does not develop predefined differential voltage difference between the two signal lines. Because of a defect, both differential signal lines can have the same analog signal level such that the signals are identical to either the non-inverting side of differential signal line or the inverting side of differential signal line. These null conditions create unrecognizable differential voltage difference or voltage difference specified outside of functional operating range by the given input buffer. As a result these null conditions can create forced mapping situation when the signals are translated into the digital domain without proper input buffer setup.

These forced mapping can contribute up to 50% of test coverage loss during boundary scan test. Simply, 50% of all possible differential signal transmission states can fall into this null condition in the presence of defects. However digital representation of these analog levels, as stated before, do not create tangible test coverage loss for the single ended signal line. More detailed analysis of possible error condition is given on “Error Population” in Section 2.

With presence of certain faults, the given receiver can encounter a null condition during both DC and AC boundary-scan test, especially with the differential signal lines. The null condition for the differential

signal lines has been a real test challenge for both DC and AC differential line boundary-scan testing because there is a very high “Error Population”. Use of small RC time constant relative to the test clock for an AC coupling can also create null condition during the AC boundary-scan test even with defect free condition. Detailed behavior of such case is discussed later in Section 3.

Reception and detection of all null conditions are the most important aspect of input test buffer design in order to achieve comprehensive differential line boundary-scan test.

Figure 2 shows simple pictorial view of how differential signal is being transformed from the differential signal driver to the input test buffer, and to the signal recover.

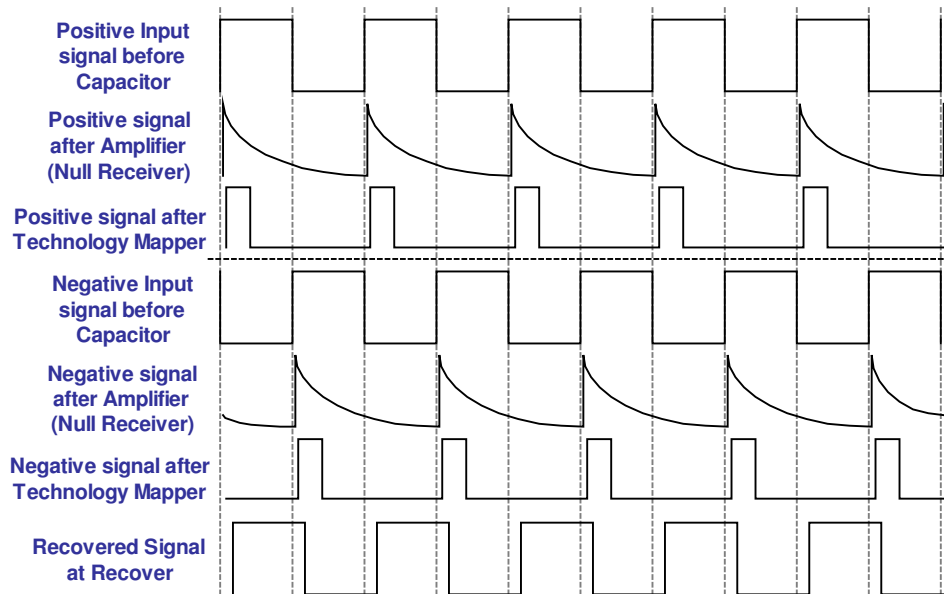


Figure 2: Signal transitions

1.3 Null Receiver and Signal Recovery with Null Condition

Once the AC signal is filtered through a coupling capacitor, the “Common Mode Voltage (V_{CM})” or the “Reference Voltage (V_{ref})” normally DC biases incoming signal at the receiver side. The common mode voltage is often determined by the receiver technology. The differential AC signal needs to be translated into the digital domain so that the signal can be processed by the following boundary-scan logic. The two input buffers shown in the first stage of Figure 1, process the incoming differential AC signals separately and amplify differentially against common mode voltage. The amplified signal is further processed by subsequent digital logic.

The example input test buffer design uses multiple input differential amplifiers as shown in Figure 4 and 5. Each input amplifier processes both differential input signals at the same time. Both amplifiers therefore provide a single ended view of each differential signal based on the common mode voltage. This amplifier stage can easily detect an open net, if the open net creates an insufficient voltage difference to trigger the input differential amplifier into a good logic state. It is very important to note that the reference voltage setup and input amplifier design influence over all AC boundary-scan test coverage.

Figure 3 shows typical differential signal input parameters and the “Null Detection Range” of 85% of the given input threshold voltage range. The 85% value was chosen arbitrarily to demonstrate how

different null receiver recovers incoming signal to create corresponding set and reset signal. Study shows [1] 80% of threshold voltage range was used successfully to achieve “Fail-Safe” condition for the differential receiver. Example fail-safe condition, however only demonstrated static performance of the fail-safe circuit and is different than the null condition created during the AC boundary-scan test.

1.3.1 Practical Difficulties

But for AC coupled differential network carrying dynamic AC test signal, example 80% null detection range may not serve satisfactory result. A coupling capacitor creates “voltage doubling effect” at each signal transition where most of AC energy is concentrated when the signal is matched with proper termination resistor network at receiver side. This voltage-doubled signal tends to over drive input buffer. A differential driver also tends to over drive the receiver for the practical board design purposes. Both of these over driving voltage conditions will result in fault amplification where faulty signal may develop larger signal difference than the specified input threshold voltage. Because of these factors, it is very difficult to specify fixed voltage range to achieve comprehensive null detection.

1.3.2 Signal Recovery Methods

In Figure 3, two recovered signal waveforms are shown, one with null detection range of 85% of threshold voltage range and the other with no null detection range. The “Set signal excluding null condition” and “Reset signal excluding null condition” waveform clearly show that whenever two input signals are within 85% of input threshold range, both signals are in logic “0” states signifying the inputs are in null condition. On the contrary, the “Set signal including null condition” and “Reset signal including null condition” waveform show that both signals change at zero differential voltage in ideal design where two signals cross each other, thus null condition is included within the “Set” and “Reset” signal waveform and they can not be at the same logic state. Preferred test signal recovery method is to sense the null condition and generate the ideal “Set” and “Reset” signal value in order to decode sensed null condition into either logic 1 or logic 0 for the Logical Link Layer [5]. In this figure the signal received through input buffer is in null condition if both signals labeled as “Set signal excluding null condition” and “Reset signal excluding null condition” are in logic 0 value. The “Active Condition” signifies functionally defined condition where the signal is no longer within the defined null condition. Figure 3 shows null condition being decoded as both logic 0, however many fail-safe circuit use logic 1 as a null condition [1]. Receiver V_{IH} and V_{IL} range defines the active condition where the differential signals operate within the functionally defined voltage range.

The null detection example can be used to design technology specific input test buffer by utilizing the input threshold range, the null detection range, receiver Input Voltage High (V_{IH}), and Input Voltage Low (V_{IL}) values. Typical AC pattern application speed of around 20 MHz should be achievable with functionally identical input slew rate because test driver should also use functionally identical slew rate. The low limit of the AC pattern application speed should be defined by the input test buffer designer but should not be less than 1 MHz and it is a function of given RC time constant of the AC coupled net and input buffer threshold range. The upper frequency value of 20 MHz is a current test frequency limit for the commercially available boundary-scan tester and the lower frequency limit value of 1 MHz is the maximum delay the AC signal sample interval can have before the signal decays below the input buffer threshold range (current input buffer has value of 20 to 30 mV) for the LVDS with 0.01 μ F coupling capacitor and 50 Ohm termination.

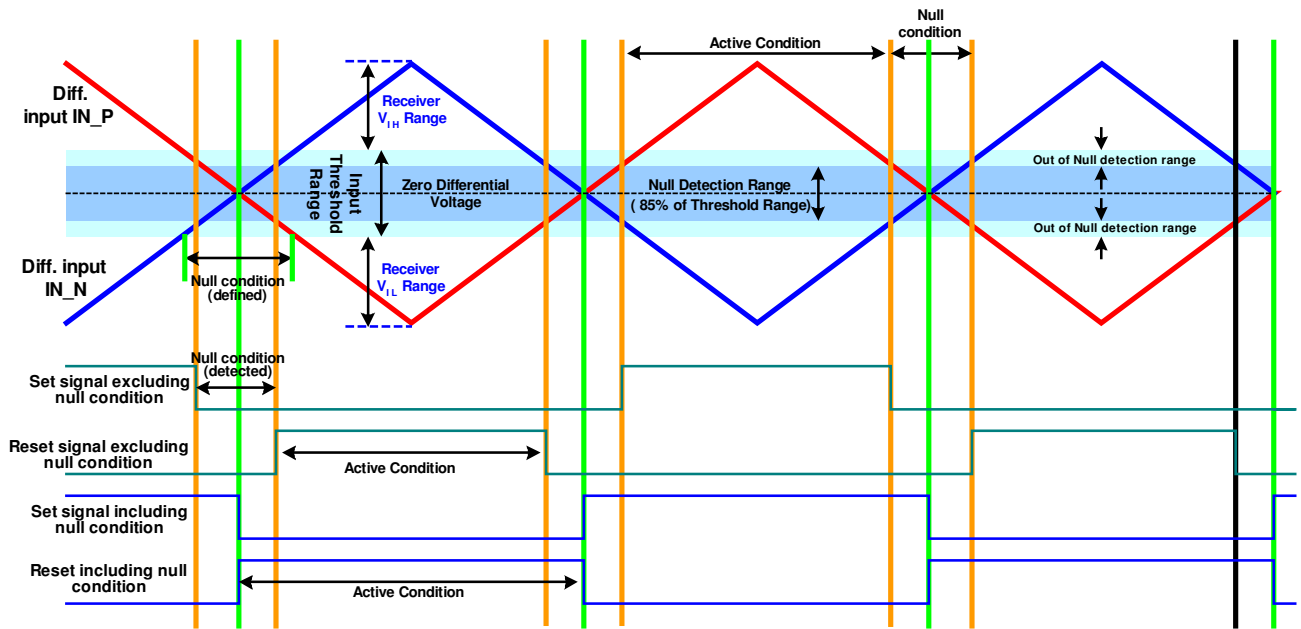


Figure 3: Null Receiver detection range and signal recovery examples

1.4 A Fail-Safe Mechanism

LVDS features a “Fail-Safe” mechanism to improve system reliability by preventing the error (null) conditions caused by open or uncommitted nets [1]. The fail-safe guarantees that the receiver outputs are in a known state, typically the logic high state, when the receiver inputs are under certain fault conditions. Without the fail-safe feature, any external noises above receiver thresholds could trigger the output to an unknown state. According to the TIA/EIA-644 Standard [6], when the receiver inputs are open, not connected to the signal driver, or the signal driver is off lined or powered off. The fail-safe feature will drive the output high. If the receiver inputs are shorted, the outputs should also be driven high by the fail-safe mechanism. The standard also states that the receiver outputs will enter a fail-safe mode if the differential inputs remain within the threshold region for an abnormal period of time. This protection feature not only has many benefits for a system designer, but also has extremely important features for differential line testing with AC boundary-scan techniques. These fail-safe features could be an essential part of input buffer design especially for AC boundary-scan testing. As stated earlier, the fail-safe feature shown as an example may not perform as intended during the boundary-scan test with certain fault conditions.

1.4.1 Input Test Buffer Examples

Three input buffer design examples are given below as an example. These examples have built-in null detection capability. If the differential voltage difference between the two signal inputs is not greater than the predefined range, both the Set and Reset signal become the same value, preferably logic 0 equivalent value. Otherwise, in normal operation the Set and Reset signals represent the current logic level or state of the differential input signals.

The left example in Figure 4 divides incoming differential signal levels into 3 segments; logic high,

logic low and null condition, and generates set and reset signal accordingly. If the null detection range is set to 100 mV as in the LVDS threshold voltage range, this circuit can serve as a good input test buffer example. Further enhancement to the example can be made to generate two scan cell interface signals, reset and reset-bar pair and set and set-bar pair as shown in Chapter 5 and Chapter 6. These signals can be used to interface with two signal recover circuits, one for the IN_P and the other for the IN_N signal.

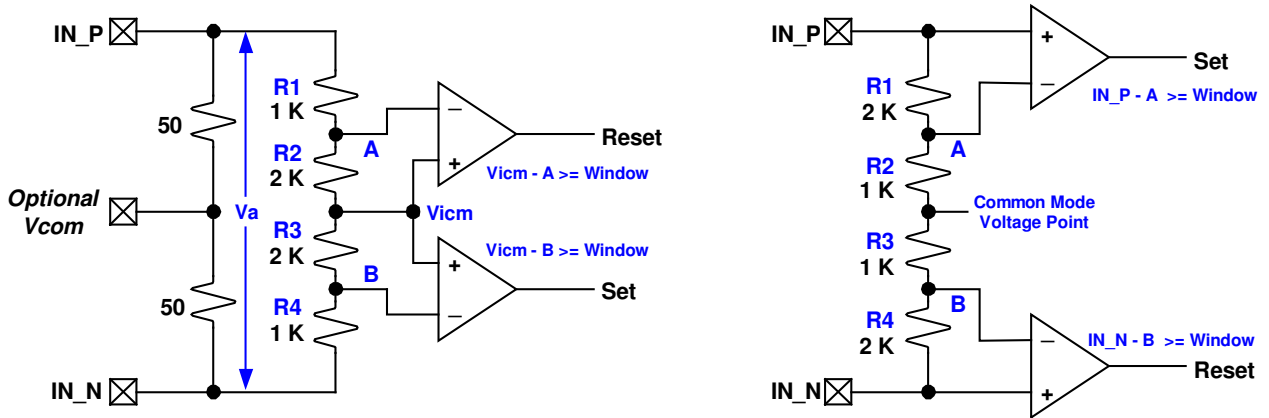


Figure 4: Input buffer design example 1 [2]

The right example in Figure 4 is from [1] and by changing 80 mV to 100 mV to work with the LVDS circuit for example, it can also achieve corresponding performance as in [1] during boundary-scan test. Both examples take common mode voltages from different sources and have different CMRR (Common Mode Rejection Ratio). The example in the right may use common mode voltage from its own voltage source rather than from incoming signals.

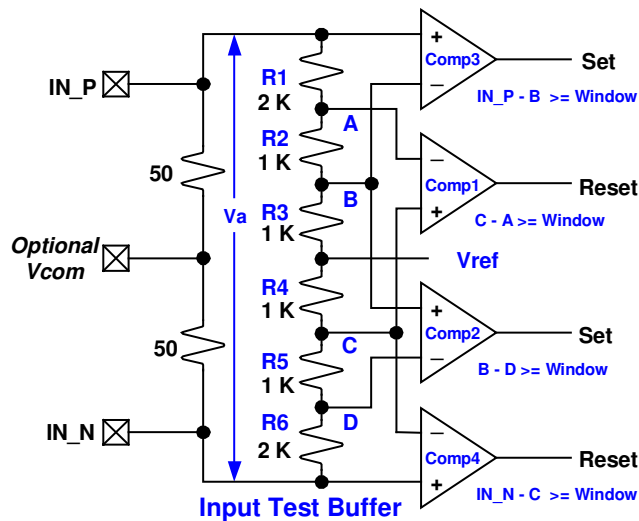


Figure 5: Input buffer design example 2

Figure 5 shows another example and uses four comparators to interface two boundary-scan cells per differential pair. Because of the voltage reference **Vref** used and the comparator setup, this example provides good test coverage and diagnostic information at the same time. More detailed interface examples are given in Chapter 6.

1.5 Test Signal recovery scheme

Figure 6 shows various ways of recovering and detecting null and active condition. A window comparator based input test buffer will create “Recovered signal excluding null condition” signal by decoding the null conditions into logic 0 value for both set and reset signals.

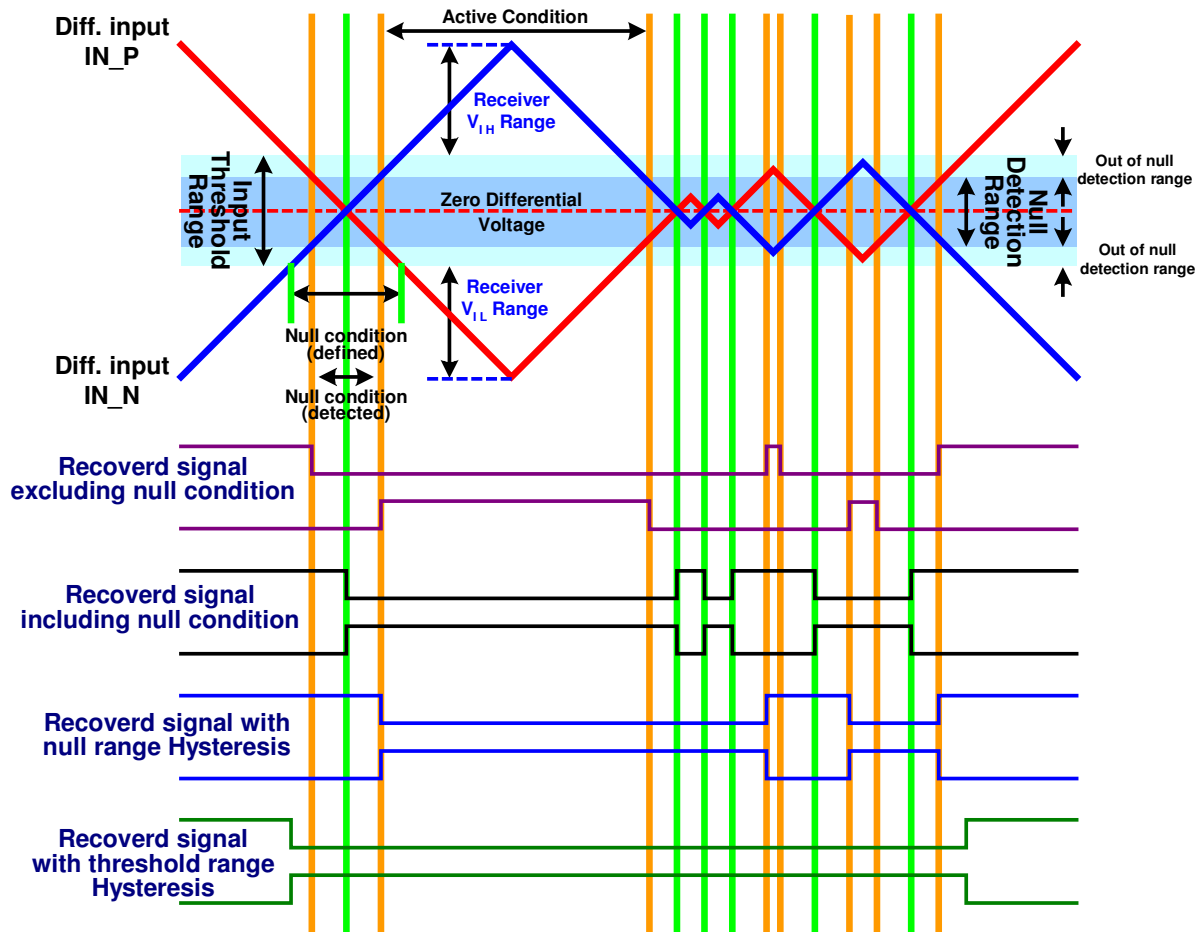


Figure 6: Various signal recovery schemes

The second “Recovered signal including null condition” signal depicts ideal functional receiver behavior where ideal zero differential voltage is used to create signal transition. The third “Recovered signal with null range Hysteresis” signal uses hysteresis to detect null condition. The fourth “Recovered signal with threshold range Hysteresis” uses entire input threshold range for null detection. Both third and fourth case where hysteresis is used to detect null condition do not generate recovered signal to signify where the null condition is from set and reset signal pair when differential signal is used differentially for null detection. However single ended view of the differential signal with the same hysteresis may generate null condition by examining both recovered signals at the same time. The hysteresis with desired null detection range can filter noise from input signal however it does hold previous value if the current input signal value is within the hysteresis region thus it requires known initial value before the test and does not provide real time status of input condition as in DC boundary scan test.

In summary, differentially processed and window comparator based null detection method proved to be the most desirable input test buffer design methodology. Further processing of this recovered signal provides additional test coverage as discussed in Section 3.

1.6 Technology Mapper

The technology “Mapper” links the signals between the analog amplifier block and the digital signal “Recover” block. The generated digital CMOS signal can then be processed by the downstream logic, the logical link layer. This technology mapper can be integrated within an input amplifier block. The pulse width shown in Figure 2 can be extended and adjusted with use of delay logic (buffer) when necessary.

1.7 Signal Recovery

When the two differential signal pulses from the technology mapper drives the set and reset input of the RS latch, the original waveform driven by the differential driver can be recovered as shown in the Figure 2. The RS latch can simply be designed with two cross-coupled NOR gates. The RS latch truth table is shown in Table 1 and used in the discussions of Section 3.

Input	Output	
Reset / Set	Q	QB
0 / 0	Q	QB
0 / 1	1	0
1 / 0	0	1
1 / 1	0	0

Table 1: RS Latch Truth Table

1.8 Short and Null Detector

The same RS latch is used to recover the valid logical state from the technology mapper signals. It is also used detect short faults, which make two differential lines into the same logic values with the aid of the null detector. The short faults between the differential signal lines create the same pulses by the null detector. When the set/reset signal inputs are both high, implying that both input amplifiers are tracking the same signal, Q and QB are forced to the logic value 0 instead of normal complementary Q and QB state (see Table 1). When the set/reset signal inputs are both low, it is not considered as short in AC aspect because of the coupling capacitance draining effect and they are selected by the different technique discussed in Section 3.

The AC short detector detects the state 00 from the Q and QB output of the RS latch and flags the state as a fault. The DC short detector compares Set and Reset state and flags as an error if both signals are in the same logic state.

1.9 AC Detector

The AC detector detects and tracks signal changes. Note that it is not counting the number of incoming pulses, but detects the toggling of input signals. The detector flip-flop is cleared at the beginning of every sixteen cycles (i.e., MSA sync pulse interval) or between each capture operation to keep the data fresh with current line activities. This clear logic is not shown in Figure 1. This AC detection can also be done before the RS latch as in AMCC implementation [7], which incorporated an analog activity detector. This

detector can be extended to count pulses between AC captures if necessary. (Note: Example circuit in Figure 1 compares AC status during the entire 16 AC pattern clock cycles. It will be a better approach to detect AC activity by checking only two consecutive cycles instead of 16 cycles because there is a “slow to change” fault in the differential line.)

1.10 Integrator

Finally, fault syndromes detected and analyzed by the preceding blocks are encoded into one or more signals to be sampled or captured by MSA input boundary scan cell(s). Table 2 shows possible combinations of input signals to the integrator.

Input Reset / Set	Output Q / QB	Recovered data	AC short status	DC short status	AC detector	Result
0 / 0	Q QB	Hold	1	1	0/1	1
0 / 1	1 0	D	0	0	0	D
1 / 0	0 1	D	0	0	0	D
1 / 1	0 0	0	0	1	1	1

Table 2: Encoded Values at Integrator from the Results of Detector Blocks

Error conditions represented by the AC short status, the DC short status or the AC detector are logic “1” and all normal conditions produce logic “0”. The first row of the column “Result” represents the null condition resulting from the AC boundary-scan test with small-RC case discussed later in Section 3. Since the RS latch does not create an “11” output condition except the transition period, which does not affect capture window proposed by the MSA proposal, it is not considered in the discussion.

2 Fault Coverage Analysis with Input Signal Patterns

2.1 Error Population

Faults can only be detected when the input test (or mission) buffer processes an incoming signal and generates a predefined condition which preserves the state and discriminates between a good and faulty signal. For differential transmission technology, test coverage depends largely on the receiver’s input buffer rather than the type of AC patterns used. Because of this, the pattern generation and driving circuit can be greatly simplified. Either in traditional DC boundary-scan test or proposed AC boundary-scan test, test escapes related to the differential transmission line are largely contributed by receiver’s input buffer, which maps an undefined logic state caused by defects into a valid logic value. This fault masking resulted from such translation makes differential line testing extremely difficult for both DC coupled and AC coupled transmission lines.

A brief overview of both single ended and differential signal error population is given in the Table 3. Note that both the transmitter and receiver have no non-driving high impedance state for simplicity. The ALS (Available Logic States) is defined as all available logic states for both transmitter and receiver for 0 and 1 transmission. All possible logic states for a pair of differential signal lines are the 00, 01, 10, 11 states. In reality, the differential lines carry analog representation of digitally driven value and have implied logical meaning only when the signals are analyzed differentially. However for simplicity and

explanatory purposes, the term 00, 01, 10, and 11 are used to represent all possible analog conditions during differential transmission. There are four possible combinations of logic state for any given logic 0 or 1 transmission. For testing purposes, there are 8 possible outcomes from both transmissions.

If only a single fault is considered at any given instance, there are only 00, 01, 11 and 00, 10, 11 combinations, so that there will be 6 possible outcomes from both transmissions. Notice that the combination 10 for the 0 transmission requires two bit reversal since fault free transmission has logic value of 01. The same condition applies to the 1 transmission, which has fault free transmission logic value of 10 so that the combination 01 is not included. Error populations are calculated by taking the percentage of error state from non-error state. If the high impedance state is used in conjunction with existing logic states, the error population may be reduced because the high impedance state helps reduce logic states based on a single error condition.

	Logical Link Value	Physical Link and Transmission Layer Value				
		Single Ended	Differential Signal			
			Possible logic state		Logic state with single error condition	
Transmitter	0	0, 1	Positive	0, 0, 1, 1	Positive	0, 0, 1
			Negative	0, 1, 0, 1	Negative	0, 1, 1
	1	1, 0	Positive	0, 0, 1, 1	Positive	0, 1, 1
			Negative	0, 1, 0, 1	Negative	0, 0, 1
Receiver	0	0, 1	Positive	0, 0, 1, 1	Positive	0, 0, 1
			Negative	0, 1, 0, 1	Negative	0, 1, 1
	1	1, 0	Positive	0, 0, 1, 1	Positive	0, 1, 1
			Negative	0, 1, 0, 1	Negative	0, 0, 1
Available logic states	2	4		8		6
Error Population		50%		75%		66.6%

Table 3: Error Population

It is also important to notice that the logic states created by a single fault are a null condition. If a differential pair sends 01, a receiver will either see 00, 01, or 11 if there is only a single bit change cause by a defect. The “10” requires two bit reversal thus it is not considered as a single fault. Two states, 00 and 11 are the faulty states and along with the 01 state they constitute 66.6 % error population and can be detected by the null detector circuit.

The Table 3 represents the DC transmission line error population with the single fault condition, not the single defect condition, where in many cases multiple fault conditions are possible. An AC coupled transmission line needs more complete analysis to determine accurate corresponding error population.

Since an AC coupling capacitor blocks transmission of DC signal from one side to the other side, it is quite possible to have up to 4 different logic states for the given logic transmission, 3 for the transmission side as we have seen in Table 3 and 4 for the receiver side. If a differential pair sends 01, through the AC coupled lines, a receiver will either see 00, 01, 10, or 11 when transient value of the transmitted signal is captures based on the AC coupling line RC time constant. The steady state value will depend on receiver termination and common mode voltage bias method and be either one of 4 possible values.

2.2 Fault Blocking

Because of the “fault blocking” capability of the coupling capacitor, certain fault can only be detected by using both DC and AC boundary-scan test. Difficulties are lie in the behavior of coupling capacitor where only transitional information is transmitted such that only fault that does create transition may only be propagated and any fault that bypasses capacitor by enabling the transition to pass through without help from the capacitive transmission media. Furthermore there is multiple fault behavior from single defect especially by the reference voltage bias circuit and the termination circuit induced faults where the faults can be masked by the other healthy differential signal line.

2.3 Proposed Fault Syndrome

Since there are infinite levels of faulty condition within an analog domain, it is difficult and time consuming to specify overall fault coverage by enumerating all different defect types and related faults unless the faults are well defined and their fault syndromes are well known for a given technology.

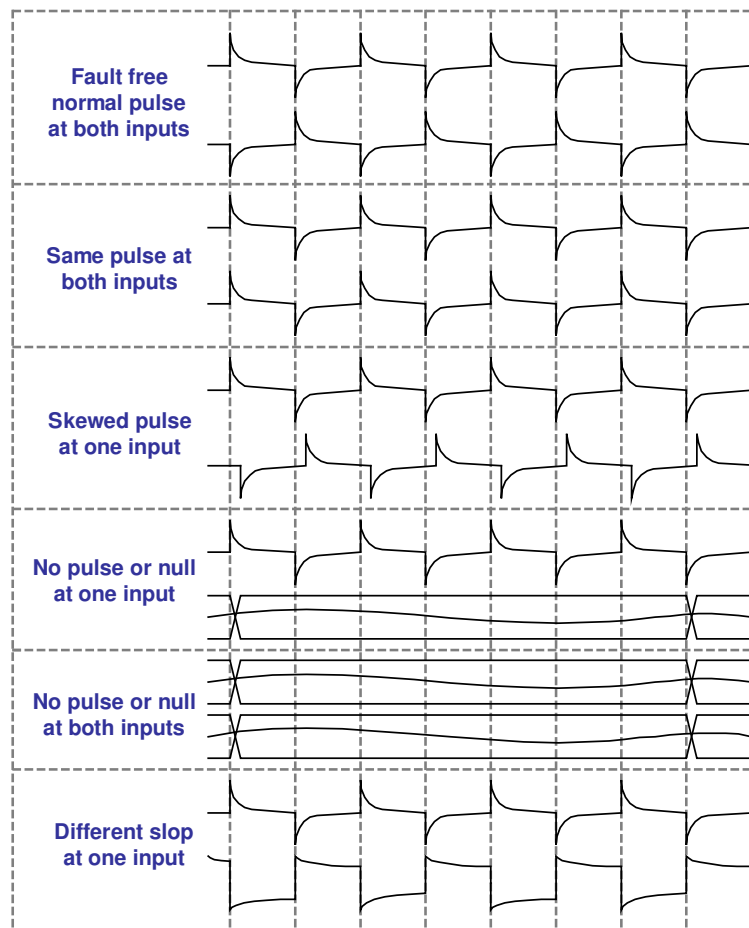


Figure 7: Faulty Input Pair Signals by Fault Syndromes

Predefined fault syndromes derived from the faulty input patterns are presented and the syndromes are used as a matrix to demonstrate effectiveness of the proposed test buffer. Defects are then mapped to different faulty input patterns and are analyzed again to determine fault coverage for the given fault syndrome.

The typical fault syndromes are shown in Figure 6. Each faulty input pattern to a differential receiver is a result of different types of defects on the differential nets.

Table 4 shows the correlation between fault syndromes and faults in LVDS and CML (*To Be Determined*) technology. Fault coverage for each syndrome is also shown. The fault detection circuit examples are presented in the next section. The column “LVDS fault map” is based on the presentation titled “Fault Analysis for LVDS” posted in www.acextest.org. Faults in the table are described according to the following notations.

Fault Syndrome	Single scan cell		LVDS Fault Map	CML Fault Map (Not Available)	Defect Map
	AC Test	AC & DC Test			
Normal Pulse	No	Yes	S (PB, PA), S (NB, NA)		
Same Pulse at Both Legs	Yes	Yes	O (PB), O (PA), O (NB), O (NA)	O (PB), O (PA), O (NB), O (NA), S (NA, PB), S (NB, PA)	
Skewed Pulse at Both Legs	Yes/No	Yes/No		SC (NB, PB), SC (NA, PA)	
Pulses at Only One Leg	Yes	Yes	S0 (PB), S1 (PB), S0 (PA), S1 (PA), S0 (NB), S1 (NB), S0 (NA), S1 (NA)	S (PB, PA), S1 (PB), S0 (PB), S1 (NB), S0 (NB), S0 (PA), S0 (NA), SF (PA), SF (NA)	
No Pulse at Both Legs	Yes	Yes	S (PB, NA), S (PA, NB)	S (PB, NB), S (NA, PA), S (NB, NA), S1 (PA), S1 (NA)	
Different Slope Pulses	Yes/No	Yes/No			

Table 4: Coverage Viewed From Input Patterns (*will be updated*)

Fault are notated in the format, Fault (Net)

Fault: S - Short, O - Open, S0 - Stuck-At-0, S1 - Stuck-At-1, SC – Capacitive Short, 0.01μF, SF – Stuck-At-Frequency, same amplitude, out of phase.

Net: Each net is specified with two characters, the first character represents the polarity of the net, either the P (Positive) or N (Negative) signal. The second character represents the location of the fault, either B (Before coupling capacitor) or A (After coupling capacitor). For many short fault examples, multiple faulty signal nets, separated by a comma are listed.

As shown in the Table 4, most common faults can be mapped to the faulty pattern types discussed above. Note that there are other types of faults that are not mapped yet, but can be detected by the example circuit provided in the first section.

3 Fault Coverage Analysis

The coverage analysis for different fault syndromes addressed in Section 2, are presented in this section. Since the signal received by the input test buffer is amplified and translated into the digital domain, only the digital representation of signal is used for the analysis and discussion. Discussions are based on two

different RC conditions of the AC coupled nets. The first one is when the AC pattern sample value in the MSA proposal is not significantly different than the driven value at the driver due to a relatively large RC value. In this case, the RC value is more than a half cycle of the AC pattern frequency. It is referred to as **large-RC**. The other case is for the RC value much smaller than the AC pattern cycle time. The shape driven by the driver is no longer maintained at the receiver. It is referred to as **small-RC**.

3.1 Large-RC case study

Figure 7 shows three different waveforms. The first case depicts a driver and a receiver working under normal operating conditions without defects. The second case shows the same pulse for both differential signal pair. The third case shows one side of input signal skewed from the other side of differential input pair. The left figures for the given cases are for the expected logic 0 value at the receiver and the right figure is for an expected logic 1. As a differential driver sends logic 0, the expected recovered value at Q should be the same logic 0 value.

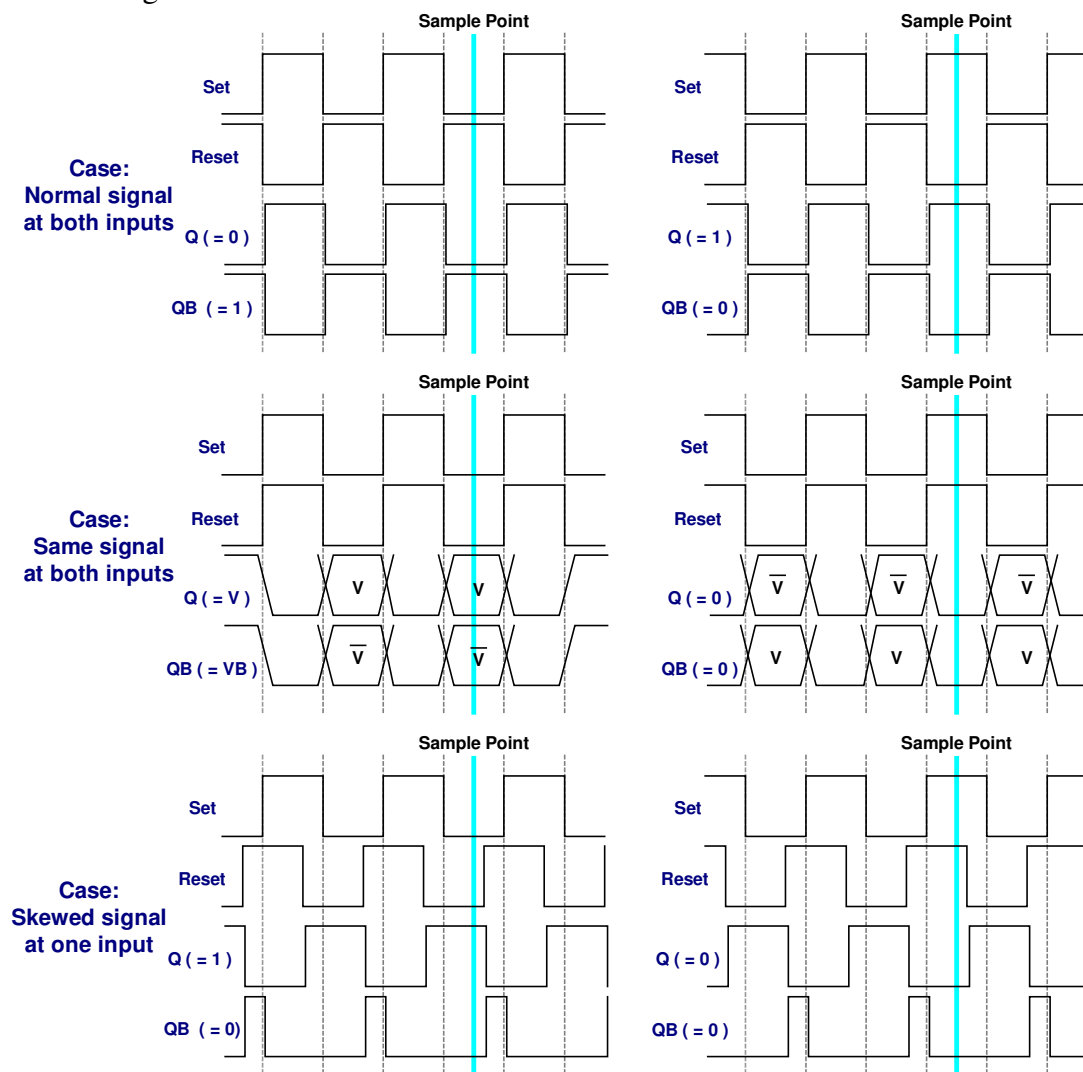


Figure 8: Large-RC examples

For all waveforms, the input pair (i.e. Set and Reset) and output pair (i.e. Q and QB) signals of the RS

latch are shown. Note that the set and reset inputs to the RS latch are the digital voltage levels after incoming signals are amplified and mapped to a digital logic signal. Set and reset are specified in pair (S value followed by R value) throughout the remainder of this paper, where the logic signal S is for the Set and the logic signal R is for the Reset of the RS latch. Note that the AC signal sample point is located at the middle of the stable logic level where the AC_Sync pulse creates the rising edge. This is based on the proposed MSA AC-Boundary-scan architecture.

3.1.1 Same Pulses in Both Inputs

When the same phase pulses are driven to both differential signal inputs, the RS latch receives either 1 or 0 for both SR inputs. When both SR inputs are logic 1's, the Q and QB are forced to logic 0 regardless of the previous Q and QB states. However when both SR inputs become logic 0 from logic 1, the values at Q and QB can be indeterminate, the final state depends on the arrival time of set and reset. Because of this, the logic state at the sample point is labeled as "V" for Q. "VB" is labeled for QB since QB has the complement logic state of Q. This fault type can be partially detected by running one specific pattern type. However when logic 1 is used as a test pattern, then the value sampled will always be 0 for both Q and QB output.

3.1.2 Skewed Pulse in One Input

The third row in the figure shows a skewed input signal at one side of differential signal pair. When logic 0 is expected, the (S, R) value at the sample point is (0, 0) followed by (0, 1) respectively. The Q value becomes 0 at (0, 1) and the Q value is maintained when (S, R) becomes (1, 1). Note that this condition occurs when the skew is greater than a half TCK cycle with 50 % duty cycle. When logic 1 is expected, Q and QB become logic 0 because the (S, R) input is (1, 1) with skew greater than a half TCK cycle. The granularity of detecting such faults can be increased by either increasing TCK frequency or by reducing the duty cycle while maintaining the same frequency. As one can see, a skewed signal relative to signal Set is the Reset signal, and the Q output of the RS latch follows the complement value of the Reset signal.

3.2 Small-RC case study

The same type of analysis is made for the small RC case. Figure 8 show the short pulses at the set and reset inputs of the RS latch. The Q and QB outputs become logic 1 and 0 as (S, R) value of (1, 0) and (0, 1) pulses are applied to the RS latch. The Q and QB logic state is maintained as the (S, R) pattern becomes (0, 0). The Q and QB logic state value is reversed when a (S, R) value of (0, 1) reset pulse is applied to the RS latch. As a result of this sequence of events, the original signal waveform is reconstructed from the set and reset pulse trains. Please note the signal state at the sample point is in a stable condition.

3.2.1 Same Pulses in Both Inputs

When same phase pulses are driven to both differential signal inputs, the RS latch receives (0, 0) followed by (1, 1) for SR inputs. A value labeled as "V" is established at Q during the transition and QB output becomes "VB" for the same reason as in the larger-RC example discussed earlier. The same

phenomenon happens when the expected value is 1. As a result, the sampled value will be the same for both situations.

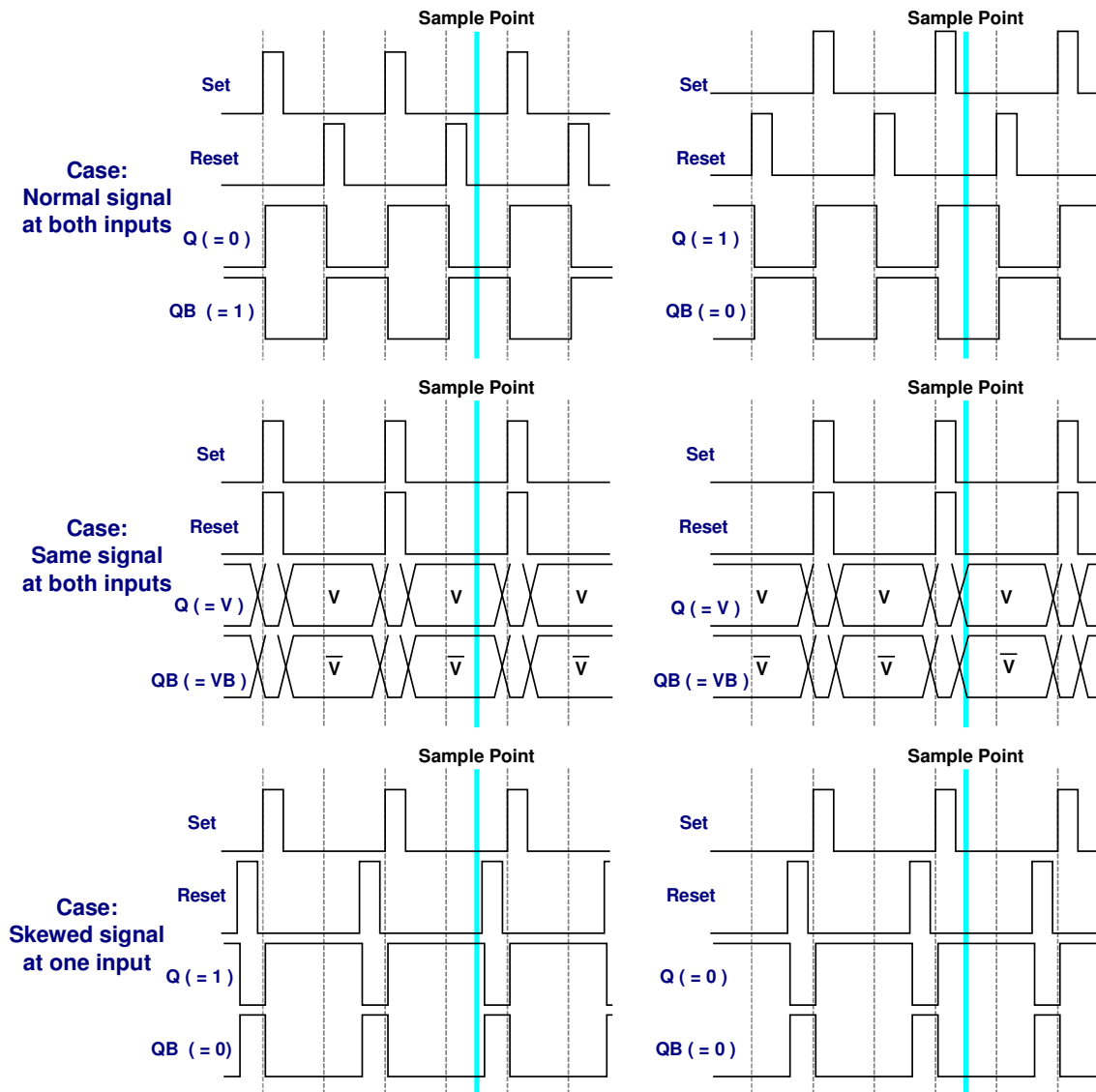


Figure 9: Small-RC examples

3.2.2 Skewed Pulse in One Input

The third row in the figure shows skewed reset input signal at one side of differential signal pair. For both expected value 0 and 1, the (S, R) value at sample point is (0, 0) followed by (0, 1). As a result, Q value is same for both situations. As in larger-RC example, the skew is greater than a half of TCK cycle.

3.3 Detection Mechanism for Heterogeneous Coupling Capacitance

This section briefly discusses the fault detection mechanism when a different size coupling capacitor is placed in one of the AC coupled differential input pair. The left column in Figure 9 shows two pulses with different width at the set and reset inputs of the RS latch. Notice that the (S, R) value is different at sample point. The right column shows an example circuit implementation to detect such a fault syndrome.

The “Set” signal is sampled by odd TCK clock cycle or AC pattern clock cycle while “Reset” is sampled at even TCK clock cycle. “Set on Odd TCK” (SOT) and “Reset on Even TCK” (RET) generated by two flip-flops are Exclusive-ORed for further usage. Again, granularity of detecting such faults caused by different capacitor size can be increased either by increasing TCK frequency or by reducing the duty cycle of TCK.

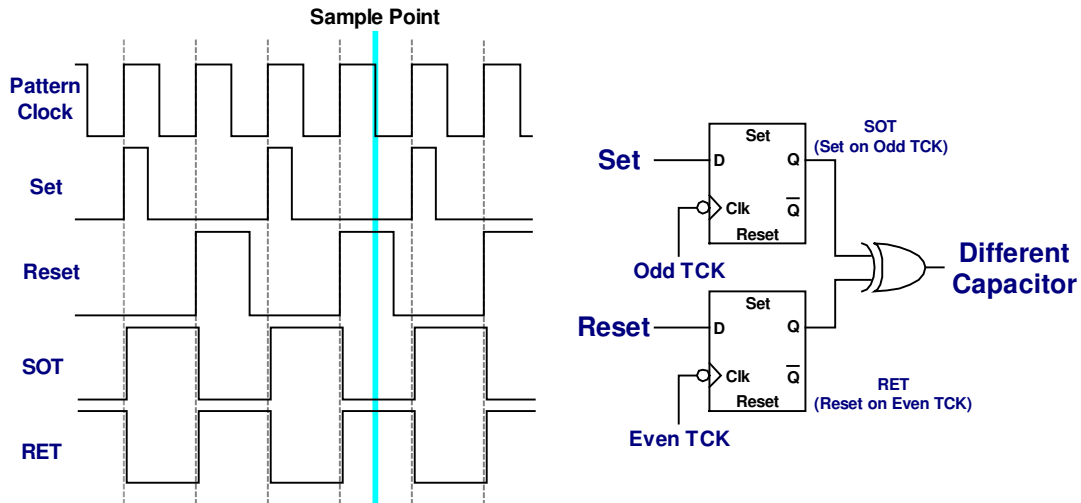


Figure 10: Different Coupling Capacitance at Differential Pair

4 Set Delayed Signal Recovery Mechanism

An additional signal recovery mechanism is presented in this Section in order to avoid sampled signal ambiguity when the sample point coincides with transition point of recovered signal. When both the Set and Reset signal coincide because of a short defect for example, the signal recover RS latch becomes unpredictable when both the Set and Reset return to logic zero at the same time. To avoid uncertainty during this condition, a unit delay of given technology is added in the Set signal path to delay the Set operation. More stable sample of recovered signal is possible as shown in Figure 11. By delaying the Set signal, the recovered signal has “high” logic priority such that fault will show up as “1” more often than “0” and “0” test pattern will detect more fault than the “1” patterns. The “0” test pattern must be executed first to reduce test time.

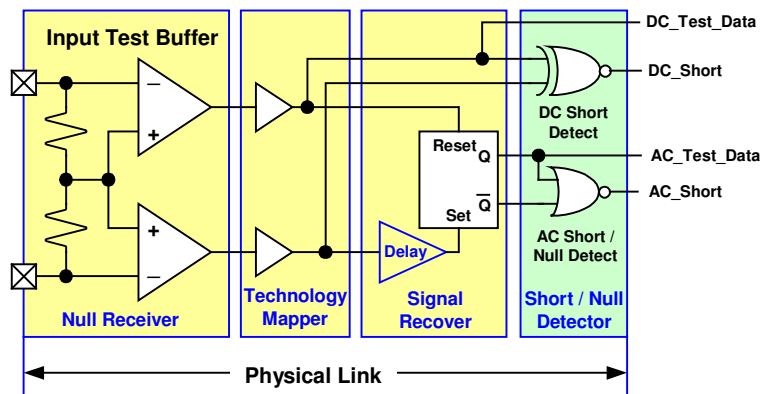


Figure 11: Set Delayed Signal Recovery Examples

Figure 12 illustrate improved condition around the sample point and Figure 9 middle waveform shows the same condition without the set delayed recovery mechanism.

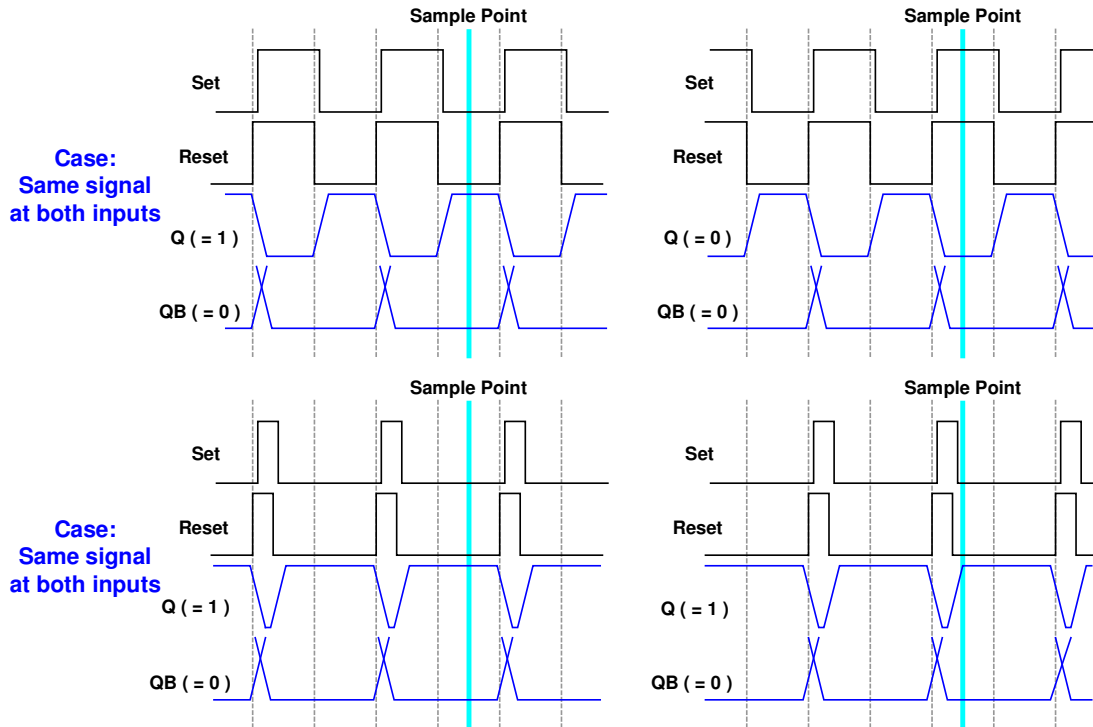


Figure 12: Set Delayed signal recovery for the same signal at both inputs

The AC short fault condition during transmission through the Small-RC time constant is short lived. The Small-RC example discussed earlier shows such effects. However by using the set delayed recovery mechanism, such short conditions can be preserved within the recovered signal and the faults can be detected without ambiguity when both “0” and “1” test pattern are used.

5 Suggested Input Test Buffer Design Parameters

Preferred input test buffer design parameters are summarized in Table 5. Chapter 6 shows examples of preferred implementation of the input test buffer for both single and two boundary-scan cell interfaces.

Input Test Buffer Configuration			
Null Detection Method	Null Detection Range (Comparator Window)	Common Mode Reference Voltage: Vref	Input Test Buffer Bandwidth
Window Comparator	1/3 of Maximum Differential Input Signal Voltage: (Max. V_{IH} – Min. V_{IL}) / 3.	Low impedance common mode reference voltage	From DC to minimum of $(1 / (0.693 \cdot RC))$ as the maximum bandwidth or 20 MHz, whichever is higher frequency

Table 5: Input Test Buffer Design Parameters

With 20.88 MHz TCK clock speed (0.693 RC for 1nF coupling capacitor), up to 1nF coupling capacitor can be used to perform direct AC signal sampling without even using the signal recover RS latch since the signal decay to 50% of full amplitude takes 34.65 nS and 33.33% of full amplitude takes 54.9 nS. The 20.88 MHz TCK clock speed is 47.89 nS long and the AC_Sync signal happens at 23.9 ns, which is a half the TCK cycle, where the incoming signal is only decayed to less than 60% (0.510 RC) of full amplitude and well above 1/3 of full signal range (54.9 nS or 1.098 RC) where the input test buffer threshold range is defined.

6 Example Schematics Diagram of Input Boundary-scan interface

This chapter shows variations of the boundary-scan cell interface for the two or four window comparator based input test buffers. Advanced features discussed in “3.2.2 Skewed Pulse in One Input” and “6 Set Delayed Signal Recovery Mechanism” are not incorporated in the examples.

6.1 Differential Input Test Buffer for single boundary-scan cell interface

In order to interface multiple fault syndromes into a single boundary scan-cell value, the DC_Short, the AC_Short, and the No_AC_Detect signals are generated with various detector circuits and combined with the DC_Test_Data and the AC_Test_Data signals to form the DC_Data and the AC_Data signals for the boundary-scan cell. Since error information is encoded into a single data bit for the boundary-scan cell, this configuration will lose diagnostic information for determining the cause and source of failure. Based on various Spice simulations conducted with the similar input test buffer demonstrated that test coverage is comprehensive for all proposed fault syndromes.

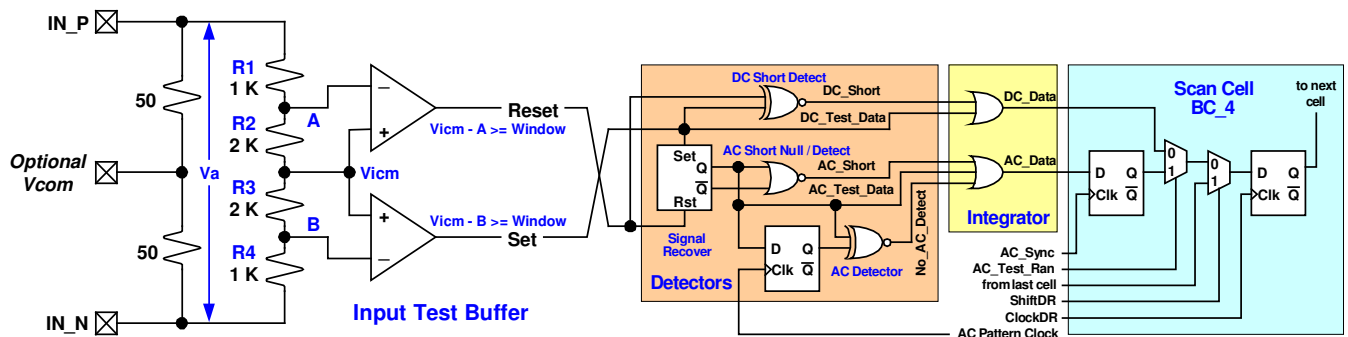


Figure 13: Differential input test buffer interface with single boundary-scan cell

6.2 Differential Input Test Buffer for two boundary-scan cell interface

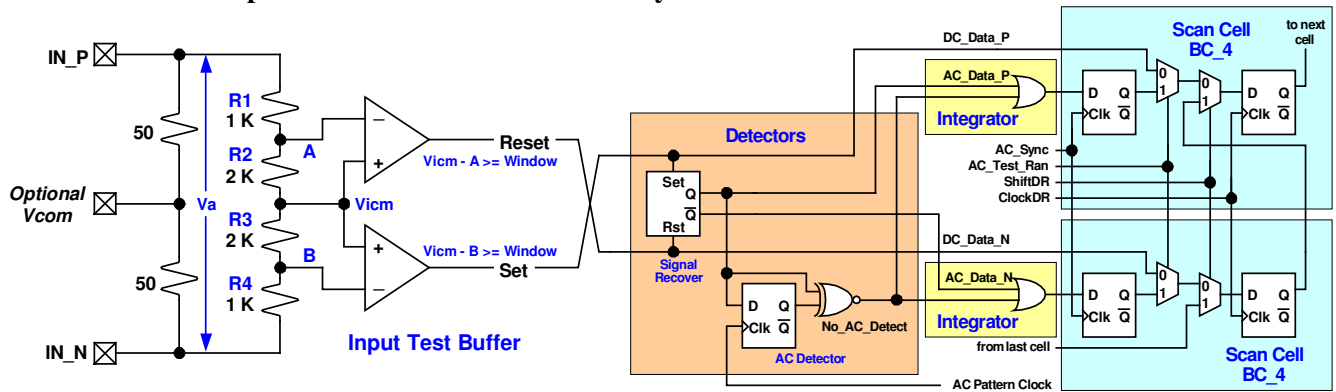


Figure 14: Differential input test buffer interface with two boundary-scan cell

In Figure 14, all short related detection circuits are removed since the DC_Short and the AC_Short failure information are available from two boundary-scan cells.

Even though there are two boundary-scan cells in this example, there will be no significant improvement on diagnosability over previous example, because differential window comparators used in the input test buffer receive evenly distribute failure information across resistor networks. The differentially detected fault may come from either one of the differential signal input, the IN_P or the IN_N, and the window comparator only sees differential result of the failing signal. The test coverage remains the same as the previous example.

6.3 Dual Differential Input Test Buffer for two boundary-scan cell interface

Figure 15 shows different input buffer configuration where the V_{ref} is from a low impedance voltage source. The Reset signal for the IN_P and the Set signal for the IN_N take reference input from the other differential signal input such that if the input common mode voltage value V_{cm} is the same as V_{ref} , which will be the optimal interconnect case, the input test buffer behaviors the same way as the previous examples. However, if one of the differential signals is out of functional range because of defects, both differential and single ended window comparison will make up the set and reset signal pair signals. These signals under error condition will provide additional diagnostic information for debugging. Since the window used in this example also follows the suggested 1/3 value of full input signal range, the circuit should maintain the same test coverage as all previous examples.

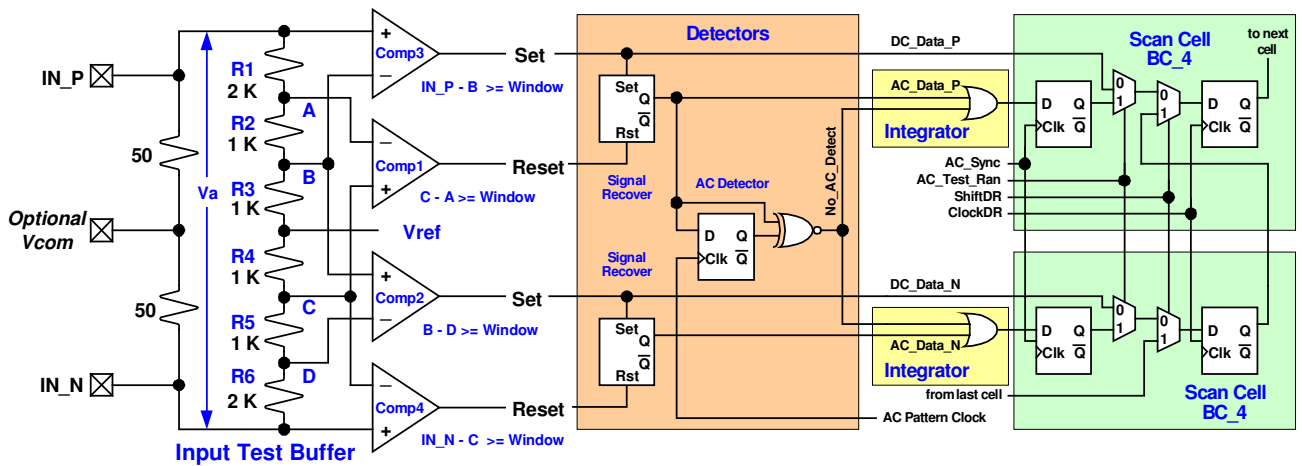


Figure 15: Dual differential input test buffer interface with two boundary-scan cell 1

6.4 Dual Differential Input Test Buffer for two boundary-scan cell interface

The Figure 16 has an additional DC_Short detection circuit. Since the DC_Data is taken from either the Set or Reset signal of the signal recoverer and single ended view of the window comparator, the DC_Short signal will provide more comprehensive error information for each test vector. No additional test coverage will be made from added short detection circuit.

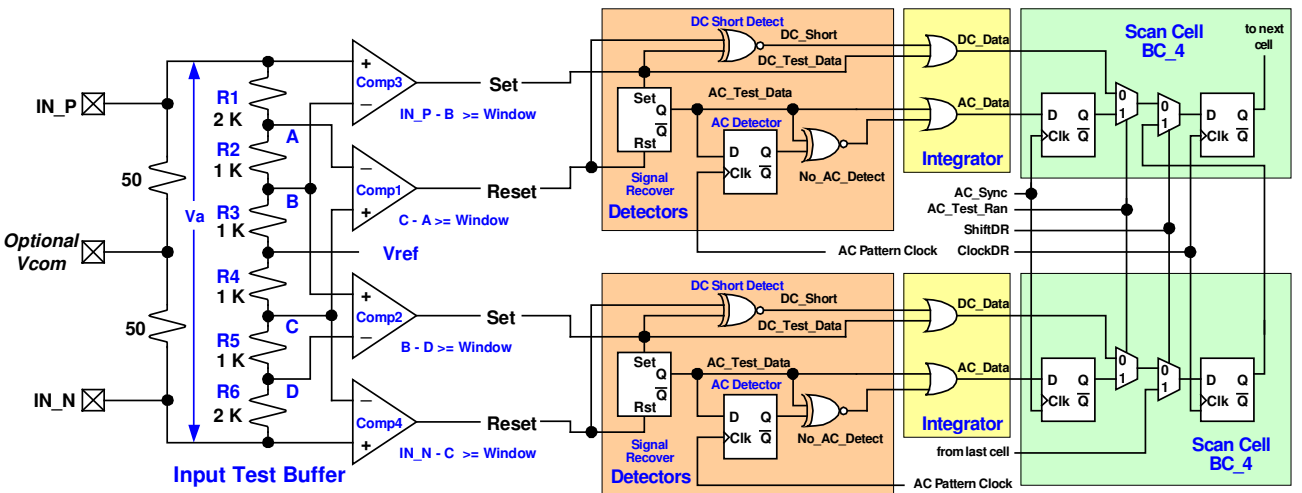


Figure 16: Differential input test buffer interface with two boundary-scan cell 2

7 Spice Simulation Examples

To be updated when the data is available.

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