

# Edge Detection with Throat-Clearing

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## 1 Introduction

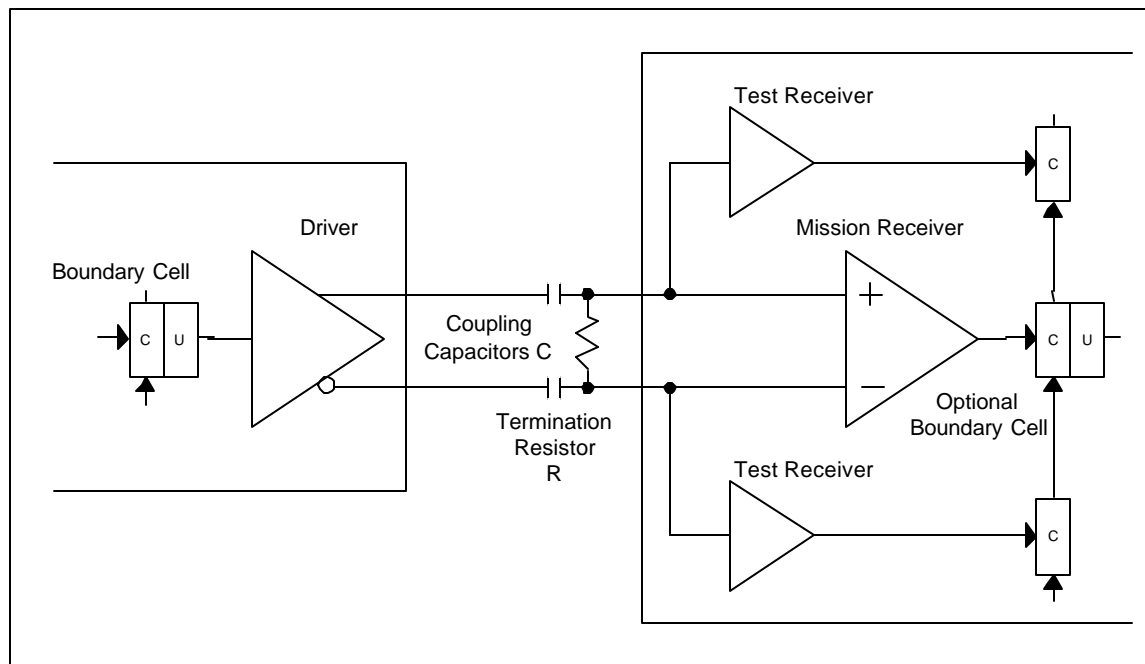
This document describes the details of a proposed solution for testing AC-coupled nets between integrated circuits on printed circuit boards or in systems. Traditionally, such interconnect has been DC-coupled and can thus be tested with well-known Boundary-Scan methods, specifically with the EXTEST instruction as codified in IEEE Std. 1149.1. However, the use of AC-coupling disallows DC-based techniques, giving rise to the need for an extension of Boundary-Scan into the AC realm.

The AC EXTEST Working Group (now IEEE P1149.6) had studied several possible technical solutions to enable AC Boundary-Scan. This proposal initially came about by combining several of the ideas that the group has been considering, with the edge-detection being proposed by Ken Parker of Agilent and the throat-clearing by Carl Barnhart of IBM.. The combined result was a radically simplified approach to addressing the AC EXTEST problem.

This document combines those two original documents and fills out the proposal and brings it up to date with the latest information and decisions regarding the Test Receiver defined in Chapter 6 of the draft P1149.6 Standard (currently at level 2.3n.)

## 1 2 AC-Coupled Differential Channel

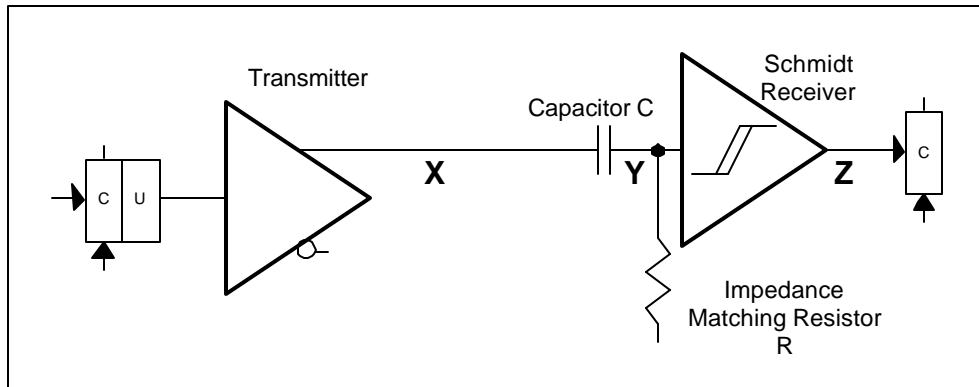
2 Figure 1 shows a general differential channel with P1149.6 differential Boundary-Scan control  
 3 and single-ended observation. It shows a boundary cell on the mission receiver, which is optional  
 4 for P1149.6, but may be required for IEEE 1149.1 instructions such as RUNBIST or INTEST.  
 5 This proposal requires two Test Receivers (one per leg) and the associated observation boundary  
 6 cell (no Update flop) in addition to the traditional IEEE 1149.1 “analog” test structures.



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 8 **Figure 1: General structure of an AC coupled differential channel with Boundary-Scan testability.**

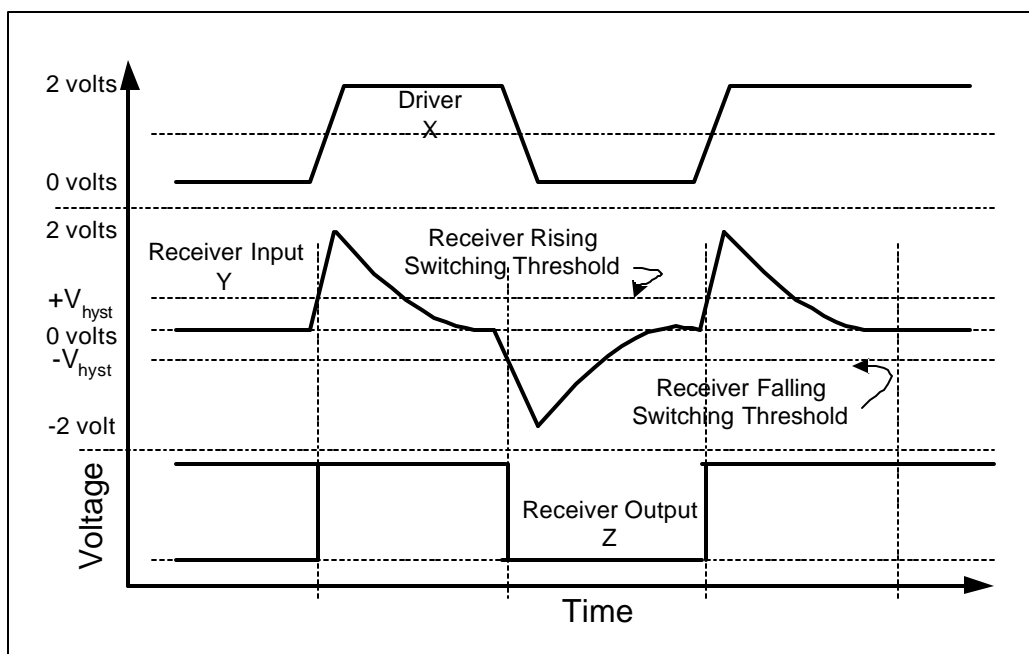
9 On the drive side, while in test mode, the edge speeds of the transmitted signals must be the same  
 10 as those when in system mode. The AC\_EXTEST Boundary Cell at the driver is modified, as  
 11 described later, so that during AC\_EXTEST two transitions are sent across the channel in  
 12 addition to any transition that occurs at Update\_DR or Update\_IR. Behavior during traditional  
 13 EXTEST is per the IEEE 1149.1 Standard.

14 On the receive side, the Test Receivers shown are hysteretic, have special behaviors that are  
 15 turned on or off by loading AC\_EXTEST and EXTEST, and are designed in accordance with  
 16 Chapter 6 of the P1149.6 draft. When EXTEST is in effect, the receiver digitizes the DC value  
 17 appearing on the pin immediately upon entry to the Capture\_DR TAP state, if it is at a valid level,  
 18 and returns a default value otherwise. When in AC\_EXTEST, the receiver output follows any  
 19 valid transitions at the input pins and holds that value until the next transition, or returns a default  
 20 value if there are no valid transitions. This *integrating* feature of the receiver reconstructs a  
 21 replica of the DC levels produced by the driver, assuming the transitions reach the receiver. One  
 22 leg of this test path is shown in Figure 2 (no mission receiver shown.) Waveforms seen at the  
 23 driver, receiver input and receiver output are shown in Figure 3 when AC\_EXTEST is in effect.



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2 **Figure 2: The test path of the positive leg of Figure 1. When AC\_EXTEST is in effect, the test**  
 3 **receiver integrates the pulse stream.**



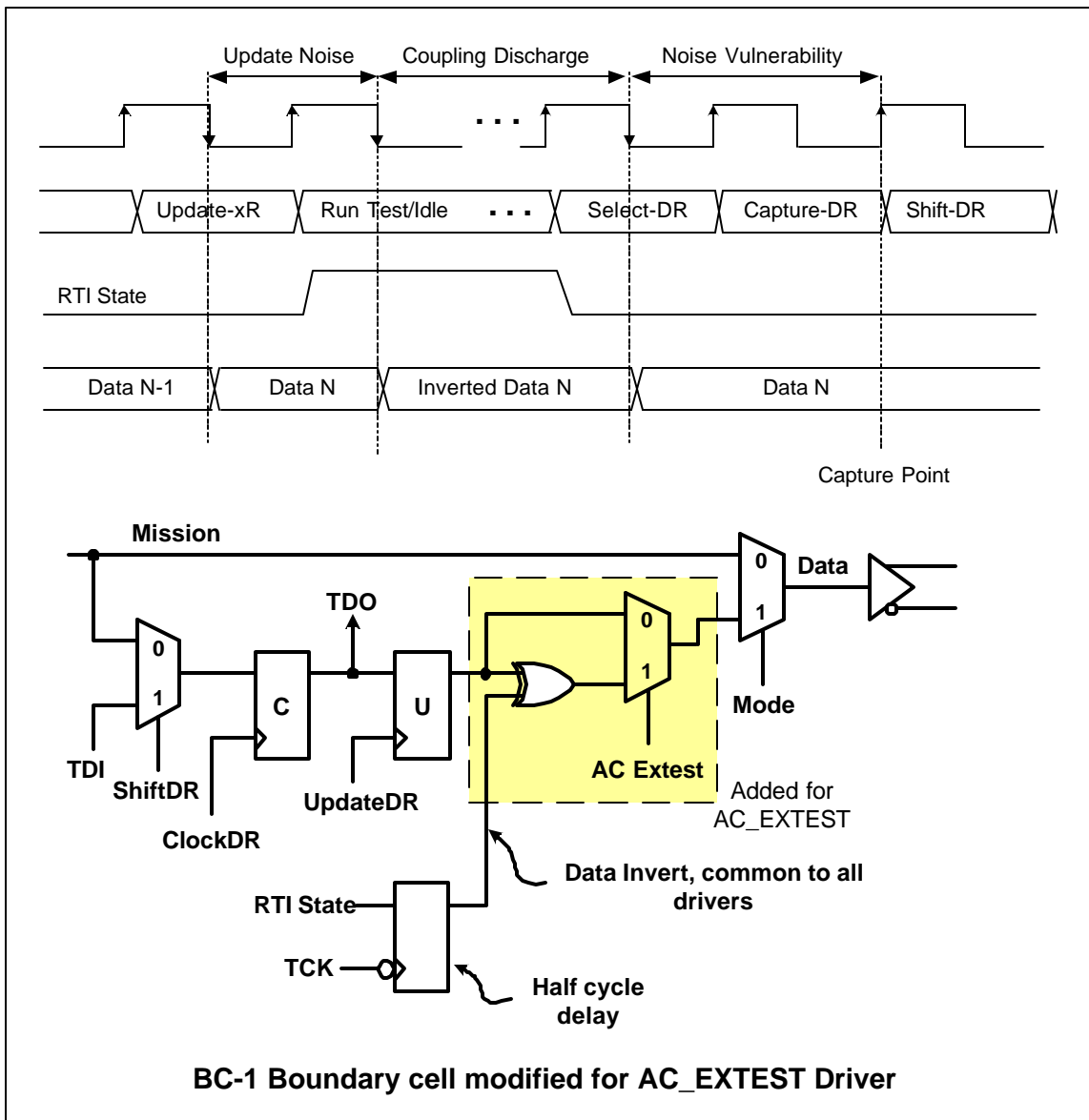
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5 **Figure 3: Test waveforms, seen at points X, Y and Z in Figure 2, when AC\_EXTEST is in effect. The**  
 6 **voltage hysteresis thresholds shown here are arbitrarily, and the time hysteresis and propagation**  
 7 **delays are not shown at all. Initial value of the receiver output is unknown, and due to noise, it's**  
 8 **value after the initial transition may still be unknown.**

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### 3 Proposed AC\_EXTEST Output Cells

First, modify the driver boundary cell by adding the circuits shown in the yellow box in Figure 4 between the update latch and the output to the driver. This can be done for any of the output boundary cells shown in IEEE 1149.1. The TAP supplies the TAP-state decode for Run-Test/Idle (RTI) synchronized to the falling edge of TCK. Upon entry to the RTI state in AC\_EXTEST, the driver output would toggle after the falling edge of TCK to the opposite of the value in the update latch. Upon exit from the RTI state in AC\_EXTEST, the driver would again toggle after the falling edge of TCK back to the same value in the boundary cell. These two additional transitions are referred to as “throat clearing”, as they are intended to eliminate unknown initial states, or any unintended state due to noise, from the hysteretic Test Receivers. (These extra transitions could be avoided by not transitioning the RTI state, giving the same driver behavior as EXTEST.)

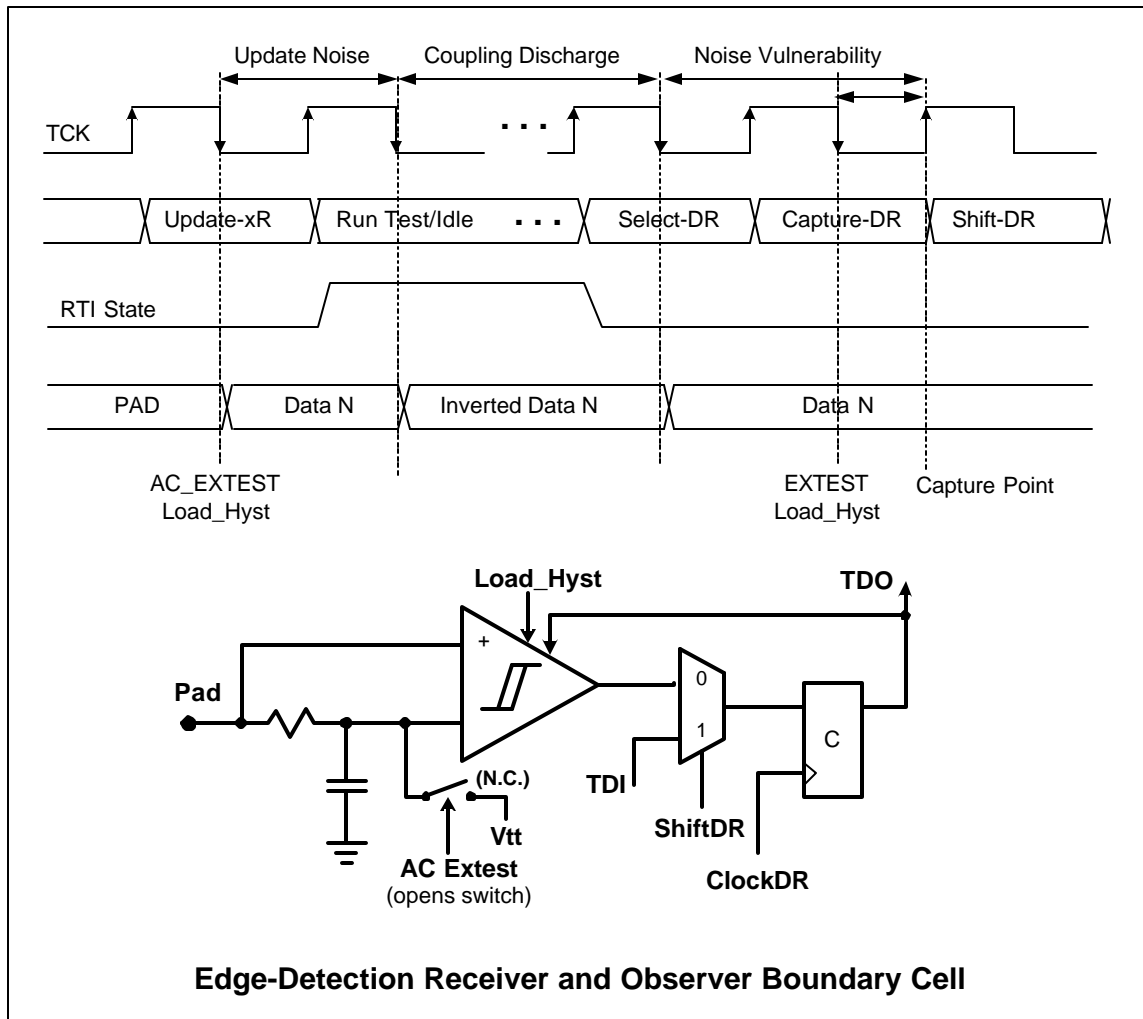


12  
13 **Figure 4. Driver Boundary Cell Modifications and timing diagram.**

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## 1 4 Proposed AC\_EXTEST Input Cell

2 As previously mentioned, the proposed input cell uses the hysteretic Test Receiver as defined in  
 3 Chapter 6 of the Draft Standard (currently version 2.3n). The data from the hysteretic receiver is  
 4 loaded directly into the scan flop of the boundary cell. As the boundary cell is an observation  
 5 cell, there is no requirement for a separate Update flop, but the hysteresis of the Test Receiver  
 6 needs to be preset to a tester supplied value, so the Test Receiver hysteresis is controlled the same  
 7 way an Update flop would be controlled. That is, the value in the scan flop of the boundary cell  
 8 is taken to the data input of the Test Receiver hysteresis preload, and a clock signal from the TAP  
 9 is used to load that value into the Test Receiver. Figure 5 shows the proposed structure.



10

11 **Figure 5. Proposed AC\_EXTEST receiver and timing diagram.**

12 The "Load\_Hyst" signal comes from the TAP. In AC\_EXTEST, it is essentially the same as the  
 13 "Update\_Clk" from IEEE 1149.1, and has its capturing edge is no later than the falling edge of  
 14 TCK in Update\_DR TAP-state. In EXTEST, however, it has its active edge coincident with the  
 15 falling edge of TCK in the Capture\_DR TAP-state.

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## 1 5 Proposed TAP Changes.

2 The proposed changes to the tap are minor: three additional outputs. As shown in the previous  
3 two sections, they are the decode of the P1149.6 mandatory instruction AC\_EXTEST to both  
4 input and output cells, the RTI TAP-state decode synchronized to the falling edge of TCK to the  
5 output cells, and the Load\_Hyst clock to the input cells.

6 These signals, and their use in these diagrams, are instructive, not required. For instance, if Rule  
7 6.1.3.1a)ii is implemented (the input is compared to a fixed reference instead of a recent average),  
8 then the low-pass filter and the switch controlled by AC\_EXTEST at the negative input of the  
9 comparator in Figure 5 would not be needed. Also, if the TAP designer supplied a signal that was  
10 the logical AND of the AC\_EXTEST decode and the synchronized RTI TAP-state decode, then  
11 only that single additional control signal would need to be supplied to the output cells. The XOR  
12 and MUX shown inside the yellow box of Figure 4 could then be reduced to a single XOR gate.  
13 Such details of internal design are left to the chip implementers.

## 14 6 Operation

15 If the AC\_EXTEST instruction is loaded in both the driver and receiver chips, and both the driver  
16 and receiver are connected to AC pins and support P1149.6, whether AC or DC coupled, then:

- 17 • Immediately following Update\_DR, there may or may not be a transition at the driver. In  
18 the Test Receivers, default values from the boundary scan cell associated with the  
19 receiving pin are loaded into the hysteresis circuits (timing to be defined in Chapter 6).
- 20 • Upon entry to Run-Test/Idle (RTI) TAP-state, the driver will toggle on the first falling  
21 TCK to the opposite of the value in the driver boundary cell. This transition may be a  
22 “valid” transition at the receiver pins, but need not be. In particular, there has been no  
23 delay to allow any preceding transitions or noise to decay to a null, which may affect the  
24 transition amplitude.
- 25 • The tester holds the test board in RTI state for a sufficient time for all AC-coupled nets  
26 on the board to decay to a null condition (about 5 times the longest time constant on the  
27 board). This is to ensure the maximum possible amplitude for the final transition, relative  
28 to the common mode voltage or the self-referenced voltage.
- 29 • Upon exit from the RTI TAP-state, the driver will toggle on the falling TCK in the  
30 Select\_DR\_Scan TAP-state, to the expected value based on the driver boundary cell.  
31 This transition must be a “valid” transition for the defect-free case, and forces the Test  
32 Receiver hysteresis to the expected value, matching the driver boundary cell. There is no  
33 additional delay prior to capture added or desired at this point, since only the transition is  
34 required, and this represents a period when the Test Receivers are vulnerable to noise.
- 35 • In the Capture\_DR TAP-state, the value held in the hysteresis is transferred to the scan  
36 cell on the rising edge of TCK.

37 If the EXTEST instruction is loaded in the driving chip, then the driver performs in accordance  
38 with IEEE 1149.1. (If the AC\_EXTEST instruction is loaded in the driving chip, and the driver is  
39 not attached to an AC pin, then it will also perform in accordance with the IEEE 1149.1 EXTEST  
40 instruction - it will not be modified as shown above.)

- 1 If the EXTEST instruction is loaded in the receiving chip, then the Test Receiver of AC pins will  
2 be held in the default state until (default state will be loaded at) the fall of TCK upon exit of the  
3 Select\_DR Tap-state (entry to Capture\_DR TAP-state). This will allow any transitions or noise  
4 that occurred at Update\_DR to decay without affecting the hysteretic comparator. If necessary,  
5 the tester should spend an appropriate amount of time in the RTI state to ensure this. During  
6 Capture\_DR, if the inputs are still at a valid level, the hysteresis will take on that value. The final  
7 hysteretic value will be transferred to the boundary scan cell on rising TCK in the Capture\_DR  
8 TAP-state. This is to ensure that an AC coupled, defect-free, net will detect a “float” and return  
9 the default value, but that a shorted capacitor will produce a result that matches the driving cell.
- 10 If an AC pin on a driving chip with the AC\_EXTEST instruction loaded is DC coupled to a  
11 receiving pin that is a DC pin, or an AC pin with the EXTEST instruction loaded, the presence or  
12 absence of the extra transitions should not disrupt the value captured by the receiver, and the use  
13 of either EXTEST or AC\_EXTEST on the driving chip should be permitted.
- 14 If an AC pin on a driving chip with the AC\_EXTEST instruction loaded is AC coupled to a  
15 receiving pin that is a DC pin, then the coupling capacitor must be large enough that the time  
16 from exiting RTI on the falling edge of TCK to the rising edge of TCK in Capture\_DR is less  
17 than one time-constant for the coupling network. Use of this connection with the EXTEST  
18 instruction loaded in the driving chip will produce indeterminate results as there may be no  
19 transitions from the driver, and its use should be discouraged.
- 20 If a pin on a driving chip is not an AC pin, or the chip has the EXTEST instruction loaded, and it  
21 is DC coupled to a receiving pin that is an AC pin, the Test Receiver should still capture the  
22 correct value, particularly if the receiving chip has the EXTEST instruction loaded. Values  
23 captured when the receiving chip has the AC\_EXTEST instruction loaded may need to be ignored  
24 by the tester in this case when there is a change in the hysteresis threshold between EXTEST and  
25 AC\_EXTEST.
- 26 If a pin on a driving chip is not an AC pin, or the chip has the EXTEST instruction loaded, and it  
27 is AC coupled to any receiver, then a very large coupling capacitor is required. This is to ensure  
28 that any transition from Update\_DR will not decay before it can be captured in the receiver  
29 boundary cell. Test operation in this case is possible but problematic, especially since there may  
30 not even be a transition at Update\_DR, and should be discouraged.
- 31 Of course, if the pin on a driving chip is not an AC pin, and is DC coupled to a receiving pin that  
32 is not an AC pin, then 1149.1 rules govern the behavior in either EXTEST or AC\_EXTEST.
- 33

1 To summarize this into a table:

Driver		Coupling	Receiver		DC Compat.	Capture Result	Comments
Pin	Inst.		Pin	Inst.			
-	-	DC	-	-	No	'X'	Functional design defect
DC or DCX		DC	DC	-	Yes	Data	IEEE 1149.1 test.
DC or DCX		DC	AC	DCX	Yes	Data	Permitted
DC or DCX		DC	AC	ACX	Yes	'X'	Vhyst-edge may prevent capture
AC	ACX	DC	DC	-	Yes	Data	Permitted
AC	ACX	DC	AC	DCX	Yes	Data	Permitted
AC	ACX	DC	AC	ACX	Yes	Data	Preferred differential test
DC or DCX		AC	DC	-	-	'X'	Discouraged, 50% no transition at Update_DR.
DC or DCX		AC	AC	DCX	-	'X'	Discouraged, 50% no transition at Update_DR.
DC or DCX		AC	AC	ACX	-	'X'	Discouraged, 50% no transition at Update_DR.
AC	ACX	AC	DC	-	-	Data	Permitted with large cap.
AC	ACX	AC	AC	DCX	-	Data	Permitted with large cap.
AC	ACX	AC	AC	ACX	-	Data	Preferred AC-coupled test

2 **Nomenclature:**

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- In any entry, "--" indicates "don't care".
  - Driver and Receiver Pin may be AC pins (P1149.6) or DC (1149.1) pins. (See glossary of P1149.6 draft.)
  - Driver and Receiver Inst(ruction) may be EXTEST (DCX) or AC\_EXTEST (ACX).
  - Coupling may be AC or DC (should be obvious.)
  - DC Compat(ability) refers to whether DC coupled driver and receiver have compatible common mode voltages and voltage swings.
  - Capture results may be either the intended DATA (true or inverted copy of the value in the driver boundary scan cell), or indeterminate ('X').
  - Comments are generally brief. "50% no transition at Update\_DR" refers to the fact that, in EXTEST, there will be a transition only about 50% of the time, with indeterminate results when there is no transition. "Vhyst-edge may prevent capture" refers to the fact that Vhyst-edge may be substantially larger than Vhyst-level, possibly preventing detection of legitimate DC signal level.

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## 1 7 Pro/Con Analysis

2 There are a number of advantages to this approach.

- 3 1. The modification to the driver cell is minimal.
- 4 2. The receiver is just the Test Receiver connected to an observer boundary cell. There  
5 are no counters or dividers needed.
- 6 3. Depending on implementation, only two to three new global (TAP to boundary  
7 register) signals are required.
- 8 4. There is no need for a new frequency or clock source.
- 9 5. The TAP design is not changed except to provide the additional mandatory  
10 AC\_EXTEST instruction decode and the additional global signals.
- 11 6. There will always be a minimum of two transitions in every AC test. The time  
12 between those transitions is controllable by the tester, based on the actual board  
13 netlist, to ensure that the final transition is robust and away from potential noise  
14 sources.
- 15 7. There are no new requirements or restrictions placed on TCK.
- 16 8. There is no need for selectively enabling the AC\_EXTEST function by pin. (If there  
17 is concern that the throat-clearing transitions could create problems for other logic on  
18 the board, whether a pin is an AC pin or not may need to be a programmable  
19 characteristic of the pin.)
- 20 9. Existing test generation and diagnostic algorithms are minimally affected, as this  
21 proposal strictly follows the “data mapping” assumptions of 1149.1 (with the legal  
22 difference of permitting the inversion between the boundary cell and the inverted leg  
23 – a situation currently recognized by most test software even though excluded by the  
24 1149.1 standard). Providing and taking advantage of default values for the receiving  
25 cells is the primary change.
- 26 10. The silicon implementation (area and power) is minimal, consisting essentially of the  
27 added Test Receiver and observer boundary cells.
- 28 11. The BSDL requirements are minimal. We still need to identify the AC pins that have  
29 this capability, but not much else. No AC/DC control cells are required.

30 There are some disadvantages.

- 31 1. Noise pulses injected into the channel can cause the hysteresis to ‘flip’ and fail a test.  
32 This is minimized with voltage and time hysteresis in the receiver, and a minimum  
33 time window of vulnerability.
- 34 2. While in almost every respect the diagnostics are unaffected, one exception is that a  
35 “stuck at” 1 or 0 will always appear to be one or the other. Thus, the stuck level can’t  
36 be reported reliably. (True for all AC\_EXTEST proposals.)
- 37 3. An existing tester that performs edge-connector test will be able to continue doing so  
38 when it is receiving from AC pins, but may need help to meet edge rate requirements  
39 when driving an AC pin. (True for all AC\_EXTEST proposals.)