FAQ: The EXTEST_TRAIN instruction is required, but it is not clear from the Standard when or why it would be used, and there is even an Recommendation to use EXTEST_PULSE unless EXTEST_TRAIN is required. So, when is it required?

A: Unfortunately, this is one of those situations where, if you need it, you know it. If you're not sure, you probably don't.

The description in the Standard says that EXTEST_TRAIN is used when an AC stability condition is required, as opposed to using EXTEST_PULSE which establishes a DC stability condition. Typical situations which might require an AC stability condition include such things as dynamic logic or analog buffers which only work at the correct edge rates and amplitudes after a minimum number of transitions.

This is not a common situation at the moment, and this instruction was included in the Standard to simply provide an alternative when needed. There are a number of unanswered questions about this instruction, and it will take time and industry experience to define the need and use of this instruction. Note also that this instruction places additional constraints on the TCK frequency, the board coupling time constants, etc. Specifically, the Test Receiver is still in AC test mode, and using the Vhyst-edge, which assumes voltage doubling from the transitions dying away between edges. There is a transition every TCK cycle, so the cycle time of TCK has to be at least Ttest (3 times the longest connectivity time constant). There may easily be situations where there is no solution to the full set of constraints. If a situation exists that requires EXTEST_TRAIN, then extra care must be exercised in determining the TCK frequency and the board coupling time constants to ensure proper operation.

FAQ: When I attempt to calculate the hysteresis value for the Test Receiver in EXTEST mode (Vhyst-level), the variation in common mode voltage specified for the driver sometimes exceeds the calculated value of the hysteresis. Doesn't this mean that the Test Receiver won't work in this case? What do I do about this?

A: Your observation is absolutely correct. Even if the variability doesn't exceed the calculated hysteresis value, it may reduce the noise margin to the point that operation in a noisy board test environment is unreliable. This inability to establish a reliable operating point for a single-ended receiver in a differential channel is why we adopted edge sensitivity for the Test Receiver. Unfortunately, in EXTEST mode, there is no choice but to try.

If you know that your chip may end up in this situation, it is best to include the optional boundary cell on the output of the functional differential receiver. This cell is only capable of detecting about half the board level defects, but that may better than having one or both of the test receivers reporting stuck-at behavior in a defect-free situation.

Attempts have been made to try to recover the common mode value from the inputs at the receiver. Our simulations indicate that defect situations can cause an erroneous recovery that may prevent detection of some defects and will definitely require changes to the diagnostic algorithms. Careful Spice simulation of the full set of defects would be necessary to verify that any such scheme works and produces results reasonably equivalent to the current solution. (The working group would be very interested in any such solution. We couldn't find one.)

FAQ: The Standard appears to allow both the coupling capacitor and the low-pass filter on chip. But this makes no sense. What gives?

A: You are correct, having both the coupling capacitor and the low pass filter on-chip makes no sense. We assumed, since an on-chip coupling capacitor means that AC coupling is guaranteed,
that such a chip would take advantage of the permission to not implement the low pass filter. In fact, it would be difficult to build a coupling capacitor large enough to meet the requirements for the ratio between the high and low pass filter time constants. For an on-chip coupling capacitor, do not implement the low-pass filter. Also, pay attention to the voltage sharing that can take place when the input capacitance of the combination of the differential receiver and the test receiver is close to the value of the coupling capacitor. This can decrease the signal amplitude at the receivers.