AC Boundary-Scan

Cisco Systems, Inc
AC Boundary-Scan: Boundary-scan beyond DC

ASIC DFT Group
Sung Chung and Sang Baeg
May 21, 2001
Problem Statement

- AC Coupled net between high speed devices
  Conventional JTAG does not work
  No JTAG infrastructure to test AC coupled net
- Many Optics / SERDES use “AC Coupling”
- Interoperability demands more “AC Coupling” between high speed devices
- Differential line lacks 1149.1 Test Coverage
Current Status

Device 1

STD 1149.1 capable

Device 2 or Connector

STD 1149.1 incapable

STD 1149.1 incapable
AC Boundary-Scan Overview

- AC Pattern *Generation* at scan cell
- AC Pattern *Application & Sample* at RTI
- AC Pattern Capture at scan cell
- Maintains DC boundary-scan compatibility
- DC & AC Operate at different TAP state
AC Boundary-Scan Operation

- Setup EXTEST value: logic 1 or 0
- Execute *AC_EXTEST* command
- *AC pattern is applied @ RTI*
- Internal Sync Pulse *samples* a logic state from incoming AC pattern
- *Capture_DR* captures a sampled value
- *Shift_DR* for test evaluation
Problem Transmission Lines

Diagram showing a simple transmission line with a driver and a receiver. The driver outputs data logic 1 or 0, which is then transmitted over a signal line. The receiver inputs the data logic 1 or 0 after processing it. The diagram also includes a common ground return path.
Fault Model for Spice Simulation

Transmission line option
- $R = 0 \, \Omega$: DC net
- $R = \infty \, \Omega$: AC net

Fault injection option
- $R = 0 \, \Omega$: Shorted net
- $R = \infty \, \Omega$: Opened net
Expanded Fault Model 1
Expanded Fault Model 2

Diagram showing the connection of nodes 1 to 5 with resistance elements and the target receiver connected to Vref.
Test Buffer and Fault Classes

Termination Network

Highspeed signal path

AC Status Detection
Null Detection
Short Detection

Test Buffer
## Fault Detection and Error Status

<table>
<thead>
<tr>
<th>Fault detection criteria</th>
<th>Resulting Error Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Null or Float Status</td>
<td>Short Status</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
<td>1</td>
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<td>1</td>
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<td>1</td>
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<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Why Fault Classes

- Fault Model changes constantly
  .. as Technology changes
  .. as Defects changes
  .. as board topology and usage changes
  There will be never enough Fault Models

- Identify un-defined logic state with Null sensor
  “00” or “11” logic state in differential line
  Don’t let functional logic makes decision for Test, it is made to tolerate such conditions during functional mode

- Null / Short / AC Status need to be identified within functional domain of the device

- Test Buffer must evolve as technology evolves
  New technology invents new faults
Timing Diagrams

- **TCK = AC Pattern Clock**
- **AC Pattern**
- **Run-Test/Idle TAP State**
- **AC_Sync**

**AC Pattern Clock Cycle**

- **1st AC Pattern Cycle**
- **AC Pattern Cycle**
- **16th AC Pattern Cycle**

**Run/Test Idle Duration**

- **AC Pattern Sample Interval = Every 16th AC Pattern Cycle**
- **Next AC Pattern Sample Interval**

**AC Pattern**

- **AC Pattern = 1**
- **AC Pattern = 0**

**AC_Sync**
Output scan cell Example 1

Data from system logic
From last cell
ShiftDR
AC_Pattern_Clock or ClockDR
UpdateDR
AC_Pattern_Source
AC_Test
DC_Mode

To next cell

D Q
Clk
Capture Cell

D Q
Clk
Update Cell

To system pin

BC_1
Output scan cell Example 2

AC_Test_Marker
Data from system logic
From last cell
ShiftDR
AC_Test
AC_Pattern_Clock
or ClockDR
UpdateDR
AC_Test
DC_Mode

To system pin

BC_1
Output scan cell Example 3
Input scan cell Example 1

From system pin
AC_Sync
AC_Test_Ran
From last cell
ShiftDR
ClockDR
UpdateDR
DC_Mode

AC Pattern Hold Cell
D Q
Clk

Capture Cell
D Q
Clk

Update Cell
D Q
Clk

To next cell
Data to system logic

BC_1
Input scan cell Example 2

From system pin

AC_Sync
AC_Test_Ran
From last cell
ShiftDR
ClockDR

To next cell
Data to system logic

BC_4
AC_EXTEST control cell Example

AC_EXTEST Control Cell

Output Cell BC_1

From last cell
ClockDR
UpdateDR

AC_Pattern_Source
AC_Test
Mode

AC_Pattern_Clock or ClockDR
UpdateDR
ShiftDR

Output Data

To next cell

To system pin
Bidi scan cell Example 1

Output Control
ShiftDR
ClockDR
UpdateDR
Mode

Output Data
ShiftDR
ClockDR
UpdateDR
AC_Pattern_Source
AC_Test
Mode

Input Data
AC.Sync
AC_Test_Ran
From last cell
ShiftDR
ClockDR

BC_1
Control Cell

BC_1
Output Cell

BC_4
Input Cell

To next cell
To system pin

Input Control
ShiftDR
ClockDR
UpdateDR
Mode

Input Data
ShiftDR
ClockDR
UpdateDR
AC_Pattern_Source
AC_Test
Mode

Output Data
ShiftDR
ClockDR
UpdateDR
AC_Pattern_Source
AC_Test
Mode

Output Control
ShiftDR
ClockDR
UpdateDR
Mode

BC_1
Control Cell

BC_1
Output Cell

BC_4
Input Cell

To next cell
To system pin
Bidi scan cell  Example 2

Control Cell  BC_2

Bidirectional Cell  BC_7

Output Control
Mode_1
ShiftDR
ClockDR
UpdateDR
Output Data
AC_Sync
AC_Test_Ran
From last cell
ShiftDR
ClockDR
UpdateDR
AC_Pattern_Source
AC_Test
Input Data

Mode_2
To system pin

Mode_3
To next cell
Bidi scan cell Example 3

Control Cell BC_2

Bidirectional Cell BC_8

Output Control

Output Data

Mode

AC_Test_Ran

AC.Sync

From last cell

ShiftDR

ClockDR

UpdateDR

AC_Pattern_Source

AC_Test

Input Data

To system pin

To next cell
### AC_EXTEST: Superset of EXTEST

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Execution effects after Capture-DR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>AC scan cell</td>
</tr>
<tr>
<td></td>
<td>Passing through RTI</td>
</tr>
<tr>
<td>AC_EXTEST</td>
<td>AC_EXTEST</td>
</tr>
<tr>
<td>EXTEST</td>
<td>EXTEST</td>
</tr>
</tbody>
</table>

This table shows effect of each instruction within the device which has both AC and DC boundary-scan cells.
Compatibility mode between devices

## Receiving AC Scan Cell (through DC net)

<table>
<thead>
<tr>
<th>Driving AC Scan Cell</th>
<th>Passing through RTI</th>
<th>Bypassing RTI</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>EXTEST</td>
<td>AC_EXTEST</td>
</tr>
<tr>
<td>EXTEST</td>
<td>Capture DC ¹</td>
<td>Capture DC ²</td>
</tr>
<tr>
<td>AC_EXTEST</td>
<td>Unknown ⁴</td>
<td>Capture AC</td>
</tr>
</tbody>
</table>

**NOTE**

1. Backward compatibility: interoperable with DC scan cell with EXTEST.
2. The AC_EXTEST is a superset of existing DC EXTEST capture operation.
3. Input cell can capture DC under the AC_EXTEST.
4. Input cell captures unknown value.

## Receiving AC Scan Cell (through AC coupled net)

<table>
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<th>Driving AC Scan Cell</th>
<th>Passing through RTI</th>
<th>Bypassing RTI</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>EXTEST</td>
<td>AC_EXTEST</td>
</tr>
<tr>
<td>EXTEST</td>
<td>Unknown ¹,²</td>
<td>Unknown ¹,²</td>
</tr>
<tr>
<td>AC_EXTEST</td>
<td>Unknown ¹</td>
<td>Capture AC</td>
</tr>
</tbody>
</table>

**NOTE**

1. All DC operations will capture unknown value due to AC coupling.
2. Presence of certain fault, sampling line status in DC may serve diagnostic purpose.
Jitter Budget

Max Jitter = (1/4 Tck Cycle) - (Setup or Hold time)

<table>
<thead>
<tr>
<th>TCK Frequency</th>
<th>Maximum Jitter</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 MHz</td>
<td>50 nS</td>
</tr>
<tr>
<td>10 MHz</td>
<td>25 nS</td>
</tr>
<tr>
<td>20 MHz</td>
<td>12.5 nS</td>
</tr>
<tr>
<td>40 MHz</td>
<td>6.25 nS</td>
</tr>
</tbody>
</table>

TCK = AC Pattern Clock

AC Pattern
AC_Sync

Reference Signal

Device 1

Device 2

In phase
Lag 1/4 Cycle
Lead 1/4 Cycle
Scalability: Test Buffer vs. Frequency

Scalable by **Test Pattern Frequency** as technology changes or **Test Buffer Approach** based on technology used in design.
Coupling Capacitor

- Practical issues with smaller coupling capacitor
  - Reactance and Inductance
  - Low loss Dielectric and low Parasitic
  - Impedance Magnitude at high speed
  - I/O characterization test makes on chip capacitors almost impossible
  - Capacitor may end up more easily on package substrate
  - Low capacitance value will increase low frequency Pattern-Dependent Jitter (PDJ) beyond functional tolerance

For a 2.488Gbps receiver, bit period $T_b = 402 \text{ pS}$. If Maximum tolerated consecutive identical digits $N_{cid} = 72$ bits and termination resistor $R = 100 \Omega$, calculated $C$ is 2.25 nF. If rise time $T_r = 120 \text{ pS}$ and $C = 2.25 \text{ nF}$, the calculated PDJ is 12 pS. If we increase $C$ to 100 nF, the resulting PDJ will be reduced to less than 1 pS.

Choosing AC Coupling Capacitors from Maxim  http://pdfserv.maxim-ic.com/arpdf/AppNotes/hfan11v2.pdf

Does capacitor value ever decrease as frequency increases??
BSDL Support

- AC_EXTEST is currently contained within the Extension
  BSDL does not disturb existing tools
  One BSDL serve both DC and AC
- Multiple AC_EXTEST Instruction & Execution support
- Selective AC_EXTEST disable function
- Easy to create:
  Register list identifies AC_EXTEST capable cells
  Duplicate from existing DC register list
- Parser will be ready within a month
Why Cisco MSA Approach??

• **KISS (Keep It Simple and Smart)**
  Simple, minimum overhead, and self-contained
  No extra test pin
  Very little effort from DC boundary-scan design
  Autonomous and transparent to ATE and CAE tools

• **Compatibility**
  Backward compatible and coexist with legacy DC boundary-scan device in DC mode
  Runs either DC, AC, or both during test
  No investment loss: *if it was working, it will be working*

• **High Noise immunity**
  Operate AC and DC in separate TAP state
  No AC interference during DC test: preserve DC test coverage
  Differential input Test Buffer filters tester related CM noise

• **Scalability**
  No need to scale with functional speed and technology change
Brief Development History

- **Initial study completed**  
  May 1st, ‘00: Draft completed

- **AC_EXTEST Specification Release**  
  June 8th, ‘00: Cisco internal release  
  June 8th to June 12th ‘00: Release to all MSA partners

- **Follow on research**  
  Oct ’00: RTL verification completed  
  Nov ’00: selected fault Spice simulation completed  
  Patent filed

- **Demo Board and RTL Verification tool**  
  Demo Board is in PCB routing and signal Integrity  
  Parser is in debug

- **Supporting 2 internal projects**  
  5 or more MSA partners to meet test need for the project within next 18 month