

AC EXTEST with Integrating Receivers

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1 Introduction

This document describes the details of a solution for testing AC-coupled nets between integrated circuits on printed circuit boards or in systems. Traditionally, such interconnect has been DC-coupled and can thus be tested with well-known Boundary-Scan methods, specifically with the EXTEST instruction as codified in IEEE Std 1149.1. However, the use of AC-coupling capacitors disallows DC-based techniques, giving rise to the need for an extension of Boundary-Scan into the AC realm.

There are several possible technical solutions to enable AC Boundary-Scan testing that have been studied by the AC EXTEST Working Group. This proposal comes about by combining several of the ideas that the group has been considering. The result is a radically simplified approach to addressing the AC EXTEST problem.

2 AC Integrating Receivers

A general differential channel with differential Boundary-Scan control and single-ended monitoring is shown in Figure 1. An optional monitor point on the mission receiver is also shown.

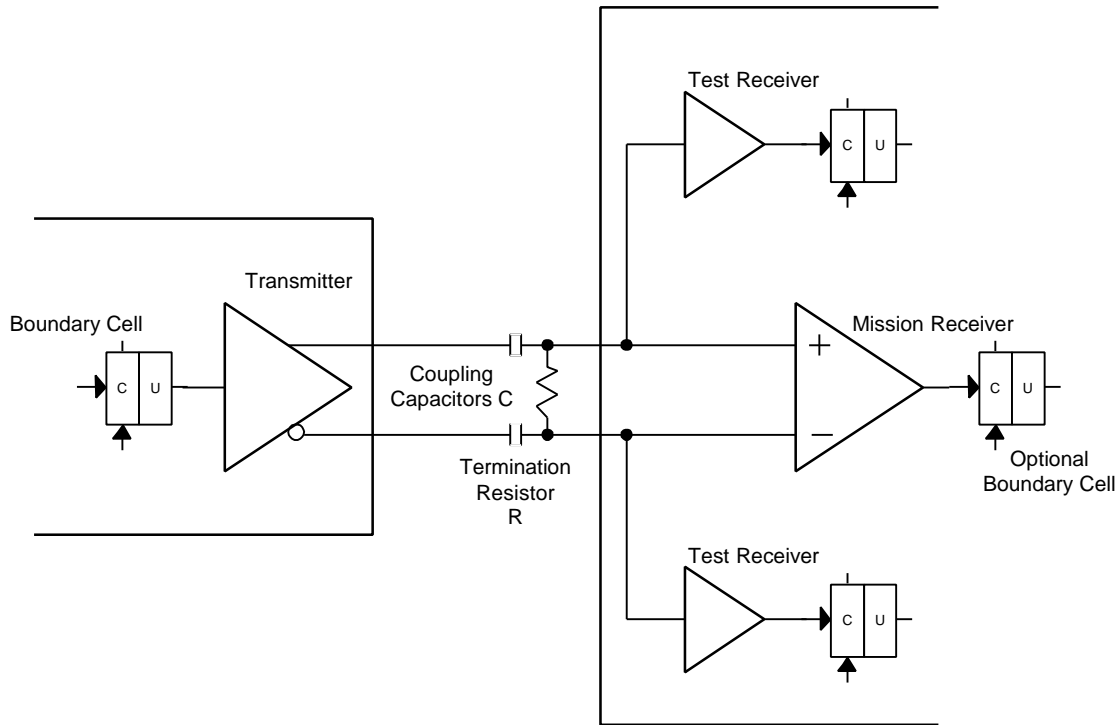


Figure 1: General structure of an AC coupled differential channel with Boundary-Scan testability.

On the drive side, there is *no change* needed to support AC EXTEST, provided that while in test mode, the edge speeds of the transmitted signals are the same as those when in system mode. Indeed, the driver IC could be an existing device implementing today's 1149.1 standard.

On the receive side, the test receivers shown have special properties that are turned on/off by loading AC_EXTEST versus EXTEST.¹ When EXTEST is in effect, the receiver simply digitizes the DC value appearing on the pin as specified by 1149.1. When in AC_EXTEST, the receiver *integrates* the signal that appears on its input. Thus if a level transition is produced by the driver, the RC network of the termination/coupling network turns this into a positive or negative-going spike. The integrating feature of the receiver then converts this back into a replica of the DC levels produced by the driver. One leg of this process is shown in Figure 2. Waveforms seen at the driver, receiver input and receiver output are shown in Figure 3 when AC_EXTEST is in effect. The receiver has its integration capability turned on.

¹ This can be accomplished simply by having two receivers, DC and AC, and multiplexing between them.

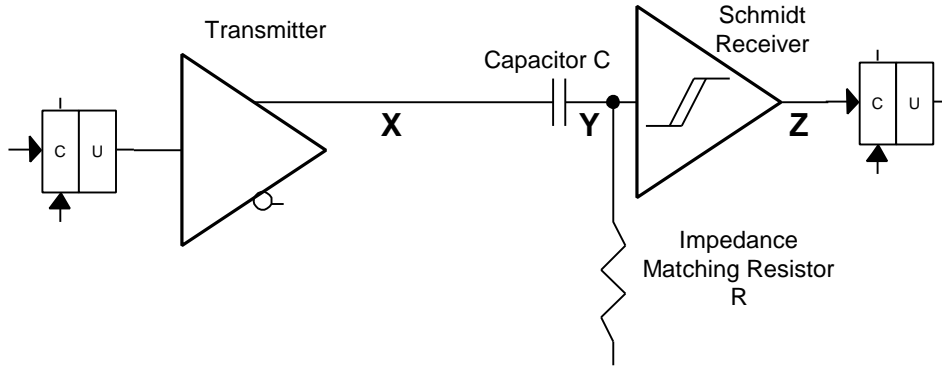


Figure 2: The test path of the positive leg of Figure 1. When AC_EXTEST is in effect, the test receiver integrates the pulse stream.

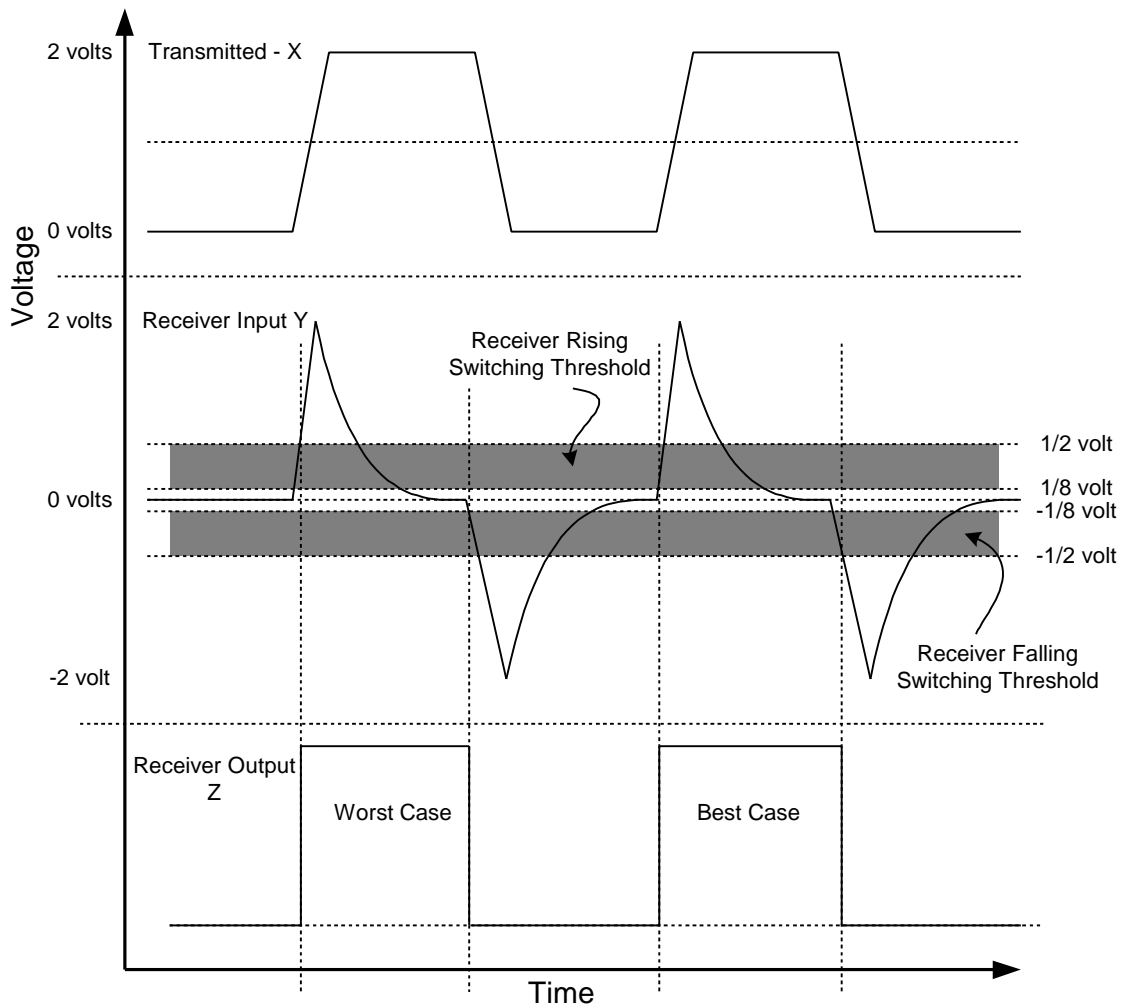


Figure 3: Waveforms seen at point X, Y and Z in Figure 2 when AC_EXTEST is in effect. The thresholds shown are arbitrarily chosen but may need standardization.

Now, during test, the driver IC conducts familiar Boundary-Scan activities with EXTEST. The receiver IC is loaded with AC_EXTEST. As the driver switches states, the integrating feature of the receiver tracks these changes such that the receiver Boundary Register cell sees exactly the same results as if the RC filter were not there. This brings up an important point: if the driver is

DC coupled to the receiver but we load AC_EXTEST in the receiver IC, the result will be the same. Thus there is no need for extra control cells to selectively turn off the AC_EXTEST feature on a pin-by-pin basis.

3 Pro/Con Analysis

There are a number of advantages to this approach.

1. There is no impact on driver design as it is a standard 1149.1 implementation. (No insertion of square waves of any kind.)
2. There is minimal impact on receiver design, no counters or dividers needed. The main concern is the properties of the integrator (see 'cons').
3. There is no need for a new frequency or clock source. The same old TAP design will work.
4. There are no new requirements or restrictions placed on TCK. Any existing tester of any vintage or cost will be able to perform this test.
5. An existing tester that performs edge-connector test will be able to continue doing so when it is receiving from drivers, but may need help when driving the receive side to meet edge rate requirements.
6. There is no need for selectively enabling the AC_EXTEST function by pin. (This was motivated by a desire to have DC hold states on drivers, and since the drivers are unmodified, this is inherent.)
7. Existing test generation algorithms are almost completely unaffected as they only need to know which ICs need the AC_EXTEST instruction loaded rather than just EXTEST.
8. The silicon implementation is very cheap. One estimate from Charles Moore for the integration capability is 28 transistors (about 7 gate equivalents) which includes threshold level control, short-pulse rejection, set, reset, and power down. (This estimate is for one receiver, or one-half a channel.)
9. The BSDL requirements are minimal. We still need to identify the receiver pins that have this capability, but not much else.

There are some disadvantages. These must be carefully considered.

1. Noise pulses injected into the channel can cause the integrator to 'flip' and fail a test. Thus the noise rejection specification for the integrator will need to be carefully thought out. While noise and ground bounce are sometimes a problem for today's Boundary-Scan testing, we don't want AC_EXTEST to be even more sensitive.²
2. We must assure that when switching from normal mode to test mode, the initial state of the integrators is consistent with the levels the drivers will be providing.
3. The specifications of the receivers must not be difficult to verify and test.
4. While in almost every respect the diagnostics are unaffected, one exception is that a "stuck at" 1 or 0 will always appear to be one or the other. Thus the stuck level can't be reported reliably. (True for all AC_EXTEST proposals now.)

² Fortunately, differential technology inherently mitigates one source of ground-bounce, asymmetric drive.