

## IEEE P1149.6:D2.3

# Draft Standard for Boundary-Scan Testing of Advanced Digital Networks

Prepared by the AC EXTEST Working Group  
of the Test Technology Standards Committee  
of the IEEE Computer Society

**Abstract:** This standard augments IEEE Std 1149.1 to improve the ability for testing differential and/or AC coupled interconnections between Integrated Circuits on boards and systems.

**Keywords:** AC Coupled Signals, Boundary-Scan, Differential Signaling, Interconnect Testing

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## Introduction

(This introduction is not part of this standard.)

The development of this standard was begun May 21, 2001 by an ad-hoc industry Working Group called by Agilent Technologies and Cisco Systems. This group formulated this draft standard, with the intention of handing it over to the IEEE for formal standardization when the underlying technology became understood.

The group adopted as its mission:

To define, document and promote a means for designing ICs that support robust Boundary-Scan testing of boards where signal pathways make use of differential signaling and/or AC coupled technologies. This technology utilizes and is compatible with the existing IEEE 1149.1 standard. The goal is to upgrade the capabilities of IEEE Std 1149.1-2001 to maintain the rapid and accurate detection and diagnosis of interconnection defects in boards and systems despite the fault masking effects of differential signaling and the DC blocking effects of AC coupled signaling.

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# 1 Overview

## 2 **1.1 Scope**

3 This document describes the details of a solution for testing differential and/or AC-coupled nets  
4 between integrated circuits on printed circuit boards or in systems. Traditionally, such  
5 interconnect has been DC-coupled and can thus be tested with well-known Boundary-Scan  
6 methods, specifically with the EXTEST instruction as codified in IEEE Std 1149.1-2001.  
7 However, the use of AC-coupling technology disallows DC-based techniques, and differential  
8 signaling can cause fault masking effects, giving rise to the need for an extension of Boundary-  
9 Scan into the AC and differential realms.

## 10 **1.2 Organization of the Standard**

- 11 Clause 1 provides an overview and context for this standard.
- 12 Clause 2 provides references necessary to understand this standard.
- 13 Clause 3 defines terminology used in this standard.
- 14 Clause 4 outlines the technologies addressed and utilized by this standard.
- 15 Clause 5 discusses TAP instructions needed for testing.
- 16 Clause 6 provides rules for I/O pin implementation.
- 17 Clause 7 provides rules for conformance and documentation of devices designed to this standard.
- 18 Clause 8 shows how this standard is used in typical testing applications.

## 19 **1.3 Context**

20 Figure 1 shows a printed circuit board containing many types of devices. Of these, some could be  
21 compliant with IEEE Std 1149.1 for the support of testing activities. These devices contain  
22 Boundary-Scan testability circuitry which allows them to participate in manufacturing tests that  
23 detect and diagnose faults such as open solder joints, shorts and missing devices.

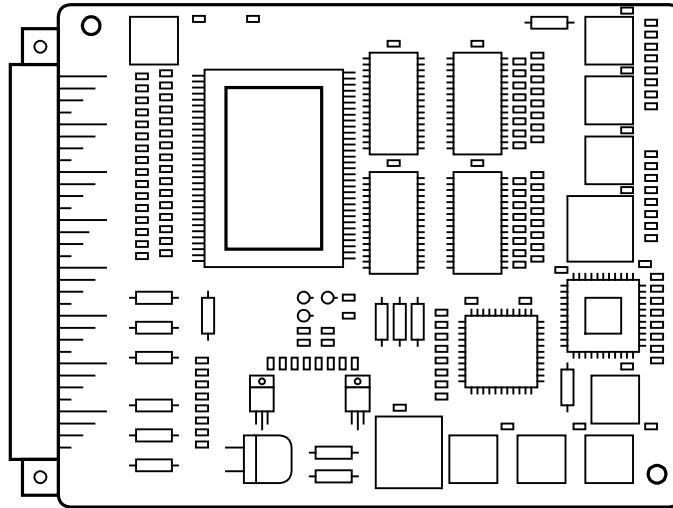
24 The additional testability elements added by this standard to these same ICs allow this  
25 interconnect testing to be conducted on differential signal pathways and/or where AC coupling  
26 (which blocks normal DC test signals) has been used on signal paths between ICs.

## 27 **1.4 Objectives**

28 The objective of this standard is to provide design guidance for testability circuitry added to an IC  
29 in addition to testability provisions specified by IEEE Std 1149.1, such that when such an IC  
30 contains differential signaling and/or is AC coupled with other ICs compliant to this standard,  
31 board and system level tests can be readily and accurately conducted.

32 Devices that adhere to this standard that are used in differential and/or AC coupled signaling  
33 environments will realize significant savings in testing costs for boards and systems. Tools that  
34 are cognizant of the capabilities provided by this standard will be able to prepare, run and  
35 interpret these tests in a highly automated fashion, with high diagnostic resolution.

- 1 This standard allows devices created by multiple vendors to operate together during testing
- 2 despite the differing characteristics and parameters of the IC processes used to fabricate the
- 3 devices.
- 4 This standard also provides design guidance to board and system designers that will enhance the
- 5 performance of the testability features of their products. This in turn will reduce system and
- 6 production costs.



7 **Figure 1: A printed circuit board containing a variety of components interconnected by printed**  
8 **wiring. Some ICs contain IEEE 1149.1 features that support Boundary-Scan interconnect testing.**

## 1 2 References

2 This document shall be used in conjunction with the following standards. When the following  
3 standards are superseded by an approved revision, the revision shall apply.

4 IEEE Std 100-1996, IEEE Standard Dictionary of Electrical and Electronic Terms.

5 IEEE Std 1149.4-1999 IEEE Standard for a Mixed Signal Test Bus.

6 IEEE Std 1149.1-2001, IEEE Standard Test Access Port and Boundary-Scan Architecture.

# 1 3 Definitions and Acronyms

2 In the following definitions, defined terms appear in **bold font**.

## 3 3.1 Definitions

4 Defined terms appear in **bold type**.

5 **AC Coupling:** The use of series capacitance in a **signal path**. This coupling will block  
6 DC voltages on the drive side of the path from appearing on the receive  
7 side. Only the AC component of the driven signal will pass through the  
8 coupling, with the effect of high-pass filtering imposed on the original  
9 signal. *Contrast with DC coupling.*

10 NOTE – AC coupling may also be accomplished with transformers which, as with capacitive coupling  
11 form a **high-pass filtered** transmission structure. While the principles used in this document can be applied  
12 to transformer coupling, this coupling technology is less often used and is thus ignored to simplify  
13 discussion.

14 **AC Pins:** Device signal pins that are the target of the rules of this standard. AC  
15 pins may be **AC coupled** and/or **DC coupled** and may also be  
16 differential. *Contrast with DC Pins.*

17 **Bias:** A high impedance (typically >1000 ohms) voltage source often used on  
18 the input of a receiver to cause it to output a deterministic state in the  
19 absence of an input signal, and/or to select the **common mode voltage**  
20 seen by a **differential receiver** in **AC coupled** signal paths.

21 **Bias network:** A network of impedances, usually higher-valued than **termination**  
22 impedances, used to establish a **common mode** or **reference voltage**.

23 **Channel:** A **signal path** or set of signal paths that transmits a single data stream  
24 from a source to a destination. *See differential signaling and single-*  
25 *ended signaling.*

26 **Characteristic Impedance:** the ratio of the complex voltage and complex current of a signal  
27 traveling forward on a conductive path. A signal path is often  
28 **terminated** with an impedance that matches the characteristic impedance  
29 of the path. This makes the path appear to be infinitely long and prevents  
30 signal degradation due to reflections that occur at unterminated ends of  
31 the path. *See termination.*

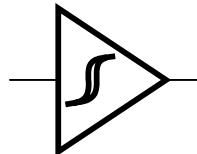
32 **Common mode noise:** A noise signal added equally to both **signal paths** in a differential signal  
33 **channel**. Common mode noise will affect or completely disrupt a **single-**  
34 **ended** measurement of a signal on one leg of a **differential receiver**, yet  
35 this receiver will accurately recover the signal within the noise.

36 **Common mode range:** The range of common mode voltage that a differential receiver is capable  
37 receiving while maintaining reliable signal recovery. A differential signal  
38 with common mode voltage within this range will be received correctly.  
39 Outside this range the receiver may fail to recover the data signal.

40 **Common mode voltage:** The offset from ground of the mean of the maximum and minimum  
41 voltages that appear on a pair of differential signals. A **differential**  
42 **driver** will, by its operational characteristics, define a common mode

- 1 voltage. A **differential receiver** will properly receive data over a range  
2 of common mode voltages, but will likely have an optimal common  
3 mode voltage where its performance is best. When the optimal common  
4 mode voltage of a receiver is significantly different than that of it  
5 associated driver, **AC coupling** can be used to match the two  
6 components of a differential **signal path**.
- 7 **Comparator:** An amplifier with two inputs labeled positive and negative, typically  
8 with very high input impedance. The amplifier usually has very high gain  
9 and produces an output signal that is the amplified difference of the  
10 positive and negative input signals. For all but the smallest differences,  
11 the output will be  $V_{\max}$  or  $V_{\min}$ , which are the most positive and most  
12 negative voltages the amplifier can produce on its output. A comparator  
13 can be used as a differential receiver. A comparator can be used to  
14 determine if an input signal is logically above or below a reference  
15 voltage.
- 16 **Current signaling:** A signal encoded by the amplitude and direction of current flow. In a  
17 differential pair, a current signal is positive when current flows from  
18 positive to negative legs, and negative in the reverse direction. The  
19 voltage that may appear on these same legs does not carry information.  
20 *Contrast with **voltage signaling**.*
- 21 **DC Coupling:** The use of simple wires or small series resistances in a signal path.  
22 *Contrast with **AC coupling**.*
- 23 **DC Pins:** Device signal pins that are equipped solely with test resources defined by  
24 IEEE Std 1149.1. *Contrast with **AC Pins**.*
- 25 **Derived voltage reference:** a voltage reference derived from: 1) other references, such as a  
26 resistive divider between power and ground, or 2) a resistive divider  
27 between two differential signals that recovers the common mode voltage  
28 of the signals.
- 29 **Differential driver:** A driver that accepts a single data stream and drives it onto two  
30 independent signal paths where one signal is the inverse of the other. The  
31 two signals are centered at the common mode voltage.
- 32 **Differential receiver:** A receiver that recovers a single data stream encoded differentially on  
33 two signal paths. It effectively subtracts the signal on its negative leg  
34 from that on its positive leg. This eliminates **common mode noise**  
35 appearing on both legs.
- 36 **Differential signaling:** The use of two independent signal paths in a channel to carry a single  
37 data signal, where one path carries an inverted copy of the signal that  
38 appears on the other path. The original data signal can be reconstructed  
39 by taking the difference of the two signals and there is no reliance on a  
40 reference voltage for determining this signal. This has the property of  
41 eliminating **common mode noise** in the transmitted signal. *Contrast with*  
42 **single-ended signaling**.
- 43 **Encoding protocol:** A stream of data bits may be encoded into a new (typically longer) data  
44 stream that has characteristics favorable for its transmission on a  
45 **channel**. The encoded stream may have added redundancy to support  
46 error correction. The encoded stream may have extra bits added to

- 1 deliberately increase the number of transitions that appear in the stream,  
2 effectively raising its apparent **frequency** and facilitating data  
3 transmission that encodes clocking information into the stream.
- 4 **Frequency:** The maximum number ( $f$ ) of transition pairs that occur on a signal path  
5 expressed in Hertz (cycles per second). With respect to **AC Coupling**, a  
6 frequency is *high* when the period ( $1/f$ ) is small compared to the **time**  
7 **constant** of the coupling. A frequency is *low* when the period is large  
8 compared to the time constant of the coupling. The frequency appearing  
9 on a signal path may vary greatly over time as a function of the data  
10 being transmitted and the data **encoding protocol**.
- 11 **Float:** The input to a receiver that is connected to an undriven signal, or a high  
12 impedance connection to a receiver input, is said to *float*.
- 13 **High pass filter:** An electrical network that passes higher frequencies and attenuates lower  
14 frequencies. DC current is blocked.
- 15 **HP\_Mult:** High-Pass Multiplier, a multiplier used to derive the minimum high-pass  
16 coupling time constant. (See sections 0 and 6.1.3.3.)
- 17 **HPLP\_Ratio:** High-Pass-Low-Pass Ratio, a multiplier used to derive the minimum  
18 ratio of high-pass coupling time constant (**HP\_Mult**) to low-pass filter  
19 time constant (**LP\_Mult**). (See sections 0 and 6.1.3.3.)
- 20 **Hysteresis:** From magnetics: lagging in the values of resulting magnetization in a  
21 magnetic material (such as iron) subjected to a changing magnetizing  
22 force. In this document, hysteresis refers to the memory of an input state  
23 to an amplifier or buffer after that state is removed but before a different  
24 input state is applied. Typically there is a hysteresis threshold that  
25 defines the difference between “no input” and “input.” As applied to  
26 electronics, a digital output circuit such as a comparator where the output  
27 switches to one output state when the input is above one level and  
28 switches to the opposite output state when the input is below a lower  
29 level, and the output does not switch at any intermediate level. Example:  
30 a buffer produces a high output when a voltage above 0.5 volts is  
31 applied, produces a low output when a voltage below 0.3 volts is applied,  
32 and does not change its output for voltages between 0.3 and 0.5 volts.
- 33 Hysteresis symbol in a buffer symbol:



- 34 **Hysteretic:** Adjective form of **hysteresis**, as in “hysteretic amplifier.”
- 35 **Interconnect test:** An IEEE Std 1149.1 Boundary-Scan test designed to detect and diagnose  
36 defects in the interconnection wiring between ICs. This standard extends  
37 the concept to include the testing of channels, where single-ended and  
38 differential signaling, and DC or AC coupling may exist.
- 39 **Load termination:** A **termination** placed at the far end (away from the driver) of a **signal**  
40 **path** used to match the **characteristic impedance** of the path. *Contrast*  
41 *with source termination*.

1	<b>Low pass filter:</b>	An electrical network that passes lower frequencies, including DC levels,
2		and attenuates higher frequencies.
3	<b>LP_Mult:</b>	Low-Pass Multiplier, a multiplier used to derive the minimum low-pass
4		filter time constant. (See sections 0 and 6.1.3.3.)
5	<b>Mission logic:</b>	The circuitry inside an IC that performs its primary design function. <i>See</i>
6		<b>test logic</b> .
7	<b>Mission mode:</b>	A device or pin of a device performing its primary design function.
8		<i>Contrast with</i> <b>test mode</b> .
9	<b>Negative leg:</b>	The signal path of a differential signal pair that has the opposite polarity
10		as the original data signal.
11	<b>Null:</b>	The input state where the two inputs to a differential receiver which are
12		supposed to be different (complementary) are instead receiving the same
13		value.
14	<b>Offset voltage:</b>	A constant DC voltage added to an AC signal.
15	<b>Operational modes:</b>	A device or pin of a device may operate in one of two modes, see
16		<b>mission mode</b> and <b>test mode</b> .
17	<b>Positive leg:</b>	The signal path of a differential signal pair that has the same polarity as
18		the original data signal.
19	<b>Reference voltage:</b>	A low impedance voltage source typically used to define a threshold for
20		comparing signals. The low impedance characteristic means it is resistant
21		to conducting noise signals.
22	<b>Referenced termination:</b>	A termination for a differential channel where the two legs are both
23		terminated to a reference voltage. This reference has a low enough
24		impedance such that the two legs are independent.
25	<b>Self-referenced comparison:</b>	The comparison of a signal with a delayed, averaged version of the
26		same signal, used to detect signal transitions. This process does not need
27		a static reference voltage to find a transition in a signal.
28	<b>Signal Path:</b>	An electrical pathway formed by a simple conductor, or a terminated
29		pathway containing a series resistance, or an AC coupled pathway
30		containing a series capacitance, that transmits a signal from a driver to a
31		receiver.
32	<b>Signal reflection:</b>	A signal wavefront traveling across a discontinuity in the <b>characteristic</b>
33		<b>impedance</b> of the <b>signal path</b> may have a fraction of its energy reflected
34		in the opposite direction on the path. The reflection may be of the same
35		or opposite polarity and will add into the waveforms appearing on the
36		path, impacting their shape. <i>See also</i> <b>transmission line</b> .
37	<b>Single-ended signaling:</b>	The use of a single signal path in a channel to carry a data signal. The
38		signal is referenced to a static reference voltage. <i>Contrast with</i>
39		<b>differential signaling</b> .
40	<b>Slew rate:</b>	Rate of change in either direction of voltage in a specified time,
41		measured in units of volts per second.
42	<b>Source termination:</b>	A <b>termination</b> placed near the source driver of a signal, to satisfy DC
43		current requirements of a driver and/or to match the <b>characteristic</b>

1 **impedance** of a **transmission line** structure to reduce **signal reflections**.  
2 *Contrast with load termination.*

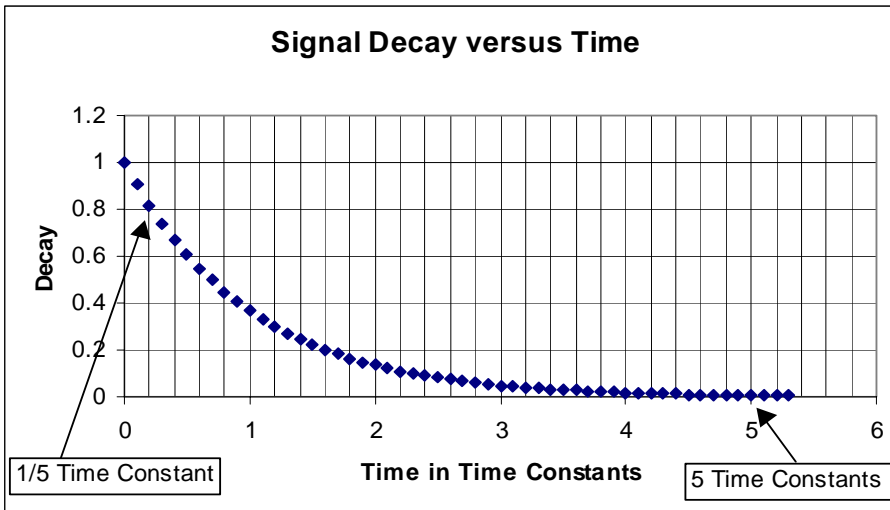
3 **Termination:** An impedance usually near the end of a signal path used to satisfy the  
4 electrical matching requirements of the **characteristic impedance** of the  
5 **signal path** and reduce **signal reflections**. The impedance is typically  
6 low, often 100 ohms or less. *See also characteristic impedance,*  
7 **referenced termination, source termination, load termination and**  
8 **unreferenced termination.**

9 **Test logic:** Testability logic defined by this standard and IEEE Std 1149.1. *Contrast*  
10 *with mission logic.*

11 **Test mode:** A device or pin of a device that, in response to the EXTEST or  
12 AC\_EXTEST instruction, is now driving and/or receiving test data as  
13 controlled by the test logic of the IC. It has been disconnected from the  
14 internal mission logic of the IC. *Contrast with mission mode.*

15 **Time constant:** Typically the product of resistance and capacitance of an RC network  
16 (e.g., a high pass filter) measured in seconds. One time constant is the  
17 time for a capacitor to discharge 63% of its voltage through a resistor. In  
18 AC coupled systems, the termination resistance combined with the  
19 coupling capacitor forms a **high pass filter**.

20 NOTE – In discussions comparing time periods to time constants, a period is *significantly* longer (shorter)  
21 than a time constant if it is five (one-fifth) times the time constant value. For example as shown in Figure 2  
22 using the five-time-constant rule, a signal will decay to 0.7% of its original value. The one-fifth-time-  
23 constant rule means that 81.9% of a signal still remains.



24 **Figure 2: Signal decay versus time in units of time constants.**

25 **Transition:** A voltage transition occurs when a signal traverses a specified voltage  
26 range in a specified time in either direction. *See slew rate.*

27 **Transmission line:** A **signal path** with a specific construction that produces a uniform,  
28 known **characteristic impedance** along its length. This minimizes  
29 degradation of a signal passing along this path that can result from  
30 impedance variations.

- 1 **Unreferenced termination:** A termination for a differential channel where a termination  
2 impedance is connected between the two legs with no connection to a  
3 reference voltage.
- 4 **Voltage signaling:** Signals are encoded by the voltage appearing on a wire compared to a  
5 reference voltage (single-ended) or the voltage appearing on a pair of  
6 wires (differential). *Contrast with **current signaling**.*

### 7 **3.2 Acronyms**

- 8 **CML:** Current mode logic
- 9 **HP\_Mult** High-Pass Multiplier
- 10 **HPLP\_Ratio** High-Pass-Low\_Pass Ratio
- 11 **HSTL:** High-Speed Transceiver Logic
- 12 **LP\_Mult:** Low-Pass Multiplier
- 13 **LVDS:** Low Voltage Differential Signaling
- 14 **LVPECL:** Low voltage PECL (Pseudo Emitter Coupled Logic)
- 15 **PECL:** Pseudo Emitter Coupled Logic
- 16 **TAP:** Test Access Port (from IEEE Std 1149.1).

# 1 4 Technology

2 The presence of coupling capacitors on chip interconnects, whether they are discreet devices  
3 mounted on a PC board or integrated inside an IC, prevents DC values from being driven between  
4 chips. An AC Boundary-Scan methodology must therefore use a time-varying signal to pass  
5 through the AC coupling when in AC EXTEST mode.

6 Differential signaling is often used to increase signaling speeds and noise immunity, compared to  
7 single-ended coupling. Differential signaling, combined with termination schemes, can have  
8 significant defect masking properties that reduce test effectiveness.

## 9 4.1 Signal Pin Types

10 It is expected that a chip possessing pins requiring AC coupling may also possess “normal” (i.e.,  
11 DC coupled) pins as well. These DC pins would supply data and/or control to/from portions of  
12 the chip that do not require AC coupling. For test purposes, it is necessary that all these pins be  
13 tested simultaneously with an EXTEST-like capability because that is how shorts (unwanted  
14 connectivity) between these pins are reliably detected. This document will refer to DC and AC  
15 pins henceforth. DC pins are those that IEEE Std 1149.1 currently governs for testing. AC pins  
16 have been treated by 1149.1 as an “analog” problem and effectively ignored.

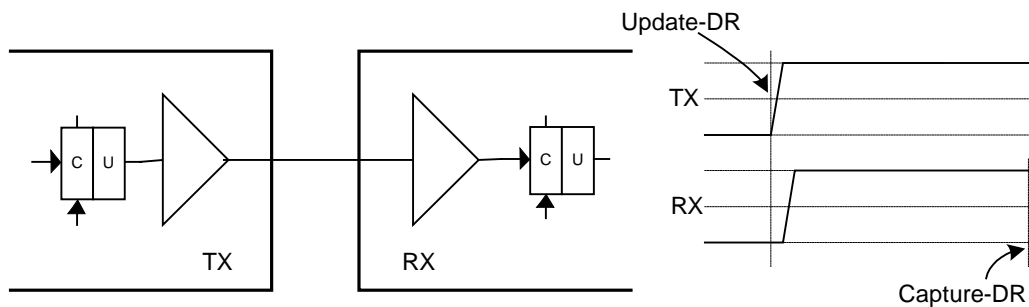
17 AC pins are a principle target of this standard. IC designers implementing this standard are  
18 expected to identify such pins and add new test capabilities for them.

## 19 4.2 Signal Coupling and Coupling Combinations

20 This section reviews a range of coupling options.

### 21 4.2.1 Single-ended DC

22 A basic, single-ended connection scheme is shown in Figure 3, along with the Boundary-Scan  
23 control and observation capability specified by IEEE Std 1149.1. This type of coupling has been  
24 quite common and is very testable using Boundary-Scan.



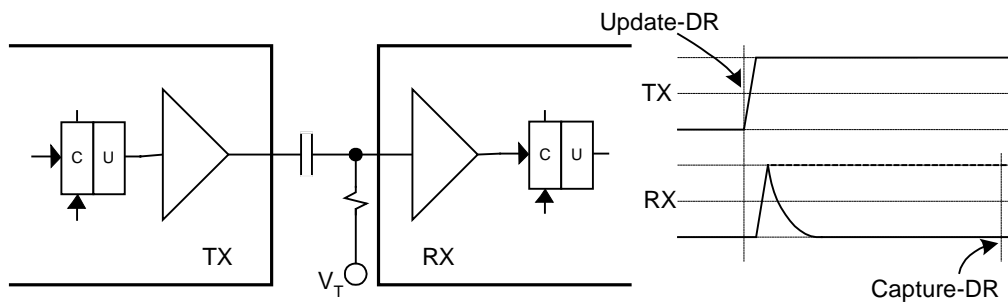
25 **Figure 3: Basic single-ended signaling with Boundary-Scan control and observation.**

26 It is important to note that in a standard Boundary-Scan test, the time between launching a signal  
27 from a driver (at the falling edge of TCK in the Update-DR or Update-IR TAP controller state)  
28 and capturing that signal (at the rising edge of TCK in the Capture-DR TAP controller state) is no  
29 less than 2.5 TCK cycles. Further, the time between successive launches on a driver is governed  
30 not only by the TCK rate, but by the amount of serial data shifting needed to load the next pattern  
31 data in the accumulated Boundary Registers of the Boundary-Scan chain. Thus the effective data  
32 rate of a driver could be thousands of times lower than the TCK rate. For DC coupled

1 interconnect this time is of no concern. For AC coupled interconnect, the signal may easily decay  
2 partially or completely before it can be captured. If only partial decay occurs before capture, that  
3 decay will very likely be completed before the next edge is produced by the driver.

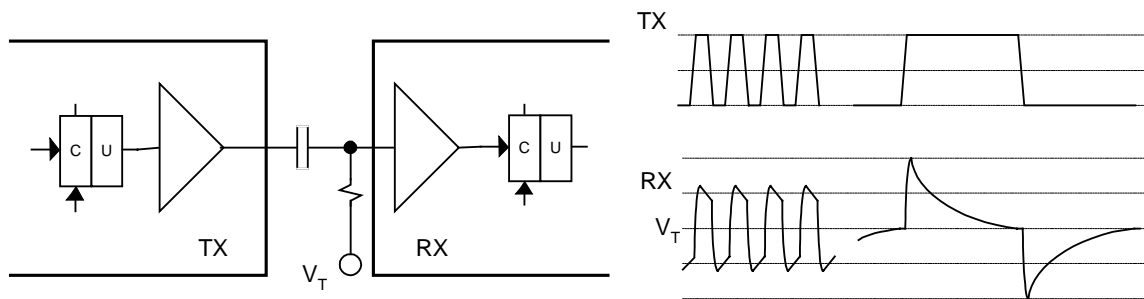
#### 4 4.2.2 Single-ended AC

5 Figure 4 shows an AC coupled single-ended connection. (The termination resistor and voltage  
6 source shown may not be necessary thus would be omitted.) While the devices may have been  
7 designed for DC coupling and actually contain Boundary-Scan resources, the AC coupling will  
8 block their operation. This interconnection configuration is thus untestable with standard  
9 Boundary-Scan algorithms. This is due to Boundary-Scan test data rates being relatively low  
10 since they are a function of the test clock (TCK) rate which may be significantly lower than the  
11 normal operating frequency of the channel being tested. The data seen by the receiver may decay  
12 before it can be captured.



13 **Figure 4: Basic single-ended signaling with AC coupling.**

14 In general, AC coupling can distort a signal transmitted across a channel depending on its  
15 frequency. For example, Figure 5 shows a channel transmitting a high and low frequency  
16 waveform. The high frequency signal is relatively unaffected by the coupling. The low frequency  
17 signal is severely impacted. First, it decays to  $V_T$  after a few time constants. Second, its amplitude  
18 is double the input amplitude. A key item to note is that the transitions in the original signal are  
19 preserved, although their start and end points are offset compared to where they were in the high  
20 frequency case.

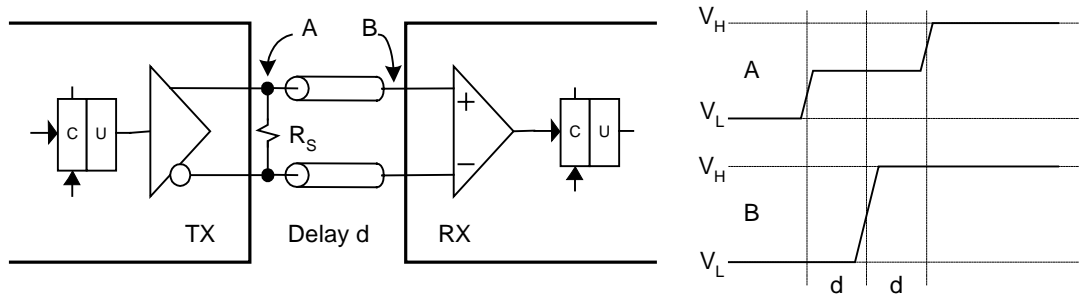


21 **Figure 5: High and low frequency response of an AC coupled channel.**

#### 22 4.2.3 Differential DC

23 Figure 6 shows a basic differential DC coupled signal path. The termination resistor may exist for  
24 impedance matching and/or source termination of the driver. The placement of Boundary-Scan  
25 resources is optional per IEEE Std 1149.1 in that they can be omitted altogether. The 1149.1  
26 standard allows a designer to designate the differential signal path as “analog”. Then the digital-  
27 to-analog and analog-to-digital interfaces (optionally) can be provided with Boundary-Scan

1 resources as shown in Figure 6. When this option is taken, it is then possible to test the “analog”  
2 signal path with Boundary-Scan algorithms. In this case the signal path is viewed by the test  
3 logic as if it were single-ended, leading to diagnostic ambiguity.

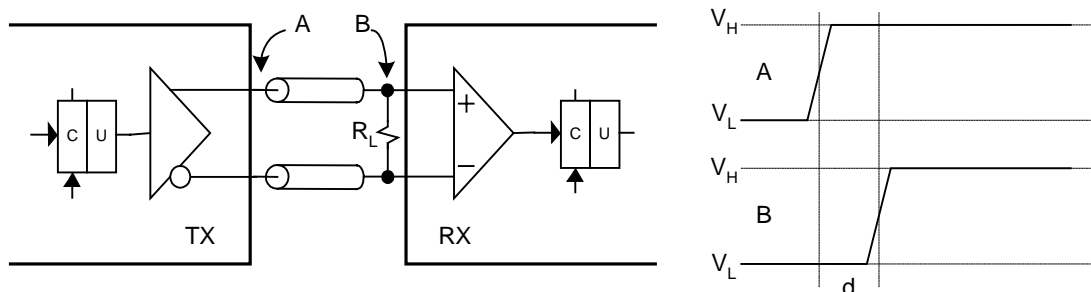


4 **Figure 6: Basic differential signaling with DC coupling and source loading.**

5 The driver in Figure 6 could be producing a voltage signal and the resistor is used to match the  
6 signal line impedance. Alternatively, the driver could be producing a current signal, where the  
7 direction of flow represents data, and the resistor is needed not only to match signal line  
8 impedance, but also to provide a DC current path to satisfy the driver’s requirements. This is  
9 called a source termination.

10 The driver in Figure 6 is looking into a termination  $R_S$  and transmission lines with characteristic  
11 impedance  $R_S$  as well. This forms a voltage divider which sends  $\frac{1}{2}$  the signal into the  
12 transmission lines. When the signal wavefront reaches the receiver (after delay  $d$ ) its high  
13 impedance does not match the characteristic impedance which reflects the signal back down the  
14 lines to the receiver. This signal ( $\frac{1}{2}$  the driver voltage) adds to the signal received so that the  
15 receiver perceives a full voltage swing. After the second transmission line delay  $d$ , the reflected  
16 signal reaches the driver and brings the voltage seen there to the full level. Thus a clean transition  
17 is seen at the receiver, but the signal seen at the driver is a two-step staircase. Since there is an  
18 impedance match at the driver, no new reflections occur.

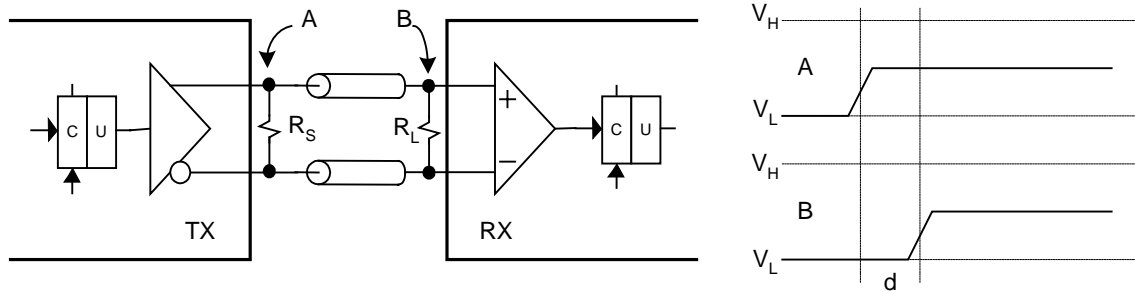
19 In the case where the impedance  $R_S$  is moved to the receiver, (to the right of the transmission  
20 lines) this is called load termination (and the resistor is renamed  $R_L$ ) as shown in Figure 7. Now  
21 the driver is looking into the transmission lines with characteristic impedance  $R_L$ . The full  
22 waveform is transmitted (no divider is now present) and this edge propagates to the receiver. At  
23 the receiver the termination resistor matches the line impedance, and thus there is no reflection.  
24 The waveforms at both the driver and receiver are full transitions.



25 **Figure 7: DC coupled driver and receiver with load termination.**

26 Figure 8 shows a driver/receiver pair that has been both source and load terminated. In this case  
27 the voltage swing seen on both sides of the transmission line has been divided by two (note  $R_S$

1 equals  $R_L$ ). This type of termination assures that in the case of an imperfect impedance match, the  
2 resulting reflections can be attenuated at both ends of the line.



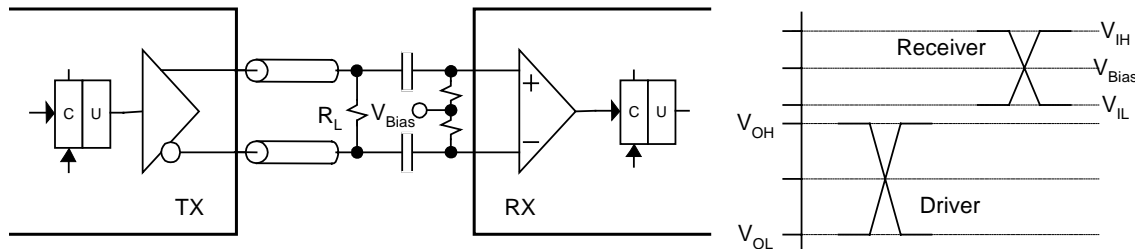
3 **Figure 8: DC coupled driver and receiver with both source and load termination.**

4 **4.2.4 Differential AC**

5 Figure 9 shows AC coupling of a voltage driver and receiver that could be completely  
6 incompatible for DC coupling because the voltage levels used by the driver are too far removed  
7 from the acceptable common mode range of the receiver. The termination network referenced to  
8 the common mode voltage source  $V_{Bias}$ , along with the DC blocking effect of the coupling  
9 capacitors, allows this configuration to work properly. This enforced compatibility is a common  
10 reason why board designers may use AC coupling.

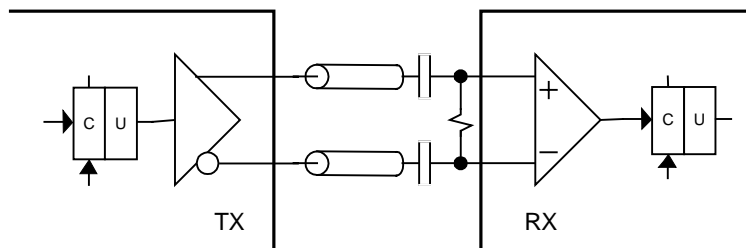
11 NOTE 1 – The receiver waveforms in Figure 9 will decay to  $V_{Bias}$  if the driver frequency is low compared  
12 to the time constant of the coupling network. Since Boundary-Scan test data application rates can be low,  
13 the receiver may indeed see null levels due to signal decay.

14 NOTE 2 – It is assumed in Figure 9 that the distance between  $R_L$  and the receiver inputs is small, such that  
15 there are no significant transmission line effects beyond  $R_L$ .



16 **Figure 9: A basic differential AC signal path with load termination and common mode generation.**

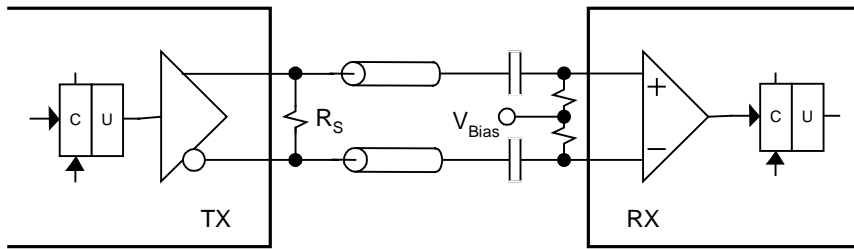
17 Figure 10 shows a basic differential AC signal path with an unreferenced termination. The  
18 termination is used for impedance matching. The driver is a voltage driver and thus does not need  
19 a source termination to provide a current path.



20 **Figure 10: A basic differential AC signal path with unreferenced termination.**

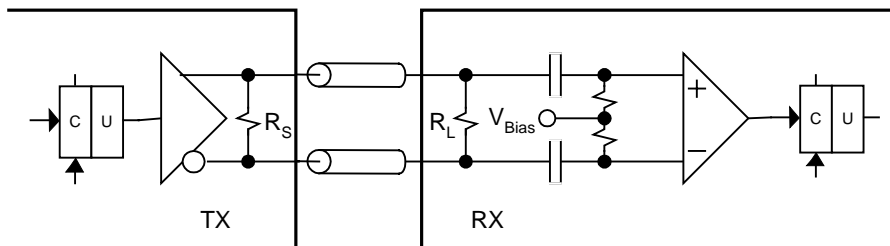
21 Figure 11 shows a basic differential AC signal path with a current driver and source termination,  
22 and also a referenced bias generator to select the common mode voltage appropriate for the

1 receiver. The source termination may also serve as an impedance match for the line. The bias  
2 network may use significantly larger resistors as long as the line distance from the capacitors to  
3 the receiver is small. This will significantly increase the time constant of the coupling network.



4 **Figure 11: Basic differential AC signal path with source termination and bias provision.**

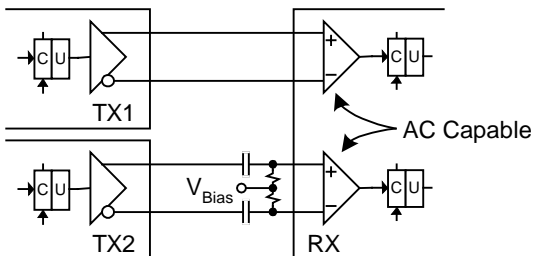
5 Finally, all the terminations, bias networks and even the coupling capacitors may ultimately be  
6 integrated into the receiver IC. Externally, the signal path appears to be DC coupled but internally  
7 it is still AC coupled, as shown in Figure 12. On-chip component defects will not need to be  
8 tested during board test. Thus only the interconnect defects (typically solder) will be relevant.



9 **Figure 12: AC coupling, termination and bias generation internal to the ICs.**

#### 10 4.2.5 Intention: When AC Capability Is DC Coupled

11 The standard for AC EXTEST proposed herein is intended to be implemented on AC pins of an  
12 IC. However, there is the possibility that a board designer may still choose to use DC coupling  
13 between devices that are DC compatible. Thus a test developer could find a situation where AC  
14 EXTEST is needed to test a DC coupled signal path. This could occur when more than one AC-  
15 capable interface exists on an IC and one is AC coupled while another is DC coupled. The test  
16 developer would need to load the AC EXTEST instruction into the device to test the AC coupled  
17 interface. It is the intention of this standard that if DC coupling of AC-capable interface is  
18 possible and gives acceptable mission performance, then the AC EXTEST test performance will  
19 also be acceptable.



20 **Figure 13: An AC-capable receiver connected to an AC-capable driver and a conventional driver.**

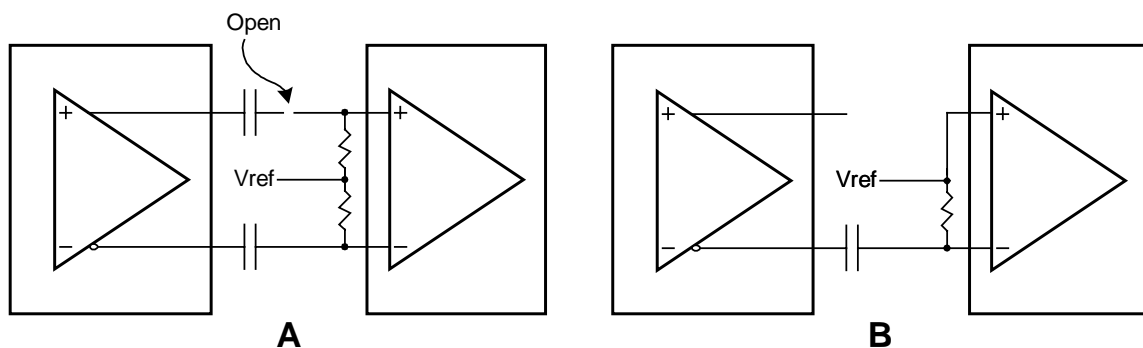
21 For example, in Figure 13 a conventional IC (TX1, containing only EXTEST support) is DC  
22 coupled to a receiver in RX. An AC-capable driver TX2 is also connected to the receiving IC. To  
23 test all the signal paths simultaneously, the conventional device TX1 must be in EXTEST while

1 the other two use the AC EXTEST instruction. See a summary of capture behaviors for various  
2 coupling and testing scenarios given in section 4.9.

### 3 **4.3 The Effects of Defects**

4 Defects are abnormalities in the structure of a board that occur during manufacturing that must be  
5 found and corrected. This “manufacturing defect” model includes things like open solder joints,  
6 shorts, missing components and dead devices. Not included in this model are performance-related  
7 issues, for example, the failure of a device to operate at its highest specified frequency at -40  
8 degrees. This recognizes the traditional role of IEEE 1149.1 as a test standard for manufacturing  
9 defects.

10 The advent of AC coupling, especially in the differential signaling domain, threatens this role.  
11 There is inherent redundancy in differential structures that can mask the presence of seemingly  
12 obvious defects. An example is shown in Figure 14.

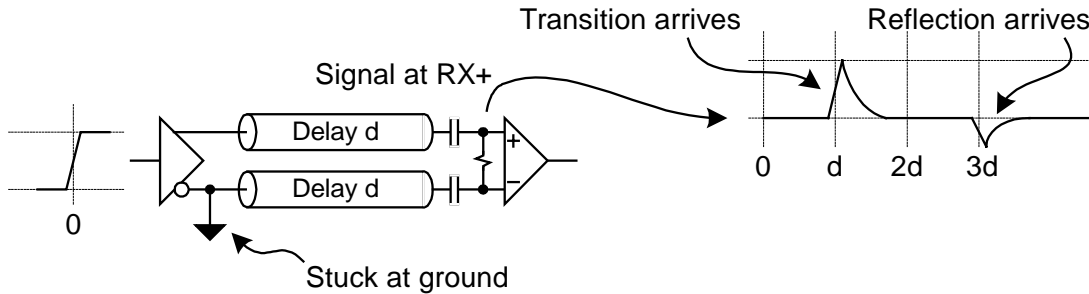


13 **Figure 14: An AC coupled differential path containing a defect (A) and an equivalent circuit (B).**

14 In this case, the positive leg of the circuit is eliminated by a defect, for example, an open solder  
15 joint on the capacitor. Yet the receiver still receives the negative leg signal and compares it to the  
16  $V_{ref}$  voltage. The receiver will still produce the correct output, although its common mode noise  
17 rejection capability is completely compromised. This might not be noticed until subsequent  
18 functional or performance testing is encountered. There it may show up as an elevated bit error  
19 rate which would not provide very much diagnostic information. This simple example illustrates  
20 why it is important to monitor *both* legs of a differential pair, as covered in section 4.5.4.

21 One defect in particular may be troublesome to detect in AC coupled structures: the shorted  
22 capacitor. This defect restores DC coupling. This defect may go unnoticed particularly in  
23 differential signal paths, especially when the DC characteristics of the driver and receiver are  
24 similar. For this reason, it is important to support the standard EXTEST instruction, because it  
25 can be used to test for shorted capacitor defects. This can be done by supplying a stream of 0s and  
26 1s to the driver side of the capacitor and showing that this stream does not show up on the receive  
27 side.

28 Finally, it is important to realize that defects that occur in high-speed circuits (where slew rates  
29 are often faster than signal path transmission times) there may be transmission lines that affect the  
30 circuit's faulty behavior as shown in Figure 15. Simulation of the circuit's behavior may be  
31 necessary to understand the effects of defects. It is important to consider transmission lines as  
32 components of the simulated model when slew rates are elevated.



1 **Figure 15: A defect may interact with transmission lines to produce unexpected effects.**

## 2 **4.4 Differential Termination and Testability**

3 Extensive study of differential channels and the effects of defects within those channels has  
4 shown that the effects of defects are heavily influenced by the termination schemes used. There  
5 are three functions of terminations:

- 6     ▪ to provide for proper DC paths needed for proper driver functioning, (usually source  
7        termination),
- 8     ▪ to provide impedance matching of transmission lines, and
- 9     ▪ in some AC coupled cases, to set common mode operating points for the receiver.

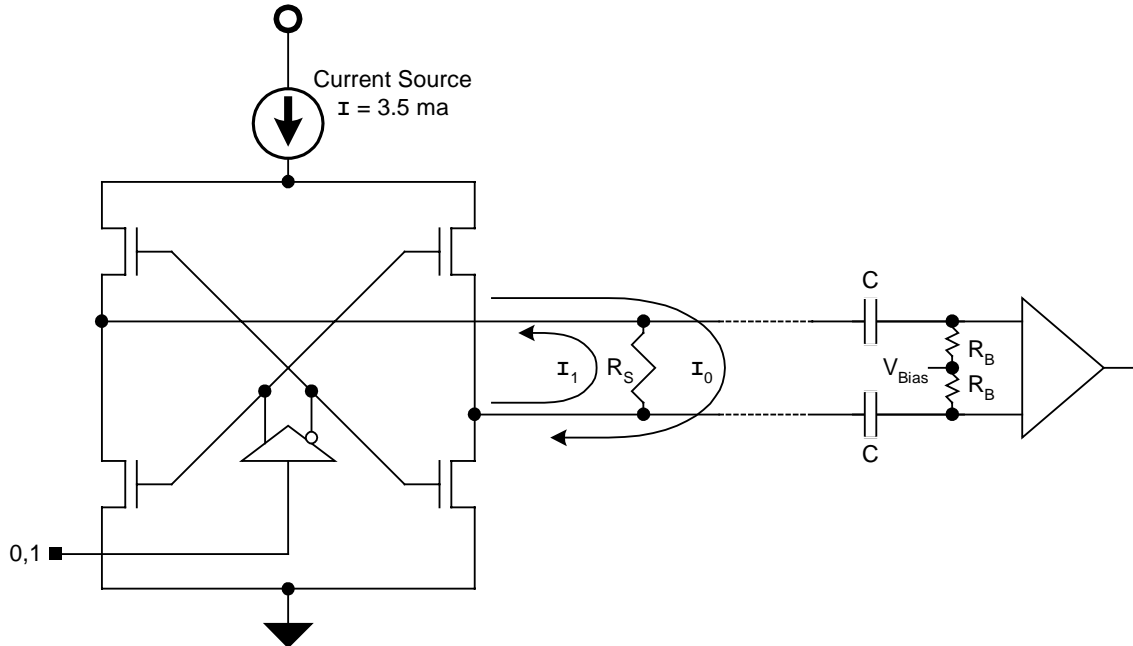
10 A given termination may provide one or more of these functions. The following subsections  
11 discuss termination options.

### 12 **4.4.1 Unreferenced Termination**

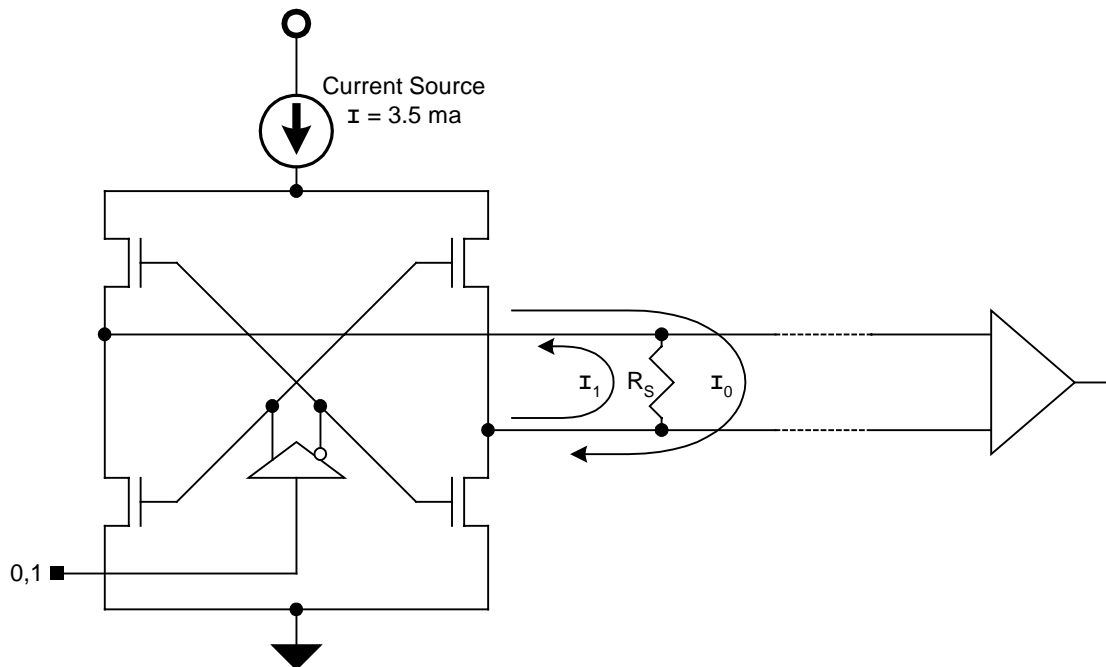
13 Source termination is usually needed for current signaling technologies, where the direction of  
14 current flow is used to encode binary data. A typical example is a Low Voltage Differential  
15 Signaling (LVDS) driver/receiver pair. Since all differential receivers operate by comparing  
16 voltages, a current signal is translated into a voltage signal for that comparison. Figure 16 shows  
17 an LVDS driver DC coupled to a voltage receiver, where  $R_S$  provides both source termination and  
18 impedance matching. The direction of current flow represents data.

19 NOTE – It is assumed that  $R_S$  is placed very close to the receiver so that any transmission line effects are  
20 only present between the driver and the resistor.

21 This form of termination is called unreferenced because there is a single resistor  $R_S$  rather than  
22 two resistors center tapped to a reference voltage (seen later in

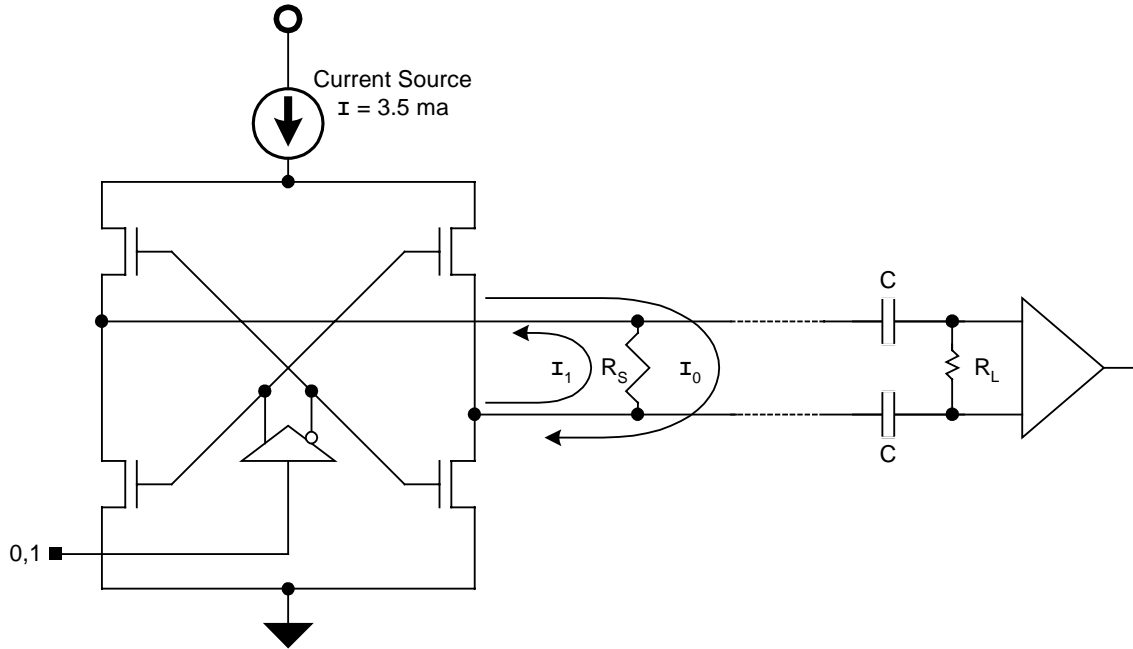


1  
2 Figure 18). In effect, the receiver is referenced to the common mode voltage of the driver/resistor  
3 combination. This means the receiver's common mode range must be compatible with the



4 driver's output.  
5 **Figure 16: LVDS driver and receiver, DC coupled.**

6 Figure 17 shows an unreferenced AC termination. Resistor  $R_S$  still provides source and line  
7 termination. Resistor  $R_L$  provides termination and a current path on the receive side, since the  
8 comparator input impedance is effectively infinity. Note  $R_L$  and  $C$  determine the time constant of  
9 this coupling.

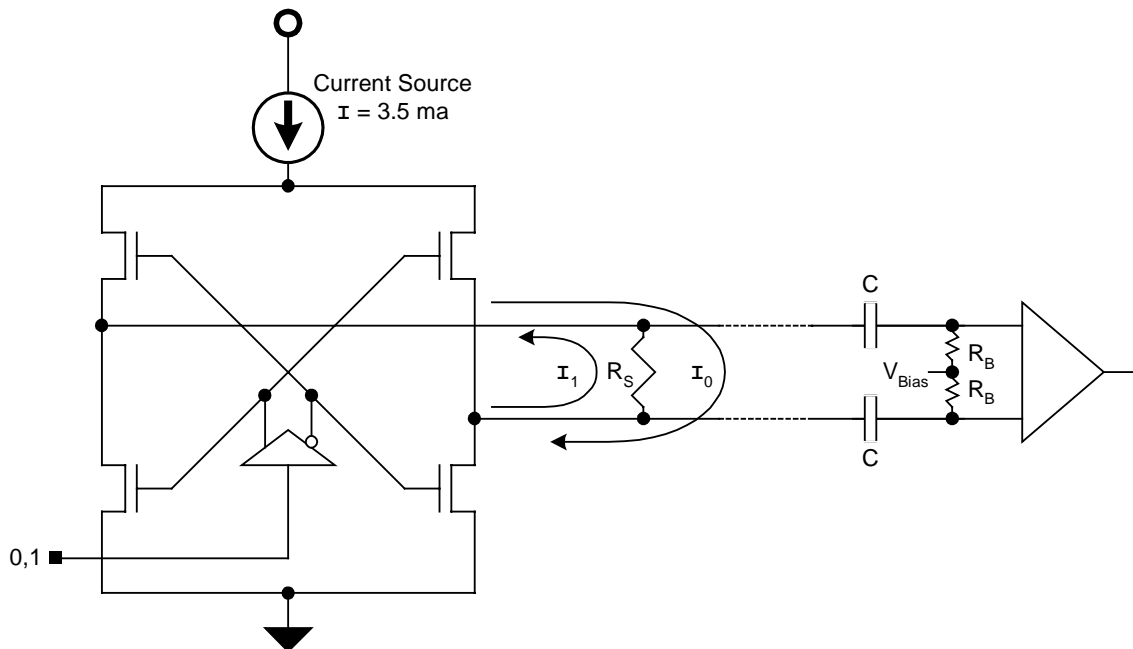


1 **Figure 17: LVDS driver and receiver, AC coupled with unreferenceed termination on the receive side.**

2 NOTE – The receiver in Figure 17 will have its own biasing circuitry built in to establish its common mode  
3 operating point.

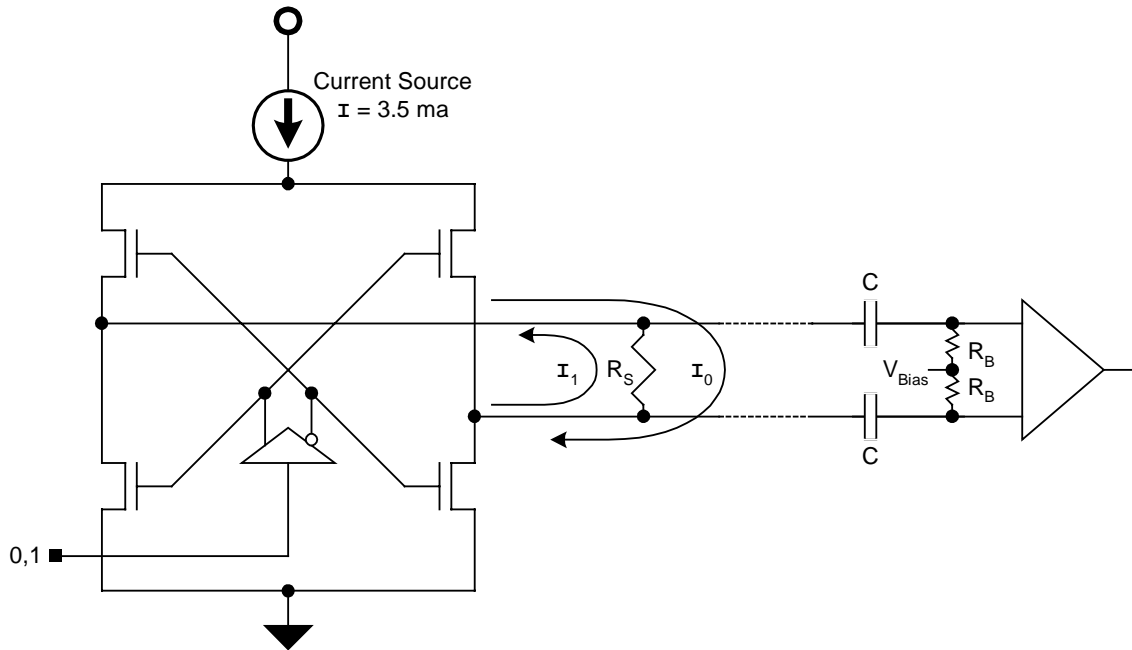
4 If the time between signal transitions is long, the voltage across  $R_T$  will decay to zero volts, or a  
5 null input condition with results that may be undefined. Note that some defects can also cause this  
6 to occur, such as either capacitor C missing. A null input condition during testing is undesirable  
7 due to its non-determinism and the ways it can interact with defects (see 4.3). Because of this,  
8 unreferenceed termination is not preferred even though it saves one resistor.

9 **4.4.2 Referenced Termination**



10 Figure 18 shows an AC coupled, referenced termination. This type of termination is used to set  
11

1 the common mode voltage of the receiver at its optimal value (here,  $V_T$ ). Resistors  $R_B$  along with  
2 capacitance  $C$  determine the time constant of the coupling. The value of  $R_B$  may be larger, simply  
3 providing bias and a larger time constant, or may be smaller to provide both bias, load impedance  
4 matching and a smaller time constant.



5  
6 **Figure 18: LVDS driver and receiver, AC coupled with referenced termination on the receive side.**

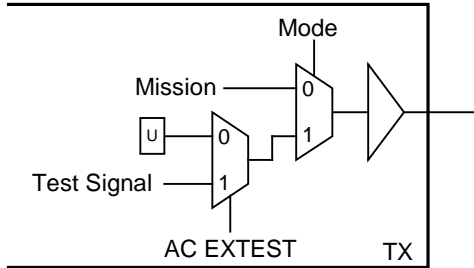
7 In the referenced termination case, if a defect such as a missing capacitor is present (this defect is  
8 shown in Figure 14) the leg with the missing capacitor will see  $V_{Bias}$  while the other leg will see a  
9 valid signal. (The unreferenced case presented both legs with a null condition.) Since test  
10 structures are to be added to both legs (see 4.5.4) they will respond in a deterministic way. This is  
11 the preferred behavior of an AC coupled link.

## 12 **4.5 Test Signal Implementation**

13 In order to test the various combinations of single-ended and differential signal paths with  
14 variations on coupling, modifications have to be made to the drive and receive sides of the path.

### 15 **4.5.1 Single-ended Drive**

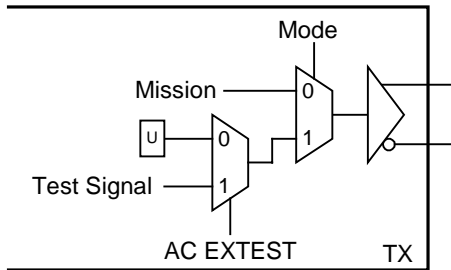
16 Figure 19 shows a single-ended output stage modified in the familiar way given by IEEE Std  
17 1149.1 for test purposes. One of two signals, the normal mission signal or test data are selected  
18 for transmission by a mode signal. (This figure does not show the full detail of the Boundary-  
19 Scan register cells that supply test data.) The test data is either the content of the Update Latch  
20 (U) when executing the (DC) EXTEST instruction, or a “Test Signal” when the AC EXTEST  
21 instruction is loaded into the device. The test signal is an AC waveform suited for transmission  
22 through AC coupling. The concept here is that the single-ended driver itself is not modified.



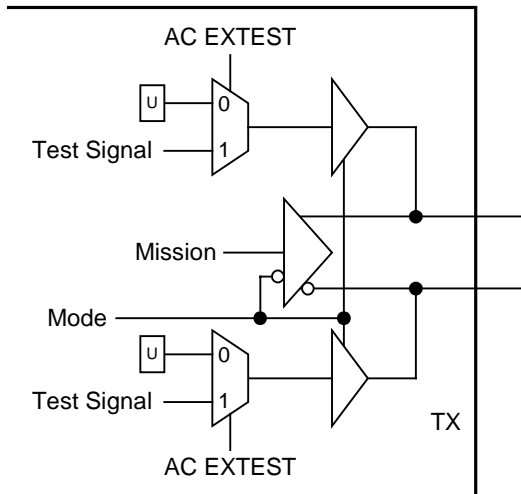
1 **Figure 19: A single-ended driver path.**

2 **4.5.2 Differential Drive**

3 There are two options for implementing a differential driver when incorporating test. The first is  
4 shown in Figure 20 where the selection between test and mission data is performed before the  
5 conversion to differential signaling. This means there will be only one data stream presented to  
6 the two differential pins and that the data will be transmitted in true differential form, using either  
7 current or voltage modes of the driver in question. Due to aggressive performance requirements  
8 in some higher-speed driver designs, it is expected that this option will often be chosen.



9 **Figure 20: Full differential driver for both mission and test modes.**



10 **Figure 21: Differential mission/Single-ended test mode driver.**

11 A second option for implementing testability in a differential driver is shown in Figure 21. In this  
12 case the mission mode signal path is differential, while in test mode the mission driver is disabled  
13 and two single-ended drivers with independent test data sources are enabled. Each controls a  
14 single side of the differential signal path. During test, the path is now a pair of independent  
15 single-ended signals. The two new single-ended test drivers must have similar drive

1 characteristics as the mission driver to assure they are compatible with the loading and coupling  
2 that the mission driver would encounter.

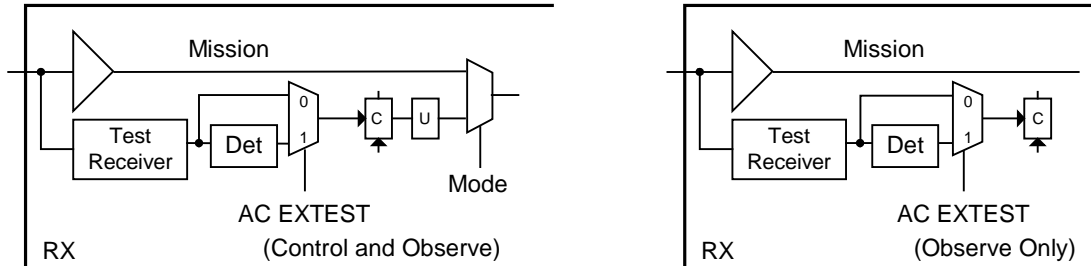
3 NOTE 1 – In describing this case in BSDL (see section 7.2) the *test mode* of the driver signals are  
4 described which are single ended. Thus the signal pair is *not* described as differential. (See the “Grouped  
5 Port Identification” section B.8.8 in IEEE Std 1149.1-2001.)

6 NOTE 2 – If such a device supports IEEE Std 1149.4, then the structure in Figure 21 may be implemented,  
7 but with drivers of insufficient drive capacity to drive the load impedance. In this case, a hybrid of Figure  
8 20 and Figure 21 may be implemented where AC EXTEST operates using the model in Figure 20.

9 This option has desirable testability and diagnosability features in that it removes some of the  
10 redundancy inherent in differential signaling, but it also reduces some of the noise immunity that  
11 differential signaling affords and may generate more noise during testing since the test signals on  
12 the two legs are no longer balanced and offsetting. There is additional cost in that the drive  
13 specifications (slew rate and amplitude) for the two added drivers must be substantially similar to  
14 those of the mission driver, into the mission load. There may be unacceptable mission  
15 performance degradation with this approach that makes it the less commonly chosen option.

### 16 4.5.3 Single-ended Test Signal Reception

17 Figure 22 shows two options for single-ended test signal reception, again familiar from IEEE Std  
18 1149.1, but with a provision for detecting an AC test signal when the AC EXTEST instruction is  
19 loaded in the device. When AC EXTEST is loaded, a specialized test receiver (see 4.6) digitizes  
20 the test signal seen at the input and a detector block (Det) determines if this represents a ‘0’ or  
21 ‘1’. When EXTEST is loaded, the mission signal is passed to the Boundary Register cell. One  
22 option shown in Figure 22 supports INTEST (control and observe capability) and the other uses a



23 simpler observe-only structure that will not support INTEST.

24 **Figure 22: Choices for single-ended signal reception, with and without support for the INTEST**  
25 **instruction.**

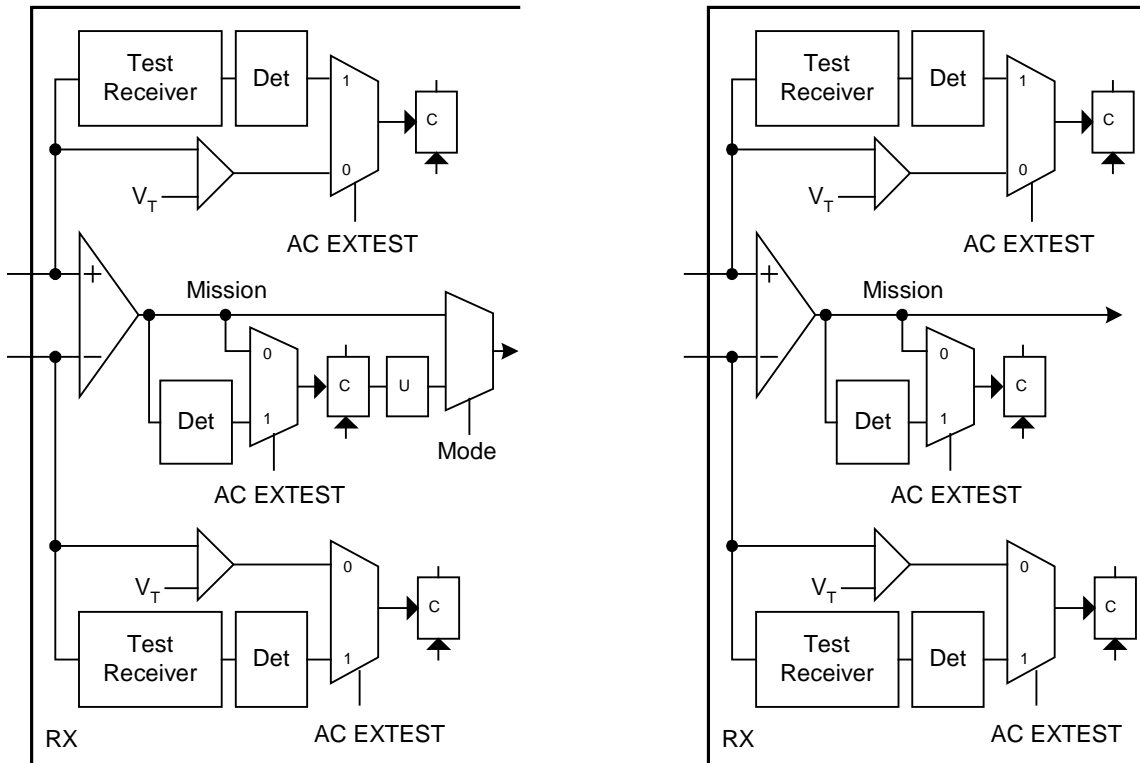
26 NOTE – The test receiver may be connected to the output of the mission input amplifier if it is a true  
27 amplifier (e.g., unity gain) rather than a threshold comparator. The test receiver is intended to process the  
28 actual waveform seen at the input pin, not an interpretation of the waveform.

29 A single-ended receiver has some form of reference used to distinguish a ‘0’ from a ‘1’ and this  
30 feature is used during (DC) EXTEST as well. However during AC EXTEST, the signal may  
31 decay to some intermediate value that cannot be reliably received by the mission receiver. The  
32 test receiver is used to sense the AC test signal.

### 33 4.5.4 Differential Test Signal Reception

34 A differential receiver is modified for testability as shown in Figure 23. The mission differential  
35 receiver path is modified to capture test data seen by the mission receiver in differential mode.  
36 The mission receiver itself is unmodified.

- 1 NOTE – As shown, the mission receiver path supports INTEST, but an observe-only structure can be used  
 2 instead if INTEST is not supported.  
 3 Each leg of the differential signal path has its own added test receiver. The purpose of this  
 4 receiver is to monitor a leg of the signal path independently. This gives additional defect  
 5 detection and diagnosis capability.  
 6 NOTE – No variations in the test receiver are needed for INTEST support since this is an observe-only  
 7 monitor.



8 **Figure 23: Differential signal reception, with and without support for the INTEST instruction.**

9 On each leg, in addition to the test receiver, there is a fixed threshold comparator (called the  
 10 “EXTEST comparator”) that compares the input waveform with a reference  $V_T$ , to produce a  
 11 logical interpretation of the input. This is used for EXTEST-based testing. The value of  $V_T$  is set  
 12 to the optimum common mode point of the mission receiver, which is the same as a referenced  
 13 termination would use.

14 The EXTEST comparator is designed to produce a deterministic output when presented with a  
 15 null input (both legs at the same voltage). When this receiver is AC coupled to a driver the  
 16 EXTEST instruction, when run at a low enough testing rate to fully discharge the coupling  
 17 capacitors, will not be able to capture the driven data, and will thus see a null condition. This will  
 18 be captured as a deterministic value. If a defect such as a shorted capacitor exists, then one of two  
 19 effects will be seen:

- 20     ▪ if the driver levels bracket the value of  $V_T$ , the driven data will be captured via the  
 21       EXTEST comparator rather than a static value, or
- 22     ▪ if the driver levels are both above or both below the value of  $V_T$ , then a static value will be  
 23       produced by the EXTEST comparator that may or may not match the null default value.

1 These facts are useful for detecting shorted coupling capacitors. An EXTEST-based interconnect  
2 test can be constructed that causes the drivers to produce a stream of data and expects the AC  
3 coupled receivers to register a known constant value if the capacitor is not shorted.

4 NOTE – If the driver levels do not bracket the value of  $V_T$ , then depending on the default value picked for a  
5 null input, the shorted capacitor may produce the same value and thus not be detected. The choice of the  
6 default value should be considered with respect to possible driver technologies that might be AC coupled to  
7 this receiver to attempt to avoid this.

8 When this receiver is DC coupled to a driver and the EXTEST instruction is executed, then one of  
9 two effects will be seen:

- 10     ▪ if the driver levels bracket the value of  $V_T$ , the driven data will be captured, in other  
11       words, the drive levels are “close enough” to the optimum common mode voltage of the  
12       receiver to register as data via the EXTEST comparator, or
- 13     ▪ if the driver levels are both above or both below the value of  $V_T$ , then a static value will be  
14       observed by the EXTEST comparator, respectively a ‘1’ or ‘0’.

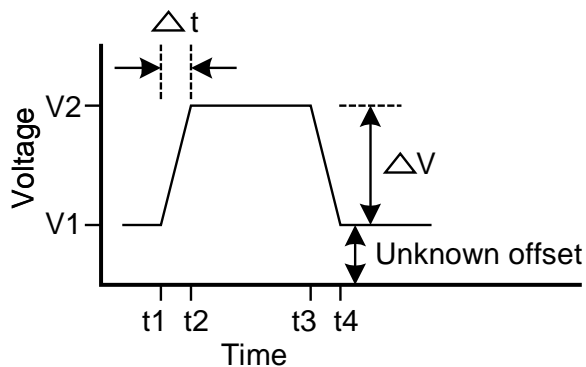
15 Thus, interconnects between DC coupled differential ICs may or may not pass data when  
16 performing EXTEST. It is probable that the fact they are DC coupled indicates they will pass  
17 EXTEST data. Test generation tools should examine the logic family information of the two ICs  
18 to determine if this will happen.

19 NOTE – Logic family information is not included in the definition of BSDL and must come from other  
20 data sheet sources.

21 Since the signals on a DC coupled differential pair may contain a significant common mode  
22 offset as well as the test signal, the design of the AC EXTEST test receiver must account for the  
23 fact that there is no fixed reference available to discriminate a ‘0’ from a ‘1’. A general discussion  
24 of the test receiver is given in sections 4.6 through 4.8, and rules for its implementation are given  
25 in section 6.1.

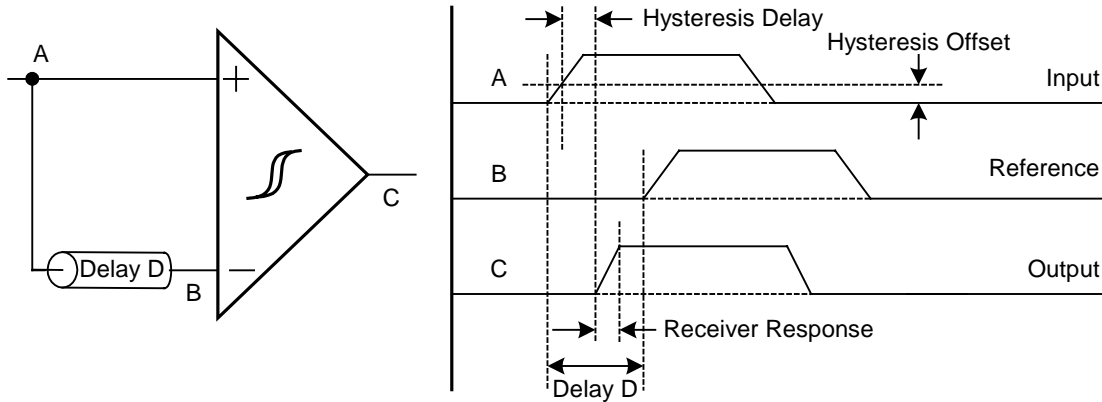
#### 26 **4.6 Test Receiver Support for the AC EXTEST Instruction**

27 The principle purpose of the test receiver seen in Figure 22 and Figure 23 is to extract a test  
28 signal that may contain an offset. Because of the offset, a simple comparison of the test signal to a  
29 static reference may not reliably extract the test signal. Using the opposite leg of the pair as a  
30 reference (as is done by the mission receiver) will often mask important defects. A solution is to  
31 look for information contained in the *transitions* of the signal. These will be independent of the  
32 offset seen in Figure 24. Valid transitions have a defined voltage swing  $\Delta V$  and slew rate  $\Delta t$ .



33 **Figure 24: A signal with unknown voltage offset and the signal transitions it contains.**

1 One way to find the transitions in a signal with an unknown offset is to compare the signal with a  
2 delayed version of itself, that is, to use its recent history as a reference. This is diagramed in  
3 Figure 25. The original signal, a delayed version and the output of the hysteretic comparator are  
4 shown. The output is a faithful reconstruction of the original waveform, delayed by the time it  
5 takes for the input waveform to pass the hysteresis threshold. The output waveform has been  
6 converted to standard logic levels, that is, the unknown offset is removed.



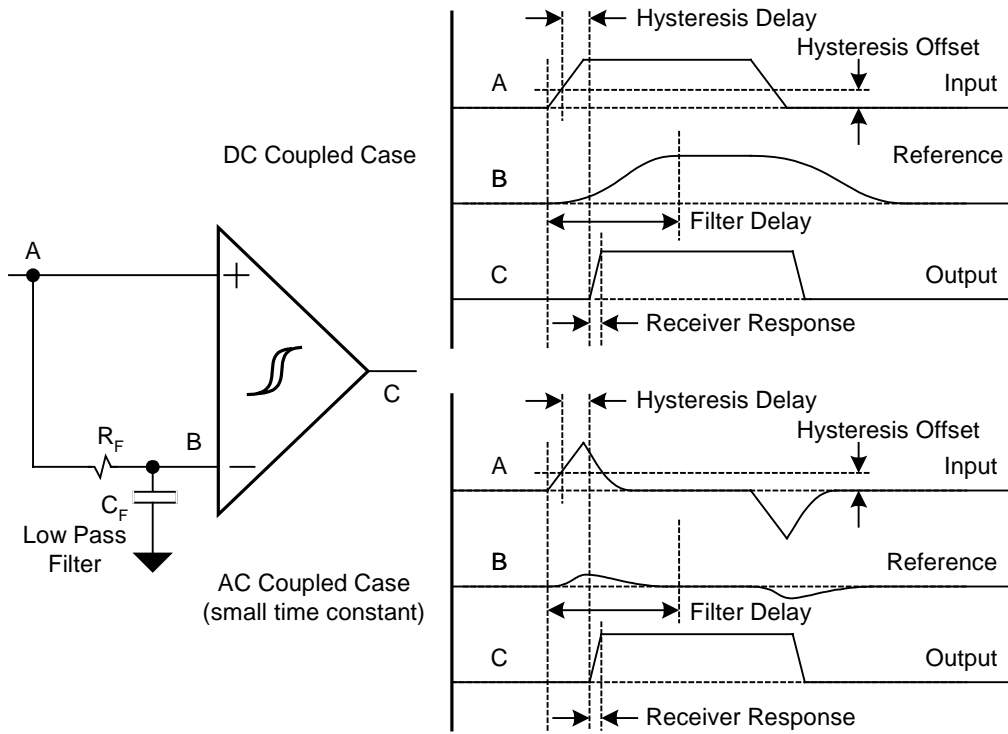
7 **Figure 25: Delayed self-referenced reconstruction of a DC coupled input waveform with unknown**  
8 **voltage offset.**

9 It will be important to assure that the delay D is longer than the transition times to be sensed. The  
10 use of hysteresis (the hysteresis voltage) can eliminate unwanted response to small signal noise  
11 (runt pulses). Additional filtering in the design of the comparator (the hysteresis delay) can  
12 eliminate response to larger signal noise of insufficient duration (noise spikes).

13 The waveforms that are applied to the test receiver may or may not be AC coupled to the driver.  
14 When AC coupled they may or may not decay significantly depending on the coupling time  
15 constant. In the case in Figure 25 the test receiver is either DC coupled or AC coupled with a very  
16 long time constant. If AC coupled signals with periods long with respect to the coupling time  
17 constant are applied to this simple circuit, the decaying signals will cause the comparator to reset  
18 itself early (after delay D) in response to the delayed reference edges and the reconstructed  
19 waveform will differ from the original.

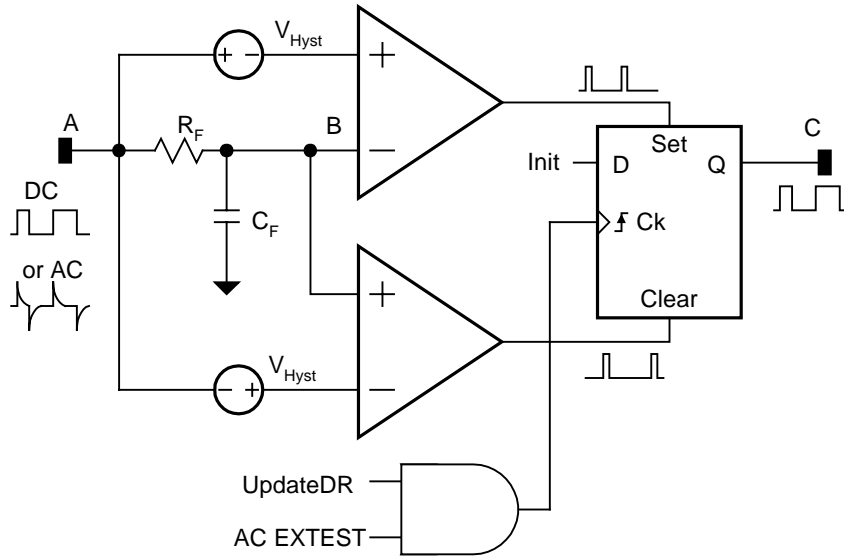
20 A low pass filtered delay solves this problem as shown in Figure 26. The simple low pass filter  
21 with a filtering time constant of  $R_F * C_F$  is used to hold the reference input to the test receiver at a  
22 constant value that is largely unaffected by short term events such as the high-pass filtered edges  
23 seen when AC coupling (low time constant) is used. If high time constant AC coupling, or DC  
24 coupling is used, then the low pass filter adjusts the reference point again to represent near term  
25 history of the input signal. The hysteresis voltage and hysteresis delay are used to control  
26 response to noise.

27 To summarize the concepts shown in Figure 26, the test receiver reconstructs an original  
28 waveform driven from either a single-ended driver or one leg of a differential driver, that is either  
29 AC or DC coupled, and is insensitive to DC offsets that may exist in the driven waveform. It does  
30 this by responding to the edges of the original waveform that are still present despite DC or AC  
31 coupling.



1 **Figure 26: Delayed and filtered self-referenced waveform reconstruction of both DC and AC coupled**  
2 **waveforms by a test receiver.**

3 Figure 27 shows one possible implementation of the concept shown in Figure 26. There are two  
4 simple comparators, one to sense rising edges and the other to sense falling edges. The  $V_{Hyst}$   
5 voltage sources set the hysteresis voltage for the comparators. The internal delay of the  
6 comparators determine the hysteresis delay. The comparator outputs set or clear a D-type flip-  
7 flop. The values of  $R_F$  and  $C_F$  are chosen to cause a delay longer than the expected transition  
8 times being sensed.



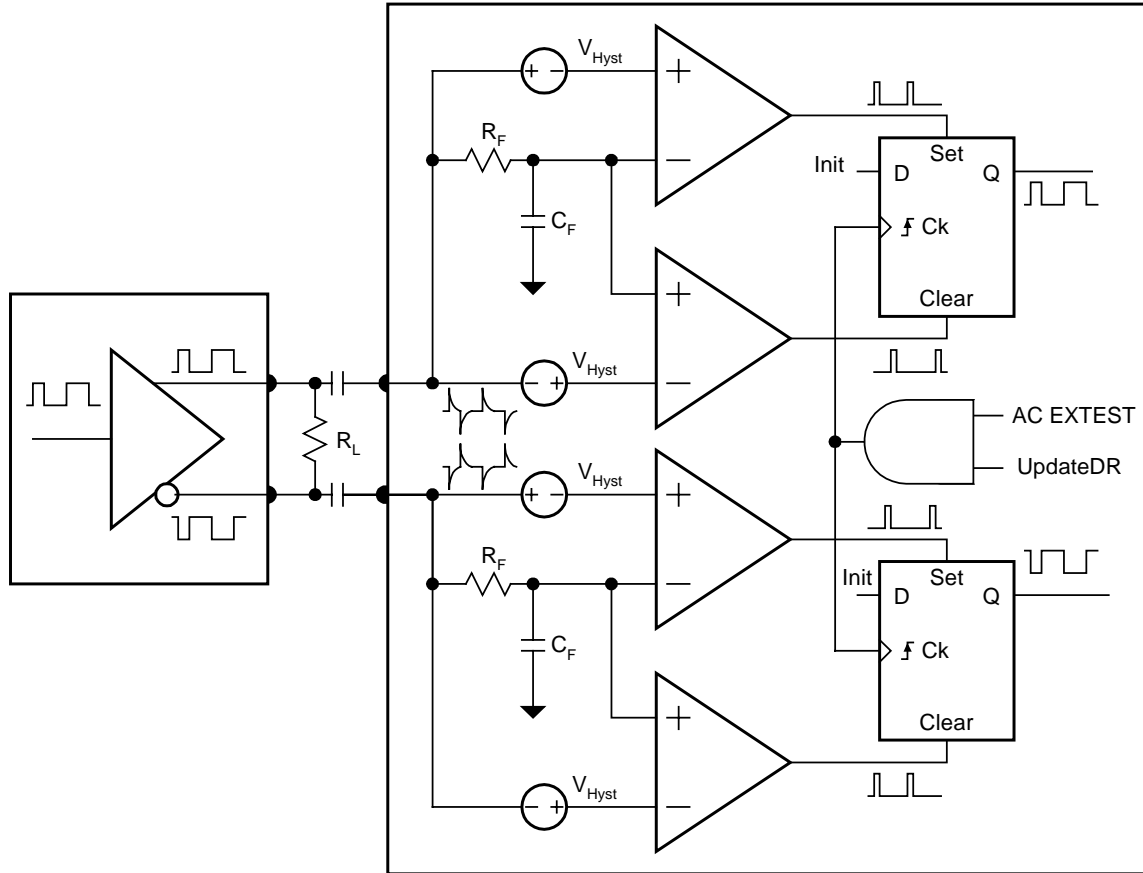
1 **Figure 27: A simple test receiver implementation possibility for the concept in Figure 26.**

2 NOTE 1 – Typical values of  $R_F$  and  $C_F$  might be 5 Kohms and 5 picofarads which could be integrated into  
3 an IC.

4 NOTE 2 – The input waveform at point A may be high-pass filtered by AC coupling, or it could be a  
5 normal DC coupled digital waveform (with an unknown offset). In either case, the edges are used to  
6 reconstruct the original digital waveform.

7 NOTE 3 – The D-type flip-flop element can be initialized by the Update clock to establish a known initial  
8 state at the time the drivers are triggered. The initialization value will be discussed later.

9 Figure 28 shows an AC coupled differential signal channel from the drive side, done  
10 differentially, to the receive side which is single-ended for test purposes. (The mission receiver  
11 has been omitted for clarity.) This supports the AC EXTEST instruction.



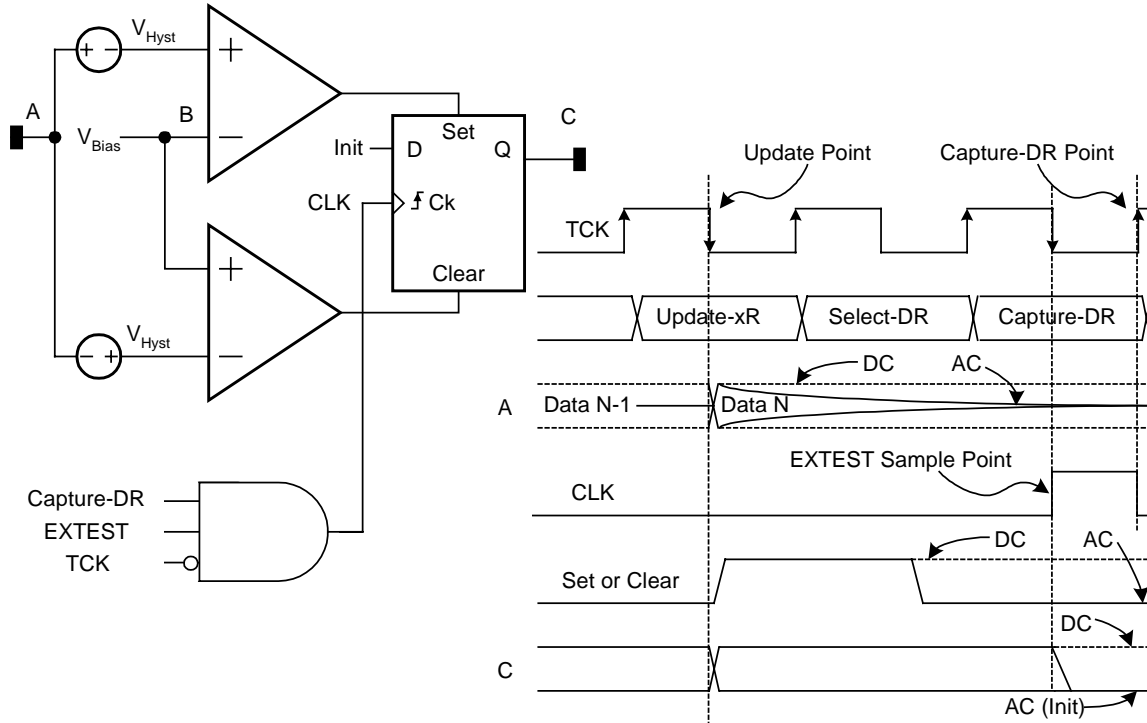
1 **Figure 28: Differential driver, AC coupling, and receiver testability structure.**

2 NOTE – In Figure 28 the mission receiver has not been shown. It would include load termination that  
3 would determine the time constant of the AC coupling.

4 **4.7 Test Receiver Support for the (DC) EXTEST Instruction**

5 The test receiver behavior for AC EXTEST has been described. However it also is important to  
6 support the standard (DC) EXTEST instruction. This amounts to “turning off” the edge  
7 integrating capability of the test receiver and having it respond only to levels. This is further  
8 complicated by the problem that there may be common mode offsets added to the signals. This  
9 necessitates choosing a reference voltage that can be used for single-ended comparison.

10 One choice is to use the internal bias voltage  $V_{Bias}$  used to set the  $V_{Com}$  point of the mission  
11 receiver (the “sweet spot”) as shown in Figure 29. This bias voltage will work well as a static  
12 reference for the test receivers when AC coupling is used. If the receiver IC is DC coupled to the  
13 driver, then the test receiver may or may not receive data depending on whether  $V_{Bias}$  is between  
14 the high and low values driven by the driver. If data is not received, the test receiver will perceive  
15 a constant logic value, either 1 or 0.



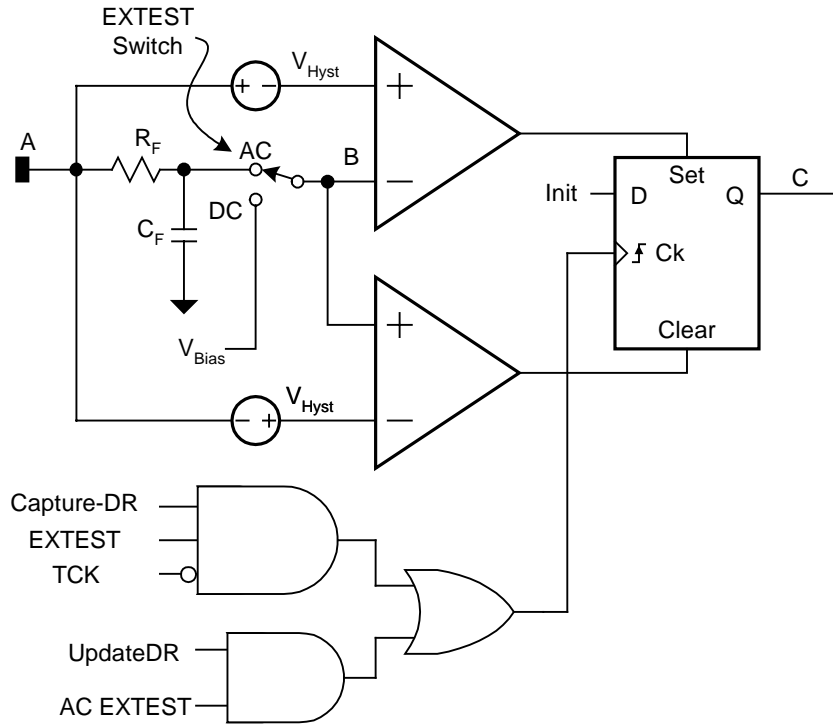
1 Figure 29: Static reference used to support (DC) EXTEST. Comparators may set or reset the  
2 hysteresis flip-flop just before the rising edge of TCK in the Capture-DR state.

Editor's note: In the above figure, the value of  $V_{Hyst}$  should be half that used for the self-referenced comparison. This error appears throughout and needs correction.

3 If the test receiver is responding to the EXTEST instruction but the receiver is AC coupled to the  
4 driver, there is the chance, particularly if the coupling time constant is longer, that the receiver  
5 will respond to a change in the driven data (see waveforms in Figure 29). The flip-flop is clocked  
6 in the Capture-DR state to set a default initial state. If there is a DC level on the test receiver  
7 input, this will override the the initial state. If the levels have decayed due to AC coupling, then  
8 the initial state will not be overridden. Extra time for signal decay can be inserted by spending  
9 time in the Run-Test/Idle state.

#### 10 **4.8 A General Test Receiver for DC and AC EXTEST Instructions**

11 A test receiver that supports both the AC and (DC) EXTEST instructions is required. This could  
12 be accomplished simply by taking the two structures already shown and selecting between them  
13 with multiplexers. However it is possible to merge their behaviors into a more efficient structure  
14 as shown in. In this structure an analog multiplexer selects between (DC) EXTEST support and  
15 AC EXTEST support.



1 **Figure 30: A test receiver structure that supports both AC and (DC) EXTEST.**

2 **4.9 Boundary-Scan Capture Data Versus Configuration**

3 The content of Table 1 shows what Boundary-Scan data will be captured by a test receiver for  
4 various combinations of coupling, DC compatibility and whether a given IC is executing  
5 EXTEST or AC EXTEST.

**Editor's Note:** Because we haven't yet decided on the data protocol being used, the info in Table 1 below contains some "protocol dependent" fields that will be filled in when we pick a protocol.

6

1 Table 1: Boundary-Scan capture results for various combinations of coupling, test instruction and  
2 driver-to-receiver DC compatibility.

Driver to Receiver Coupling	Test instruction loaded in:		Capture result when DC levels of driver and receiver are:		Comments
	Driving IC	Receiving IC	Compatible	Incompatible	
DC	EXTEST		Data (Note 1)	Fixed 1 or 0 (Note 2)	Typical test for DC coupling
	AC EXTEST		Data		AC test on DC coupled paths may be forced by board topology .
	EXTEST	AC EXTEST	Protocol Dependent (Note 3)	Protocol Dependent	Edge based approach will not get its “throat cleared” because driver is in EXTEST. May transmit data but there is a noise issue.
	AC EXTEST	EXTEST	Protocol Dependent	Fixed 1 or 0	Edge based approach will transmit data
AC	EXTEST		Default (Note 4)		Used to test shorted capacitors. Will pass data (a failure) or will register a (possibly passing) fixed value.
	AC EXTEST		Data		Typical test for AC coupling.
	EXTEST	AC EXTEST	Protocol Dependent	Protocol Dependent	Edge based approach will not get its “throat cleared” because driver is in EXTEST. May transmit data but there is a noise issue.
	AC EXTEST	EXTEST	Default		With edge based approach, may be used to test shorted capacitors.

3 NOTE 1 – In Table 1, “data” indicates Boundary-Scan data is successfully transmitted.

4 NOTE 2 – “Fixed 0 or 1” indicates the incompatible levels will be seen as either a 1 or 0 depending on  
5 where the receiver threshold is set.

6 NOTE 3 – “Protocol Dependent” indicates the signaling protocol will determine the result (TBD). In some  
7 cases data may be transmitted. In other cases the result is nondeterministic.

8 NOTE 4 – “Default” indicates the response is the same that a floating test receiver would produce.

1

2 **4.10 Noise Sources and Sensitivities**

**Editor's Note:** The following section will discuss the sources of noise, how the Test Receiver is sensitive to noise, and how to avoid susceptibility. This will offer guidance to IC designers, board designers, and test engineers. Rules that appear in later clauses will specify Test Receiver noise characteristics relative to the mission mode of the system. Not clear if we can impose rules on board designers or test engineers.

3

4 **4.10.1 Noise Sources that Affect Mission Operation**

5 Ground bounce, signal coupling, EMI

6 **4.10.2 Noise Sources Unique to Testing**

7 Intra-IC noise generation (lobotomy effect), rogue signals on the board, impedance mismatches

8 **4.10.3 Noise Sources Exacerbated by Testing**

9 Ground bounce, signal coupling

10 **4.10.4 Avoiding Noise**

11 Hysteresis voltages, hysteresis delay, self-reference filtering, use of the Run-Test/Idle state, noise  
12 rejection of the data protocol, limits on ATPG

13

# 1 5 TAP Instructions

## 2 **5.1 IEEE Std 1149.1 Instructions**

3 All TAP instructions provided by IEEE Std 1149.1 perform as specified in that standard for all  
4 DC pins. For AC pins, all IEEE Std 1149.1 instructions perform as specified with the exception  
5 of the introduction of hysteresis behavior for AC input pins. (See section 6.1.2.)

### 6 5.1.1 Rules

7 a) All instructions specified by IEEE Std 1149.1 shall perform as specified in that standard,  
8 and for any such instruction that controls or observes pin, all DC pins shall also perform  
9 as specified by that standard.

10 NOTE – The AC pins shall perform per rules specified herein.

### 11 5.1.2 Description

12 The IEEE Std 1149.1 standard is the underpinning for this standard

## 13 **5.2 The AC\_EXTEST Instruction**

14 This standard specifies a new test mode instruction, AC\_EXTEST, that governs new capabilities  
15 defined for AC pins (see 4.1). All DC pins will perform as if the IEEE Std 1149.1 EXTEST  
16 instruction is operating whenever the AC\_EXTEST instruction is effective.

### 17 5.2.1 Rules

18 a) An AC\_EXTEST instruction shall be provided for components that possess AC pins, and  
19 the component designer shall select the opcode(s) for this instruction.

**Editor's Note:** I have left the door open here for:

1. A device with zero AC pins not implementing AC\_EXTEST, and
2. Other instructions we may decide to implement (e.g, for I/O configuration support).

20 b) The AC\_EXTEST instruction shall become effective at the falling edge of TCK in the  
21 *Update-IR* TAP Controller state.

22 NOTE – By “effective” it is meant that (enabled) AC drive pins shall respond to the content of the  
23 Boundary Scan register as discussed in section 6.2.2, and AC receive pins shall behave as discussed in  
24 section 6.1.3.

25 c) The AC\_EXTEST instruction shall remain effective in the *Run-Test/Idle* TAP Controller  
26 state.

27 NOTE – See section 6.2.3 for activities controlled by AC\_EXTEST in the *Run-Test/Idle* TAP Controller  
28 state.

29 d) DC pins shall perform exactly as specified for the EXTEST instruction by IEEE Std  
30 1149.1 whenever the AC\_EXTEST instruction is effective.

### 31 5.2.2 Description

32 The AC\_EXTEST instruction implements new test behaviors for AC pins, and simultaneously  
33 behaves identically to IEEE Std 1149.1 EXTEST for DC pins. (See Clause 6 for the specification  
34 of AC test behavior.)

- 1 The AC\_EXTEST instruction enables edge-detecting behavior (see section 6.1.3) on signal paths
- 2 containing AC pins, where test receivers reconstruct the original waveform created by a driver
- 3 even when signal decay due to AC coupling is present.
- 4 The (DC) EXTEST instruction enables level-detecting behavior (see section 6.1.2) on signal
- 5 paths containing AC pins. This instruction is useful for detecting shorted capacitors on AC
- 6 coupled paths.

# 6 Pin Implementation Specifications

## 6.1 Input Test Receivers

All AC pins (see 4.1) that receive data into an IC are equipped with test receivers. Single-ended AC pins will have one test receiver and differential channels will have one test receiver per leg. The IC designer will design the mission performance of the input to accept some range of voltage changes and slew rates. The rules given below assume that an input will respond to a minimum input voltage change and that the slew rate of input changes will be at or above some minimum, because AC coupling is anticipated or even built into the IC itself. These minimums are defined by the performance requirements of the mission of the IC and are depicted in Figure 31 for both AC and DC coupled signals.

When AC EXTEST is in effect, it is the purpose of the test receiver to reconstruct the test waveform driven by the upstream driver when either AC or DC coupling is used. It does this by reacting to the edges and not the levels of the input waveform. When DC EXTEST is in effect, the test receiver behaves as a level detector.

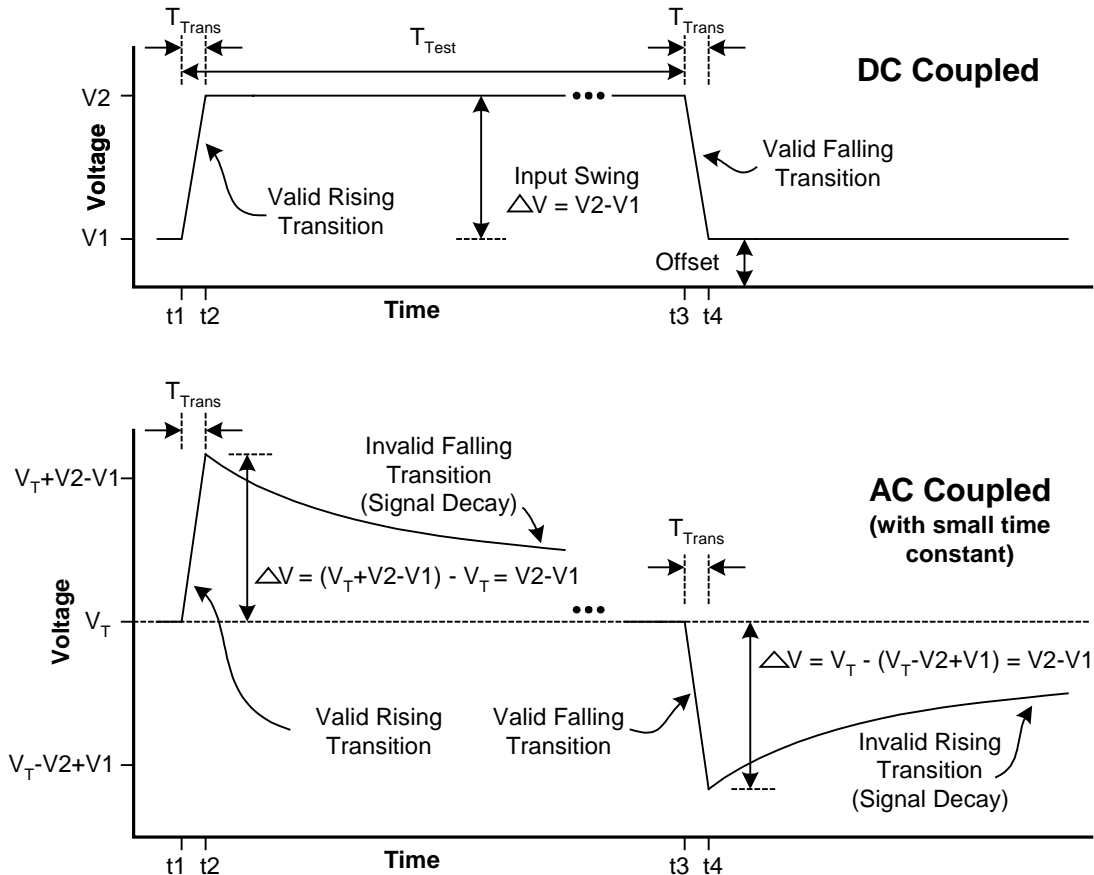


Figure 31: Definitions of voltage changes and transition times for waveforms presented to the test receiver using either DC or AC coupling.

The value of  $T_{Test}$  is the minimum time between signal transitions that can be caused by Boundary-Scan testing. This value is governed by test-related parameters such as TCK frequency for the device.

1 NOTE – IEEE Std. 1149.1 EXTEST does not take attenuation or transition time into account. The test  
2 transitions are very far apart (at best, once per scan of the boundary register), but the receiver values are  
3 captured 2.5 TCK cycles after a possible transition. Therefore, for DC EXTEST,  $T_{\text{Test}}$  should be assumed to  
4 be 2.5 times the minimum TCK period for the chip.

5 The *minimum input swing*, termed  $\Delta V_{\text{Min}}$ , is the smallest change in voltage during an active  
6 transition ( $\Delta V$  in Figure 31) that is expected to occur during tests specified by this standard.  
7 Typically, this will be the  $\Delta V_{\text{Min}}$  of a driver of the same protocol and technology reduced by some  
8 factor to account for attenuation expected at the maximum test frequency ( $1/(2 * T_{\text{Test}})$  in Figure  
9 31). This attenuation is generally significantly less than the attenuation expected at maximum  
10 functional channel frequency. The transition time,  $T_{\text{Trans}}$  in Figure 31, is the maximum amount of  
11 time this minimum voltage swing is expected to take. Signal transitions that take significantly  
12 longer than  $T_{\text{Trans}}$  are not considered valid. For example in Figure 31, the passive, undriven,  
13 falling decay on a capacitively coupled signal that follows an actively driven rising transition is  
14 not a valid falling transition. The rules that follow will define a test receiver that can differentiate  
15 a valid signal transition from a decay transition.

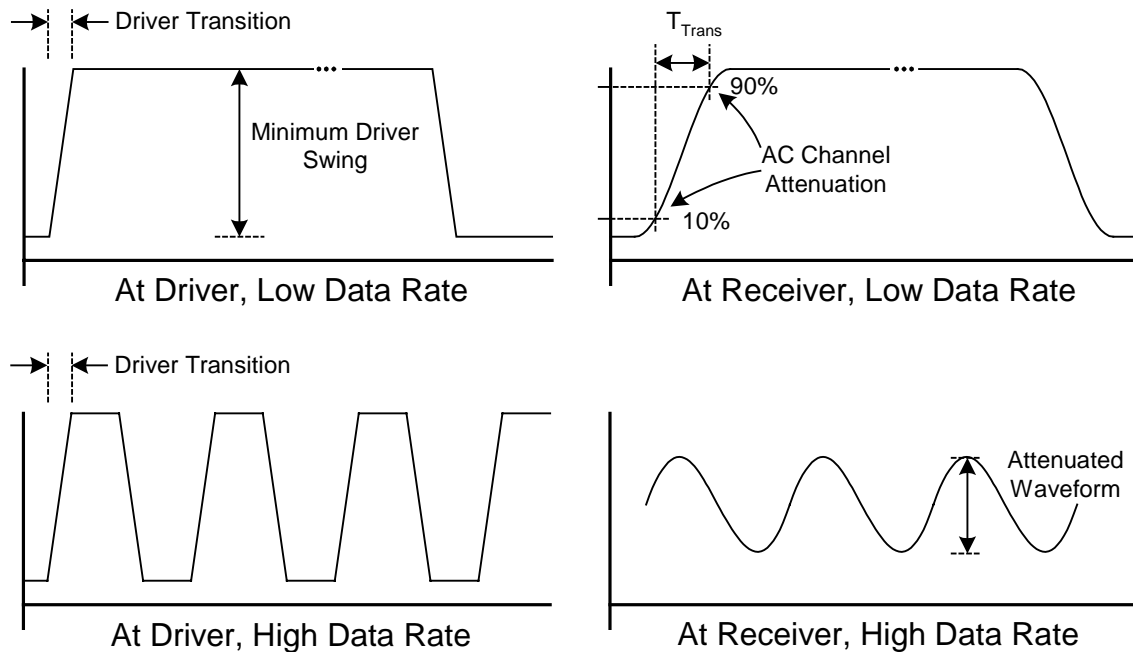
16 In the following rules, a designer is required to identify parameters such as minimum and  
17 maximum voltage swing ( $\Delta V_{\text{Min}}$ ,  $\Delta V_{\text{Max}}$ ) and maximum transition time ( $T_{\text{Trans}}$ ), but with some  
18 latitude.

19 The preferred way to determine these parameters is to start with the transmission protocol  
20 specification. For example, the LVDS Standard (IEEE Std 1596.3, or ANSI/TIA/EIA-644)  
21 specifies that the voltage swing at the driver should be 454mv maximum and 247mv minimum. It  
22 also states the voltage swing at the receiver should be 100mv minimum, but this is at maximum  
23 data rate, as shown in Figure 32. The standard does not state an expected attenuation at a slower  
24 test data rates, e.g., 5 - 50MHz, but conservative engineering judgement might suggest that the  
25 minimum voltage swing at the receiver, for that frequency, would be no less than, for example,  
26 80% of the minimum swing at the driver, or about 200mv in this example. The maximum swing  
27 of the driver (454mv) could then be used as  $\Delta V_{\text{Max}}$  and the attenuated minimum swing of the  
28 driver (200mv) used as  $\Delta V_{\text{Min}}$ .

29 The LVDS standard further specifies a maximum driver transition time of 1.5ns for data rates  
30 greater than 200Mbps, or 30% of the bit-width otherwise. The standard documented here  
31 provides that the transition time of the driver is the same in test mode as in functional operation,  
32 so one should be able to use this same value for test. However, the transition time at the receiver  
33 will be longer than the transition time at the driver due to high frequency attenuation, even in low  
34 data-rate operation. So at the receiver, a better estimate for  $T_{\text{Trans}}$  would be 50% of the minimum  
35 bit time (25% of the maximum channel frequency cycle time) since longer transition times than  
36 that would cause severe amplitude attenuation at the maximum data rate and probably  
37 compromise the reliability of the channel. To continue the example, assume an LVDS driver and  
38 receiver designed for 200Mbps maximum bit rate, then the bit time would be 5ns. The LVDS  
39 Standard dictates 30% of the bit time, or 1.5ns, for the driver transition time, and for this Standard  
40 one could use 50% of the bit time, or 2.5ns, for the receiver transition time called  $T_{\text{Trans}}$ .

41 When there is no other guidance, a possible way to determine these parameters is to consider the  
42 actual characteristics of a driver implemented in the same technology for the same channel  
43 protocol. Over acceptable manufacturing process variation, temperature variation, etc, this driver  
44 will produce a maximum and a minimum voltage swing into a specified range of loads. This  
45 voltage swing will normally be larger than needed to assure the receiver reliably recovers data, to  
46 allow for high frequency attenuation in the channel between the driver and receiver (see Figure  
47 32). As described above for the LVDS example, a conservative attenuation factor for the  
48 maximum expected test frequency can be determined using appropriate engineering tools and  
49 judgement and applied to the minimum voltage swing to determine an appropriate minimum

1 voltage swing during test at the test receiver. (The maximum voltage swing is not usually  
2 adjusted to allow for very tight coupling with negligible attenuation.)



3 **Figure 32: Driver waveform and the attenuated waveform seen at the receiver. The attenuation is a**  
4 **function of driver data rate.**

5 In addition, both driver and receiver will be designed for a specific maximum channel frequency  
6 or bit width. Again, a good estimate for  $T_{Trans}$  at the receiver, in a typical channel design, would  
7 be 50% of the bit width or 25% of the cycle time at maximum frequency.

8 If the designer is expecting the receiver to be connected, AC or DC coupling, to a driver of a  
9 different transmission protocol, or implemented in a different technology, then analysis of the  
10 board channel design will have to be performed to verify that the channel will attain the desired  
11 data rate. By extending this analysis, using the techniques described above, the designer can  
12 determine the required parameters.

13 These types of considerations allow the designer to define the minimum and maximum voltage  
14 swings and transition time required by the following rules. This “test design point” information  
15 may be supplied as part of the data sheet for the final device.

16 The offset voltage shown in Figure 31 may vary depending on different circuit configurations.  
17 For example, an IC with an input pin possessing a test receiver may be AC or DC coupled to a  
18 driver intentionally by a board designer. Depending on which is chosen, there could be different  
19 offsets observed at the test receiver. When a defect occurs, the coupling may be affected. For  
20 example, a shorted coupling capacitor may create DC coupling to a receiver that was designed to  
21 be AC-coupled.

## 22 6.1.1 General Properties of AC Input Pins and Test Receivers

### 23 6.1.1.1 Rules

24 a) All AC pins that receive input data, whether they are single-ended or part of a differential  
25 pair, shall have a test receiver function attached to the pin.

26 NOTE – This rule applies to input and bidirectional pins (see AC pin definition in section 4.1).

- 1       b) With respect to the required or expected mission behavior of the input signal at an AC  
2       input pin, the device designer shall identify a *minimum valid signal transition* in terms of  
3       its *minimum input swing* ( $\Delta V_{\text{Min}}$ ) and *maximum transition time* ( $T_{\text{Trans}}$ ) over which this  
4       minimum input swing may occur.

5       NOTE 1 – In the event that the pin is one-half of a differential pair, the determination of  $\Delta V_{\text{Min}}$  is with  
6       respect to a fixed reference (e.g., ground) and not with respect to the other member of the differential pair.

7       NOTE 2 – If the transition times of rising and falling edges are different, then the longer of the two is  
8       defined as the maximum.

9       NOTE 3 – See permission 6.1.1.2c) for the case where there is no maximum transition time specification  
10       for the mission receiver. See also the discussion in section 6.1 on determining  $T_{\text{Trans}}$ .

- 11       c) With respect to the required or expected mission behavior of the input signal at an AC  
12       input pin, the device designer shall identify a *maximum valid signal transition* in terms of  
13       its *maximum input swing* ( $\Delta V_{\text{Max}}$ ).

14       NOTE – If the pin is bidirectional, then the pin driver may determine  $\Delta V_{\text{Max}}$ , but some external, AC  
15       attenuated driver may determine  $T_{\text{Trans}}$ .

- 16       d) The test receiver shall be implemented to operate in two modes of operation:  
17            i. a level-detecting mode selected by the (DC) EXTEST instruction (see specific-  
18            ations in section 6.1.2), and  
19            ii. an edge-detecting mode selected by the AC\_EXTEST instruction (see specific-  
20            ations in section 6.1.3).  
21       e) The test receiver shall be implemented with hysteresis voltage offsets for the two  
22       operational modes called:  
23            i.  $V_{\text{Hyst\_Level}}$  in the level-detecting mode (see detail in section 6.1.2), and  
24            ii.  $V_{\text{Hyst\_Edge}}$  in the edge-detecting mode (see detail in section 6.1.3).

### 25   6.1.1.2 *Permissions*

- 26       a) A test receiver may be isolated from its pin with a linear buffer as long as it still sees the  
27       actual waveform appearing on the pin.  
28       b) Circuitry needed to implement the test receiver may be shared with that needed for the  
29       implementation of the mission receiver, as long as all rules for this standard are observed.  
30       c) If the mission receiver has no specification for a maximum transition time, then the value  
31       of  $T_{\text{Trans}}$  may be chosen to match the maximum expected transition time for an upstream  
32       driver that is in test mode, taking into account any expected AC attenuation in the path.

33       NOTE – See the discussion in section 6.1 on determining  $T_{\text{Trans}}$ .

### 34   6.1.1.3 *Description*

35       The rules and permissions in Section 6.2.1 require that there be a bimodal test receiver on each  
36       and every AC input pin, and then define five electrical parameters, based on the expected  
37       mission-mode input signal, that shall be used to design the test receiver. Consider rule 6.1.1.1b).  
38       This rule applies to signal transitions within any common mode or fixed voltage range definition  
39       of the mission of the pin. Changes outside of this range are not valid signal transitions. For  
40       example, a signal transition that forward biases input protection diodes would be outside the  
41       normal operating range of the receiver. In addition, the minimum valid signal transition is the  
42       smallest, slowest transition that represents a valid state change of the signal, i.e., that represents a  
43       change in signal data (and is to be differentiated from a signal decay seen in an AC coupled  
44       channel). This could be determined by examining the characteristics of a driver implemented in  
45       the same technology, its minimum specifications, and the maximum amount of signal attenuation

1 allowed between the driver and receiver. The transition parameters ( $T_{\text{Trans}}$  and  $\Delta V_{\text{Min}}$ ) are used in  
2 subsequent rules.

3 Permission 6.1.1.2c) allows a device designer to substitute the maximum transition time of an  
4 upstream driver in test mode that is expected to be connected to this test receiver. This handles  
5 the case where there is no maximum transition time specified for the mission receiver, for  
6 example, a low frequency analog input. A designer can thus avoid having to implement edge-  
7 detection for very slow edges. However the designer must assure that the upstream driver's  
8 parameters are known, which is often the case for custom designs or standard logic families.

9 Rule 6.1.1.1c) defines a maximum input voltage swing. This value, the tolerable amount the  
10 receiver can be overdriven, is used in subsequent rules to improve the noise immunity of the test  
11 receiver.

12 Rule 6.1.1.1d) requires that the test receiver have a level-detection mode (familiar from IEEE  
13 Standard 1149.1) and also an edge-detecting mode. The edge-detecting mode is required since  
14 AC coupling is a high-pass filter that will not propagate DC levels.

15 Rule 6.1.1.1e) states the test receiver will be implemented with voltage hysteresis levels, with a  
16 specification for level and edge detecting modes. While this hysteresis provides noise immunity,  
17 it also defines the test receiver as having three possible detection states: legal "one", legal "zero",  
18 and an "indeterminate" value in between. Due to the behavior of DC signals when transmitted on  
19 an AC-coupled net, the explicit detection of the "indeterminate" input state is critical to defect  
20 detection and diagnosis. More specifications on edge and level detection are given in the  
21 following sections as a function of these hysteresis parameters.

## 22 6.1.2 Level Detection Behavior of Input Test Receivers

23 The level detection behavior is selected by the (DC) EXTEST instruction from IEEE Std 1149.1.

### 24 6.1.2.1 Rules

- 25 a) For the level-detection mode of a test receiver, the device designer shall identify a fixed  
26 threshold voltage  $V_{\text{Threshold}}$  that defines the mid-range of the minimum input voltage  
27 swing  $\Delta V_{\text{Min}}$ , and the designer shall identify a hysteresis voltage offset value  $V_{\text{Hyst\_Level}}$ .
- 28 b) Whenever a test receiver is operating in level-detection mode on an AC input pin, the test  
29 receiver shall:
- 30 i. determine the logic value on the pin by comparing the current voltage on the pin to a  
31 fixed threshold voltage  $V_{\text{Threshold}}$  for a minimum period of time called the hysteresis  
32 delay ( $T_{\text{Hyst}}$ ) and,
  - 33 ii. produce a one only after this period has elapsed, if the voltage continuously  
34 compares greater than this threshold  $V_{\text{Threshold}}$  plus the hysteresis voltage  $V_{\text{Hyst\_Level}}$   
35 or,
  - 36 iii. produce a zero only after this period has elapsed, if the voltage continuously  
37 compares less than this threshold  $V_{\text{Threshold}}$  minus the hysteresis voltage  $V_{\text{Hyst\_Level}}$ .
- 38 c) The delay period ( $T_{\text{Hyst}}$ ) shall be chosen by the device designer by considering recom-  
39 mendation 6.1.2.3a).

**Editors Note:** The next three rules may need modification depending on the type of signaling protocol we chose.

- 40 d) Whenever a test receiver is operating in the level-detection mode on an AC input pin, the  
41 test receiver output shall be forced to a known initial value on the falling edge of TCK in

1 the Capture-DR TAP controller state, and this initial value shall be retained as long as  
2 there is not a valid logic level on the pin, as described in rule b) above, during the period  
3 from the fall of TCK to the rise of TCK in the Capture-DR TAP controller state.

4 e) Whenever a test receiver is operating in the level-detection mode on an AC input pin and  
5 there is a valid logic level on the pin as described in rule b) above that remains or  
6 becomes valid after the fall of TCK in the Capture-DR TAP controller state, the test  
7 receiver output shall assume the value corresponding to the most recent valid input level  
8 and that value shall be retained until the rising edge of TCK in the Capture-DR TAP  
9 controller state

10 f) Whenever a test receiver is operating in level-detection mode on an AC input pin, the  
11 output of the test receiver shall be captured in the capture latch of the Boundary-Scan  
12 register cell associated with the pin at the rising edge of TCK in the Capture-DR TAP  
13 controller state.

#### 14 6.1.2.2 Permissions

15 a) Per rules 6.1.2.1d) through f), the output of the test receiver is only relevant during the  
16 window of time between the rising and falling edges of TCK in the Capture-DR TAP  
17 controller state, and this output may be considered a “don’t care” at other times.

#### 18 6.1.2.3 Recommendations

19 a) The amount of hysteresis delay  $T_{\text{Hyst}}$  should be chosen by the designer to reject common  
20 noise sources such as ringing or over/undershoot that may occur on a signal pin.

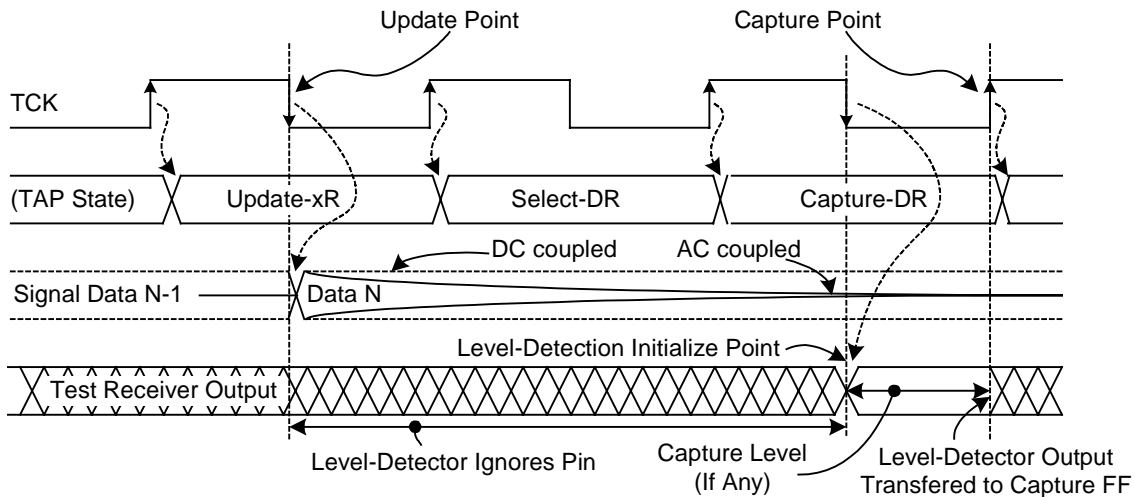
#### 21 6.1.2.4 Description

22 In level-detection mode, the test receiver is a fixed-threshold single-ended logic comparator with  
23 hysteresis. Per rule 6.1.2.1a), the designer defines the parameters of this comparator. Because of  
24 this single-ended fixed-threshold nature, it is possible that a test receiver in level-detection mode  
25 will not be able to discern both logic states produced by an upstream driver when they are DC  
26 coupled. This can happen when a driver from a dissimilar logic family is DC coupled to a  
27 receiver, or when a shorting defect in an AC coupled structure creates a DC coupling. (The edge-  
28 detection mode, described in section 6.1.3, overcomes this problem.)

29 Rule 6.1.2.1b) defines a *valid logic level* as a signal persisting at one logic level at least a  
30 hysteresis level beyond the threshold for a minimum period of time. The IC designer may choose  
31 a threshold value at the midpoint of a voltage swing deemed optimal for the mission receiver.  
32 This may be the same voltage used to bias the mission receiver when it is AC coupled as seen in  
33 Figure 12 (page 17). The hysteresis voltage ( $V_{\text{Hyst\_Level}}$ ) will eliminate response to small-amplitude  
34 noise. The hysteresis delay period ( $T_{\text{Hyst}}$ ) will eliminate response to short-duration large-  
35 amplitude pulses. For example, if the hysteresis delay is set to 5 times the value of  $T_{\text{Trans}}$ , this will  
36 allow the receiver to ignore typical ringing that may occur on transitions or due to other coupled  
37 noise. The designer should contemplate the nature of noise sources that may impact signals  
38 received at a pin when choosing the hysteresis delay. (See section 4.10.)

39 Rules 6.1.2.1d) and e) define the behavior of the hysteretic memory of this level detection. If  
40 during the time between the falling edge of TCK and the capture of data at the rising edge of  
41 TCK in the Capture-DR TAP controller state there is a valid level, this level is captured. If the  
42 level is not valid, then a default initial value is captured (see Figure 33). This determines the  
43 result when an AC coupled signal decays to an invalid level before the sample interval. The time  
44 between the falling and rising edges in the Capture-DR TAP controller state is a window of input  
45 observation and of vulnerability to noise events with magnitude sufficient to disturb the validity

1 of the level appearing on the pin. See Figure 29 (page 31) for an example of one way to  
2 implement the (DC) EXTEST capability.



3 **Figure 33: Timing of level-detection initialization and data capture in a test receiver.**

4 **6.1.3 Edge Detection Behavior of Input Test Receivers**

5 The edge detection behavior is selected by the AC\_EXTEST instruction provided by this  
6 standard.

7 **6.1.3.1 Rules**

- 8 a) Whenever a test receiver is operating in edge-detection mode on an AC input pin, it shall  
9 determine the magnitude of input signal change by one of two methods:
- 10 i. by comparing the instantaneous voltage on the pin to the recent average of the  
11 voltage on the pin, determined by a method equivalent to that given in  
12 recommendation 6.1.3.2b)
  - 13 ii. if a device input *is guaranteed* to be AC coupled to its driver, by comparing  
14 the instantaneous voltage on the pin to a fixed threshold voltage.

15 NOTE 1 – Even when method ii is permitted, method i may still be exercised.

16 NOTE 2 – The opportunity to implement method ii clearly exists in the case where the AC coupling is  
17 implemented on-chip. It may also apply to a device not containing AC coupling when the device designer  
18 assures that in all applications the input will be AC coupled at the board or system level.

19 NOTE 3 – When adopting method ii, the device designer may choose a threshold value at the midpoint of a  
20 voltage swing deemed optimal for the mission receiver. This may be the same voltage used to bias the  
21 mission receiver when it is AC coupled as seen in Figure 12 (page 17).

22 NOTE 4 – If method ii is adopted, then rule b) below must be interpreted as defining hysteresis centered at  
23 the fixed threshold voltage.

- 24 b) Whenever a test receiver is operating in edge-detection mode on an AC test input pin, the  
25 test receiver shall respond only to transitions having a magnitude greater than the  
26 hysteresis voltage  $V_{\text{Hyst\_Edge}}$ , where  $V_{\text{Hyst\_Edge}}$  is a fraction no less than 50% of  $\Delta V_{\text{Min}}$  and  
27 no greater than 90% of  $\Delta V_{\text{Min}}$ .

28 NOTE – See rules d) and e) below for further definition of the meaning of the word “respond.”

- 1 c) Whenever a test receiver is operating in edge-detection mode on an AC input pin, the test  
2 receiver shall respond to valid signal transitions defined in rule 6.1.1.1b) only when the  
3 new signal level persists for at least a minimum period of time called the *hysteresis delay*  
4 ( $T_{Hyst}$ ) and this delay period shall be chosen by the designer by considering recom-  
5 mendation 6.1.2.3a).

6 NOTE – There may also be a propagation delay in the test receiver. This time is not included in the value  
7 of the hysteresis delay. This delay should be small compared to the value of  $T_{LP}$  given in rule g) below.

- 8 d) In response to a valid signal transition as defined in rules b) and c) above, the test  
9 receiver shall output a logic one when the signal transition is a rising or a logic zero when  
10 the signal transition is falling, and it shall retain that logic value until the next valid  
11 transition occurs.

- 12 e) If a test receiver has not received a valid signal transition as defined in rules b) and c)  
13 above, it shall produce a default output of either a logic one or logic zero.

**Editor's note:** The treatment of “default output” is yet incomplete, as it is dependent on how we implement the signaling protocol. One approach appears in Figure 27 (page 30). Upon first entering into edge-detection mode, the hysteretic memory should be set (as this rule suggests) to a deterministic value. Whether this initialization is the only one performed or whether there may be other initializing events is still to be determined.

- 14 f) When an AC input pin is AC coupled to a driver, the time constant ( $T_{HP}$ ) of the effective  
15 high-pass filtering of the coupling shall be no less than  $HP\_Mult$  times the value of the  
16 hysteresis delay  $T_{Hyst}$ , where  $HP\_Mult$  is chosen per rule i) below.

- 17 g) When method i of rule a) above has been exercised, the time constant ( $T_{LP}$ ) of the low-  
18 pass filter given in recommendation 6.1.3.2b) shall be no less than  $LP\_Mult$  times the  
19 value of the hysteresis delay  $T_{Hyst}$ , where  $LP\_Mult$  is chosen via rule i) below.

20 NOTE – When method ii rather than method i of rule a) is exercised, this rule is unnecessary since recent  
21 signal history is not used as a reference.

- 22 h) When rules f) and g) above have been exercised, the value of  $T_{HP}$  shall be no less than  
23  $HPLP\_Ratio$  times the value of  $T_{LP}$ , where  $HPLP\_Ratio$  is chosen from Table 2 (page  
24 47).

- 25 i) The choice of  $HP\_Mult$  and (if needed)  $LP\_Mult$  are found by selecting values from  
26 Table 3 (page 48) for the value of  $V_{Hyst\_Edge}$  closest to or higher than the value used in the  
27 design.

28 NOTE – No value of  $LP\_Mult$  is needed when method ii rather than method i of rule a) is exercised.

- 29 j) When method i of rule a) above has been exercised, tools that perform tests shall assure,  
30 when the AC EXTEST instruction is in effect in any IC participating in those tests, that  
31 the time between subsequent test data changes ( $T_{Test}$ ) is no less than 3 (three) times the  
32 low-pass filter time constant ( $T_{LP}$ ) of any IC.

33 NOTE – When method ii rather than method i of rule a) is exercised, this rule is unnecessary since recent  
34 signal history is not used as a reference.

### 35 6.1.3.2 Recommendations

- 36 a) For better small-amplitude noise immunity, the value of  $V_{Hyst\_Edge}$  selected per rule  
37 6.1.3.1b) should be set closer to the high limit.

38 NOTE – Proper accounting for process variations that may affect the value of this threshold should be  
39 observed to stay within the limits given in rule 6.1.3.1b).

- 40 b) The “recent average” of a signal may be generated with a simple low-pass filter.

41 NOTE 1 – See Figure 26 (page 28) for an example of this filter.

1 NOTE 2 – See rule 6.1.3.1g) above for the time constant determination for this low-pass filter.

### 2 6.1.3.3 Description

3 Rule 6.1.3.1a) specifies two methods for detecting edges, the first by comparing the instantaneous  
4 value of the signal against its recent history. See Figure 26 (page 28) for an example of one way  
5 to do this comparison. The second method allows the comparison to be done versus a fixed  
6 reference, when the signal is guaranteed to be AC coupled. This can be the case where the  
7 coupling is integrated into the device. A designer is not required to use this second method, but  
8 may find it useful to reuse a portion of the circuitry needed for level-detection (see rule 6.1.2.1a)).  
9 In such cases, the values of  $V_{\text{Hyst\_Level}}$  and  $V_{\text{Hyst\_Edge}}$  may be equivalent.

10 Rule 6.1.3.1b) defines the range for the hysteresis voltage  $V_{\text{Hyst\_Edge}}$  between 50% and 90% as the  
11 target for a designer to set a trip point value for test receiver response and allows for significant  
12 margin. See recommendation 6.1.3.2a). See also rule 6.1.3.1i), which uses this value to determine  
13 bounds on time constants.

14 Rule 6.1.3.1c) defines the hysteresis delay  $T_{\text{Hyst}}$  used to provide noise rejection. If a signal change  
15 does not persist long enough (for example, it is a short noise pulse) the hysteresis delay will  
16 suppress the test receiver's response to it. This gives the test receiver two methods for ignoring  
17 noise. The hysteresis voltage will ignore small-amplitude noise and the hysteresis delay will  
18 ignore large-amplitude pulses of insufficient duration. See section 6.1.3.4 for a discussion of how  
19 hysteresis delay may be controlled within an implementation.

20 Rule 6.1.3.1g) governs the low-pass time constant (or equivalent) that is used to establish the  
21 recent average value of a signal. The low-pass filter time constant is set large enough to assure  
22 that the recent history of the average input voltage is not unduly influenced by the rise time of the  
23 signal itself and small enough to settle before a new test-induced transition arrives.

24 Rules 6.1.3.1d) and e) specify the behavior of the test receiver when transitions occur or do not  
25 occur. When no transitions have been received, the hysteretic memory of the test receiver will  
26 retain a default initial value.

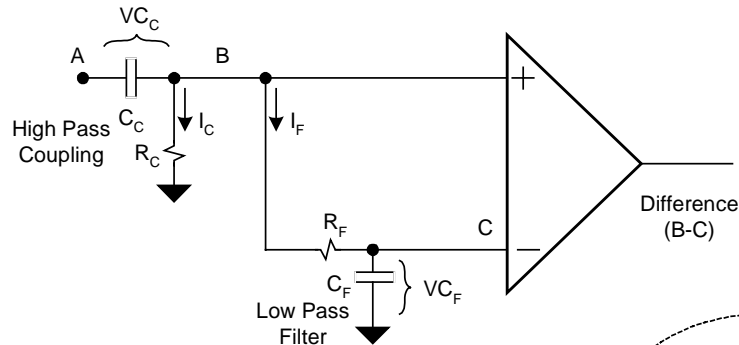
**Editor's note:** This treatment of "default initial value" is yet incomplete, as it is dependent on how we implement the signaling protocol.

27 Rule 6.1.3.1f) specifies the minimum value for the high-pass time constant when AC coupling is  
28 used. An upstream driver is expected to produce edges that are equal to or faster than the  
29 minimum input swing  $\Delta V_{\text{Min}}$  within a maximum time  $T_{\text{Trans}}$ , given an acceptable level of AC  
30 attenuation in the channel. These edges will pass through this high-pass coupling virtually  
31 unchanged. This rule assures the subsequent decay will be much slower than a valid signal edge  
32 so it will not be confused with a valid signal transition, as depicted in Figure 31 (page 37).

33 When the high-pass AC coupling is implemented on a board rather than inside an IC, the IC  
34 designer shall communicate to the board designer this minimum time constant required for AC  
35 coupling. In a 50 ohm load termination environment, the minimum value of capacitance specified  
36 by this rule might be 1000 picofarads. If the same time constant were implemented on-chip, then  
37 the resistive component would likely be determined by a biasing network and the capacitance  
38 could be much smaller, for example 10 Kohms and 5 picofarads, which are both amenable to on-  
39 chip integration.

40 In rule 6.1.3.1g), the value of HPLP\_Ratio is a function of the ratio of the minimum input swing  
41 from rule 6.1.1.1b) to the maximum input swing from rule 6.1.1.1c), times the  $V_{\text{Hyst\_Edge}}$  fraction.  
42 Values of HPLP\_Ratio closer to one (1) yield poorer noise immunity. Ratios much larger than

- 1 one (1) have higher value for noise immunity but force larger values of resistor/capacitor  
2 combinations in the coupling network.
- 3 Rule 6.1.3.1j) governs the behavior of tools that perform tests, assuring that transitions caused by  
4 a tool do not occur too close together in time. This rule assures that the recent history of a signal  
5 is not influenced by the recent history of the test.
- 6 Given a model of the basic test receiver circuit that uses high-pass coupling and low-pass filtering  
7 to generate a self-referenced edge detector (one half shown in Figure 34) the effects of the rules  
8 given in section 6.1.3 are plotted in Figure 35 for a single rising edge transition.



Voltage at A:  $V_A = \text{Input Stimulus}$

Voltage at B:  $V_B = V_A - V_{C_C}$

Current through  $R_C$ :  $I_C = V_B / R_C$

Current through  $R_F$ :  $I_F = (V_B - V_{C_F}) / R_F$

Voltage across  $C_C$ :  $V_{C_C} = (I_C + I_F) \cdot \Delta t / C_C + V_{C_C}$

Voltage across  $C_F$ :  $V_{C_F} = I_F \cdot \Delta t / C_F + V_{C_F}$

Time t+1

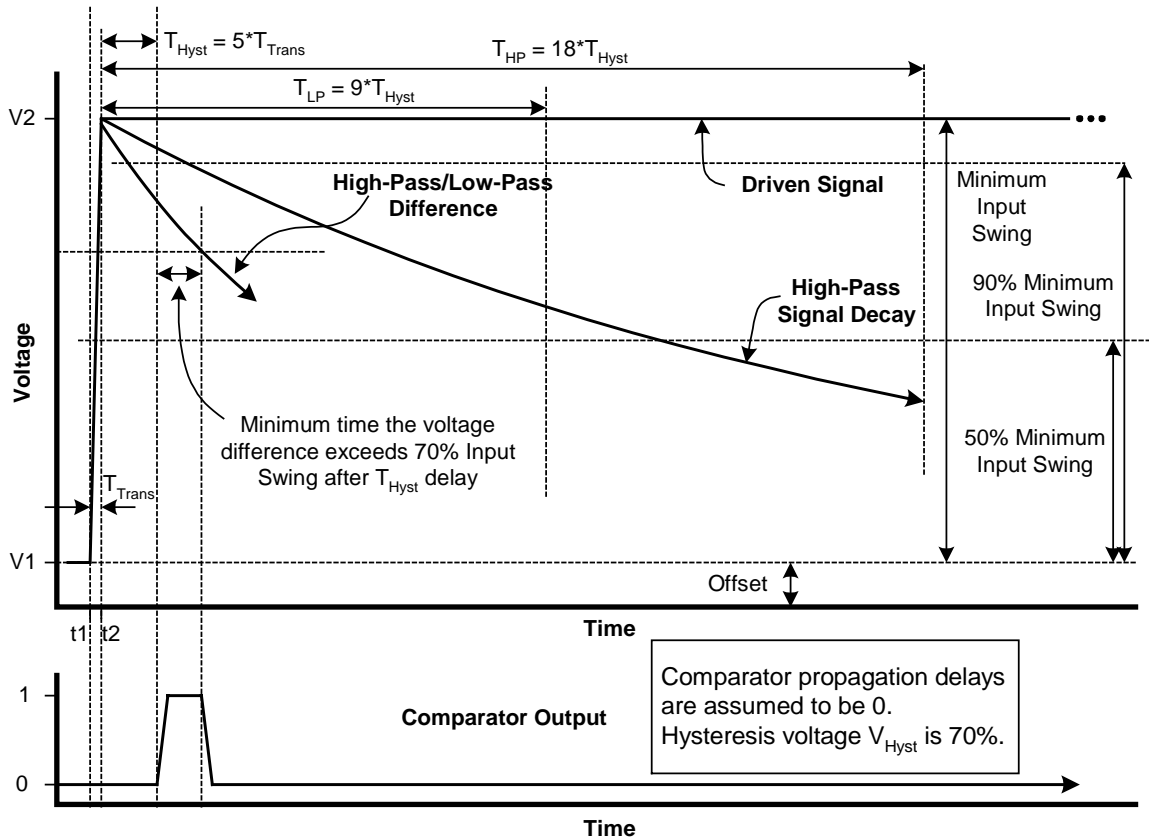
Time t

9 **Figure 34: Model with recurrence equations for a portion of test receiver circuitry. The comparator**  
10 **has hysteresis delay. The hysteresis voltage has been omitted in this figure and subsequent analysis.**

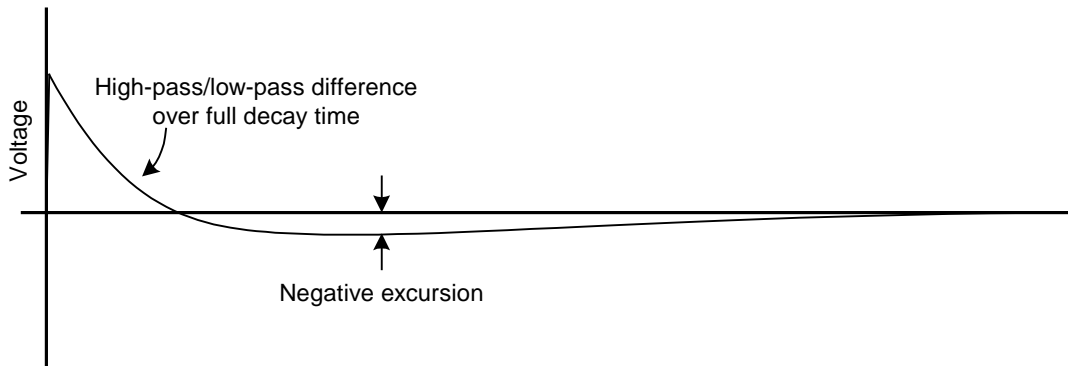
11 Figure 35 shows the output of the non-hysteretic comparator in Figure 34 to illustrate the effects  
12 of the selected time constants and offsets for a single rising edge, on that portion of circuitry  
13 devoted to detecting a rising edge. Rule 6.1.3.1b) gives the two horizontal lines for 50% and 90%  
14 input voltage swings. This example uses hysteresis voltage  $V_{\text{Hyst\_Edge}}$  at 70% of the minimum  
15 input swing. Given a signal with a valid rising edge with rise time  $T_{\text{Trans}}$  the output of the high-  
16 pass filter will decay as shown. There must be, by rule 6.1.3.1c), a hysteresis delay  $T_{\text{Hyst}}$  where  
17 the comparator does not respond. The time constant  $T_{\text{HP}}$  of decay due to the high-pass filter, by  
18 rule 6.1.3.1f) must be no less than 18 times (in this example) the value of  $T_{\text{Hyst}}$ . However, the  
19 decay of the difference signal is faster as shown, due to the low pass filtering set to no less than 9  
20 times the value of  $T_{\text{Hyst}}$  by rule 6.1.3.1g). The choice of multipliers (9 and 18, from Table 3)  
21 assure that the minimum time that the voltage difference exceeds 70% of the minimum input  
22 swing is significantly greater than the hysteresis delay. If the either or both multipliers are  
23 increased, this minimum time will increase. If the hysteresis voltage is decreased from 70%, the  
24 minimum time will increase. Finally, if the circuit is DC coupled (equivalent to an infinite  
25 coupling time constant) the minimum time will increase.

26 Rule 6.1.3.1h) controls the ratio of high-pass to low-pass time constants via the content of Table 2  
27 below. The ratio is selected by first determining the ratio of driven signals the receiver is prepared  
28 to accept,  $\Delta V_{\text{Min}} / \Delta V_{\text{Max}}$  and using this ratio to de-rate  $V_{\text{Hyst\_Edge}}$ . The comparator takes the  
29 difference of the high-pass filtered and low-pass filtered signals, and after much of the transition  
30 effect has decayed, this difference can drop below zero. (This is seen in Figure 36, which depicts  
31 a complete transition and decay cycle.) When a larger signal is applied, this multiplies the  
32 negative excursion. In order to prevent this negative excursion from re-triggering the test receiver

- 1 in the negative direction, the high-pass and low-pass time constants are adjusted to prevent this.
- 2 As the ratio of these two constants gets larger, the negative excursion is reduced. In the extreme
- 3 case of an infinite ratio (DC coupling) there is no negative excursion.



4 **Figure 35: Relationships of key delay times and time constants given by rules in section 6.1.3.1 for the**  
5 **detection of a rising edge. Here the value of  $V_{Hyst}$  has been set to 70% of the minimum input swing.**



6 **Figure 36: High-pass/low-pass difference signal over the full decay time.**

1 **Table 2: Values of multiplier HPLP\_Ratio versus  $V_{Hyst\_Edge}$  times the voltage ratio  $\Delta V_{Min}$  over  $\Delta V_{Max}$ .**

$V_{Hyst\_Edge} * (\Delta V_{Min}/\Delta V_{Max})$	HPLP_Ratio	Comments
> 0.13	2	12.5% actual over/undershoot (worst case)
Between 0.13 and 0.10	4	9.9%
Between 0.10 and 0.09	6	8.2%
Between 0.09 and 0.07	8	6.9%
Between 0.07 and 0.06	12	5.8%
Between 0.06 and 0.05	16	4.3%
< 0.05	32	2.5%

2 Rule 6.1.3.1i) selects minimum values for HP\_Mult and LP\_Mult (from Table 3 below) which  
3 determine high-pass and low-pass time constants. This is consistent with rule 6.1.3.1h) which  
4 may have the effect of raising HP\_Mult above the minimum value.

5 **Table 3: Values of multipliers HP\_Mult and LP\_Mult for selected values of hysteresis voltage  $V_{Hyst}$ .**

$V_{Hyst}$ % $\Delta V_{Min}$	HP_Mult	LP_Mult	Comments
50%	10	5	Lowest small signal noise immunity for positive noise events. Highest small signal noise immunity for negative noise events. Gives smallest values for on-chip filter components.
60%	12	6	
70%	18	9	Best small signal noise immunity for general noise events.
80%	30	15	
90%	75	37	Highest small signal noise immunity for positive noise events. Lowest small signal noise immunity for negative noise events. Gives highest values for on-chip filter components.

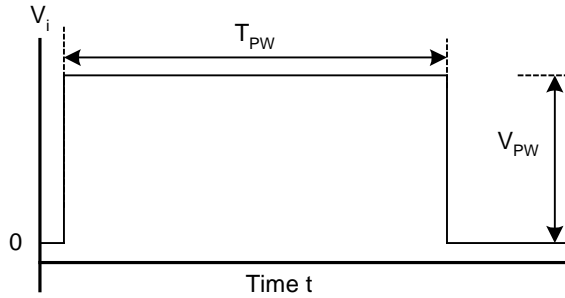
6

7 **6.1.3.4 Noise Rejection in the Edge-Detecting Mode**

8 The hysteresis delay  $T_{Hyst}$  used to provide noise rejection during edge-detection mode. The  
9 hysteresis voltage setting will reject a noise pulse with small amplitude. But if a noise pulse with  
10 amplitude greater than the hysteresis voltage is encountered, the test receiver is expected to reject  
11 those with duration less than  $T_{Hyst}$ . There are two techniques that can be utilized separately or in  
12 combination to accomplish this. (Other techniques may also be applied to achieve this result.)  
13 These techniques are *bandwidth limitation* and *slew rate limitation*.

14 **6.1.3.4.1 Noise Rejection by Bandwidth Limitation**

15 Bandwidth limitation can be added to the test receiver to limit its response time. Consider a  
16 rectangular pulse waveform of height  $V_{PW}$  and pulse width duration  $T_{PW}$ , where  $V_{PW}$  is greater  
17 than the hysteresis voltage. (See Figure 37.) For analysis purposes, assume that the lower  
18 amplitude of the pulse is at 0 volts, although the results are applicable to the general case of an  
19 arbitrary baseline voltage. Furthermore, assume the rise and fall times of the pulse are much  
20 faster than the those of the test receiver input stage so they can be ignored in this analysis, but the  
21 test receiver input stage is adequately fast enough to track the pulse itself.



1 **Figure 37: Pulse input to test receiver.**

2 The test receiver can be modeled in the small-signal domain as a single-pole low-pass amplifier  
 3 with a frequency response (as designated by the lowercase nomenclature) given in Figure 38  
 4 where  $v_o$  and  $v_i$  are the output and input voltages of the amplifier and  $A_0$  is its DC gain. Let  
 5  $\tau_{BW} = 1/2\pi f_{BW}$  be the time constant of the bandwidth frequency,  $f_{BW}$  and  $s$  be the complex identity  
 6  $j\omega$ .

$$\frac{v_o}{v_i} = \frac{A_0}{1 + s \tau_{BW}}$$

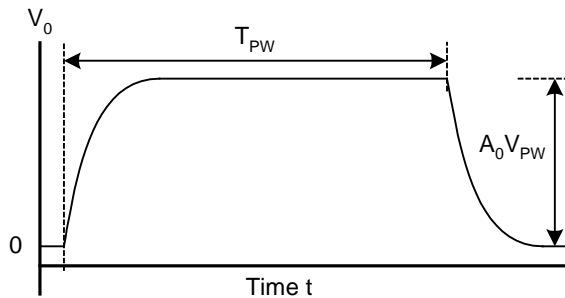
7 **Equation 1: Frequency response of a simple single-pole low-pass amplifier.**

8 Furthermore, assume that the test receiver has an input referred switching threshold of  $V_{TH}$ . The  
 9 input voltage must exceed  $V_{TH}$  for a sufficient period of time to cause the test receiver to switch  
 10 its output state. In the time domain (as designated by the upper case nomenclature) the output  
 11 response of the test receiver will be described by Equation 2 which is shown in Figure 38 for  
 12  $T_{PW} \gg \tau_{BW}$ .

13 NOTE – The propagation delay through the test receiver has been ignored.

$$\frac{V_o}{V_i} = A_0(1 - \exp(-t / \tau_{BW}))$$

14 **Equation 2: Time domain output response of the test receiver.**



15 **Figure 38: Output response of the test receiver to the rectangular pulse.**

16 The output amplitude for an arbitrary input can be obtained by solving Equation 2 as

$$t = -\tau_{BW} \ln \left\{ 1 - \left( \frac{V_o}{V_i A_0} \right) \right\}.$$

17 **Equation 3: Solution of Equation 2 for time t.**

18 In order to for the receiver circuitry to switch the input amplitude will have to exceed the input  
 19 referred switching threshold for a period of time long enough to allow the output level to reach

1 the output referred switching threshold,  $A_o V_{TH}$ . Thus, the input pulse must persist for a minimum  
2 period of time,  $T_{TH}$ . This time can be calculated from Equation 3 as

$$T_{TH} = -\tau_{BW} \ln \left\{ 1 - \left( \frac{V_{TH}}{V_{PW}} \right) \right\}$$

3 **Equation 4: Minimum pulse width duration.**

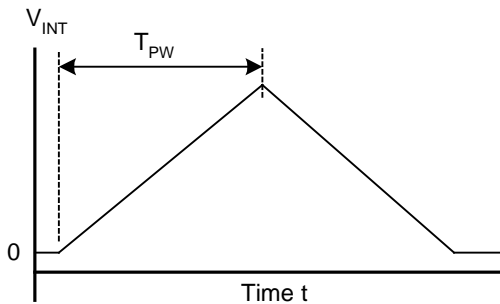
4 If the pulse width is less than the minimum time,  $T_{TH}$ , then the pulse will be rejected. Alternately,  
5 the pulse will be rejected if the bandwidth of the receiver circuit is

$$f_{BW} < -\frac{1}{2\pi T_{PW}} \ln \left\{ 1 - \left( \frac{V_{TH}}{V_{PW}} \right) \right\}$$

6 **Equation 5: Test receiver bandwidth specification.**

7 6.1.3.4.2 Noise Rejection by Slew Rate Limitation

8 In most situations the switching of the test receiver will be limited more by its large signal and  
9 internal slew capability rather than its small signal bandwidth. This is manifested by the limited  
10 rate at which an arbitrary internal node of the receiver can transition due to its capacitive load  
11 and/or limited current drive capability. Hence, at this internal node of the test receiver circuitry,  
12 the voltage  $V_{INT}$  will be limited by its slew rate  $SR$ , as depicted in Figure 39.



13 **Figure 39: Slew rate limited response of a control node internal to the test receiver.**

14 It is assumed that the duration of the input signal is not long enough to allow the internal node  
15 voltage to achieve its final value for the given level of input signal before the direction of the  
16 voltage transition reverses as the result of the reversal of the input signal. In order for the circuit  
17 to switch the voltage at the internal node, it will have to achieve a level equal to its internal  
18 switching threshold  $V_{THINT}$ . This situation can be expressed as the switching condition

$$V_{INT} = SR \cdot T_{PW} > V_{THINT}$$

19 or

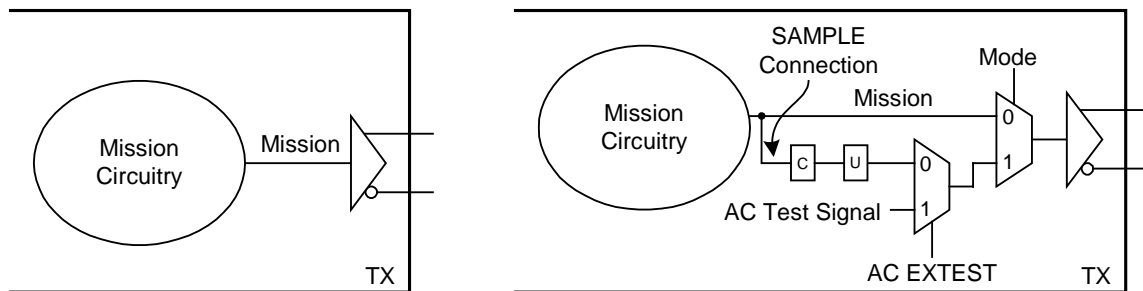
$$T_{PW} > \frac{V_{THINT}}{SR}$$

20 If the duration of the input pulse does not meet the criteria set forth in this equation, it will be  
21 rejected.

## 22 **6.2 Output Drivers**

23 All AC pins (see 4.1) that drive data from an IC are equipped with test circuitry that allows  
24 Boundary-Scan test instructions to co-opt the mission driver and substitute test signals in place of

1 mission data. The goal is to use the mission driver with its *native drive levels* and *edge rate* to  
2 produce test signals (as defined in section 6.1). This is conceptualized in Figure 40 for a  
3 differential mission driver, but the concept is identical for single-ended drivers.



4 **Figure 40: A mission driver (differential) and added test circuitry.**

5 The actual implementation may be different, since adding a multiplexer (as shown) in the mission  
6 signal path may introduce an unacceptable delay, but the effect is the same as shown. The test  
7 circuitry used to implement the functionality is not required to perform at the frequencies of the  
8 mission, except with respect to voltage levels and edge rates seen at the pin(s). The time between  
9 test edges will likely be much larger than for mission edges.

**Editor’s Note:** The ‘AC TEST Signal’ shown in Figure 40 is a function of the signaling protocol still to be decided.

10 The mission circuitry may be digital or analog. If digital, it could operate at extremely high  
11 frequencies so as to have ‘analog’ properties. In many cases, the signal states captured via the  
12 ‘SAMPLE connection’ to the Boundary-Scan capture flip-flop may be indeterminate. This is  
13 especially true in cases where the TCK rate is much lower than the performance of the mission  
14 circuitry. Thus this standard allows the relaxation of the requirement from IEEE 1149.1 to  
15 implement the SAMPLE instruction for AC output pins – the SAMPLE instruction must be  
16 implemented, but the SAMPLE connection shown may be omitted and replaced with a default  
17 value. If the mission of the device *is* a candidate for use with the SAMPLE instruction, then  
18 SAMPLE functionality should be implemented.

19 NOTE – The SAMPLE instruction must be implemented on DC pins and all inputs.

## 20 6.2.1 AC Pin Driver Behavior for IEEE Std 1149.1 Test Instructions

21 Test mode instructions from IEEE Std 1149.1 include EXTEST and CLAMP, and within options  
22 contained within IEEE Std 1149.1, the RUNBIST and INTEST instructions may also provide  
23 data to the driver, when they do not disable all drivers. The HIGHZ instruction always disables  
24 drivers. The rules below assume there is an appropriate load or termination available to allow a  
25 driver to operate as specified for its mission mode when enabled.

26 Non-test mode instructions (e.g., SAMPLE, PRELOAD, BYPASS, IDCODE, USERCODE) do  
27 not interfere with the mission performance of the driver.

### 28 6.2.1.1 Rules

- 29 a) The single-ended (or differential) driver for an AC output pin (or channel) shall be  
30 provided with data by a single associated Boundary-Scan register cell.
- 31 b) When in test mode, an enabled output driver of an AC output pin (channel) shall produce  
32 on its output(s) a static value that matches the value stored in the Update flip-flop of the  
33 associated Boundary-Scan register cell.

1 NOTE 1 – In the case of a differential driver driving a channel, one output pin will track the polarity of the  
2 data and the other pin will be the complement of this data.

3 NOTE 2 – Depending on if permission 6.2.1.2a) is implemented, the pin or channel may always be  
4 enabled.

5 c) When in test mode, an enabled output driver of an AC output pin (channel) shall produce  
6 on its output(s) a transition matching the levels and edge rate of the mission performance  
7 specified for the driver, when the content of the Update flip-flop of the associated  
8 Boundary-Scan register cell changes.

9 d) When in test mode, a disabled output driver of an AC output pin (channel) shall produce  
10 on its output(s) a quiescent, non-driven state.

11 NOTE 1 – There may be biasing supplied in the driver implementation that establishes a state as perceived  
12 by a downstream receiver, but this state is at most weakly driven. It is expected that if another enabled  
13 driver shared this channel, it would be unaffected by this weak state.

14 NOTE 2 – A driver may be disabled (see permission 6.2.1.2a)) by a control cell, or by an instruction such  
15 as RUNBIST, INTEST or HIGHZ.

**Editor's Note:** I see a subtle problem here to be wary of. If a driver performing EXTEST is connected to a downstream test receiver performing AC EXTEST, *and* the driver transitions from disabled to enabled states, this may not produce a suitable transition for the edge-detector to see. I have not contemplated the implications (if any) on test algorithms. Note the signal protocol (e.g. 'throat-clearing') may eliminate this problem.

#### 16 6.2.1.2 Permissions

17 a) The single-ended (or differential) driver for an AC output pin (or channel) may be  
18 disabled or enabled via the content of a control cell in the Boundary-Scan register, per the  
19 rules within IEEE Std 1149.1.

20 b) With respect to the SAMPLE instruction, the device designer may opt to have the  
21 Capture flip-flop load a deterministic value rather than attempt to sample the state of the  
22 mission circuitry on the rising edge of TCK in the Capture-DR TAP controller state.

#### 23 6.2.1.3 Recommendations

24 a) When the mission circuitry is digital, or is capable of slower digital performance, the  
25 designer should implement the SAMPLE instruction behavior per IEEE Std 1149.1.

#### 26 6.2.1.4 Description

27 For AC pins only, permission 6.2.1.2b) allows a device designer to opt out of the requirement by  
28 IEEE Std 1149.1 that mandates capturing the digital state of the mission circuitry on the rising  
29 edge of TCK in the Capture-DR TAP controller state while executing the SAMPLE instruction,  
30 since there are cases where this signal is analog in nature, or if digital, it is changing so fast so as  
31 to make sampling at the much slower TCK rate meaningless. If, when SAMPLE is loaded, the  
32 mission can be suitably observed (e.g. there is a single-cycle mode) then the designer should  
33 implement SAMPLE as recommended in 6.2.1.3a).

### 34 6.2.2 AC Pin Driver Behavior for Test Instructions Provided by This Standard

35 This standard provides one new instruction, AC\_EXTEST. This instruction is a test mode  
36 instruction and uses the same Boundary-Scan register cells already specified for the IEEE Std  
37 1149.1 instructions, that is, the mapping of data and control cells does not change.

1 **6.2.2.1 Rules**

2 a) The single-ended (or differential) driver for an AC output pin (or channel) shall be  
3 provided with data by a single associated Boundary-Scan register cell, and that cell shall  
4 be the same required by rule 6.2.1.1a).

5 b) When in test mode, an enabled output driver of an AC output pin (channel) shall produce  
6 on its output(s) a waveform matching that of the AC Test Signal.

7 NOTE 1 – In the case of a differential driver driving a channel, the positive output pin will track the  
8 polarity of the waveform and the negative output pin will be the complement of this waveform.

9 NOTE 2 – Depending on if permission 6.2.1.2a) is implemented, the pin or channel may always be  
10 enabled.

11 c) When in test mode, an enabled output driver of an AC output pin (channel) shall produce  
12 on its output(s) transition(s) matching the levels and edge rate of the mission performance  
13 specified for the driver, matching the waveform of the AC Test Signal.

14 d) When in test mode, a disabled output driver of an AC output pin (channel) shall produce  
15 on its output(s) a quiescent, non-driven state.

16 NOTE 1 – There may be biasing supplied in the driver implementation that establishes a state as perceived  
17 by a downstream receiver, but this state is at most weakly driven. It is expected that if another enabled  
18 driver shared this channel, it would be unaffected by this weak state.

19 NOTE 2 – A driver may be disabled (see permission 6.2.1.2a)) by a control cell.

20 **6.2.2.2 Description**

21 When the AC\_EXTEST instruction is in effect, an enabled AC pin driver will produce the AC  
22 Test Signal waveform (or its complement on the negative leg of differential pair) with the native  
23 voltage range and edge rate of the driver produces in mission mode.

24 **6.2.3 The AC Test Signal**

25 [Depends on the protocol selected. It could be as simple as the content of the Update FF (single  
26 edge encoding), a “precede with complement” waveform (throat clearing) or a stream of edges  
27 (phase or frequency-based), etc.]

# 1 7 Conformance and Documentation 2 Requirements

## 3 **7.1 Conformance**

### 4 7.1.1 Specification

#### 5 Rules

6 a) A component conforming to this standard shall comply with all rules set out herein.

7 NOTE – Due to rule XXX, this also implies conformance with the rules set out in IEEE Std 1149.1.

### 8 7.1.2 Description

9 Conformance to the rules set out herein and in IEEE Std 1149.1 are essential for testing boards  
10 and other assemblies containing both DC and AC coupled interconnections, allowing  
11 manufacturing defects such as shorted or open solder joints to be found and repaired before  
12 shipment. Conformance allows:

- 13 ▪ IC vendors to provide testability features in a standardized way, so that each new IC design  
14 does not need new engineering investment to provide testability.
- 15 ▪ makers of Automatic Test Equipment to develop and continually refine standardized tools for  
16 the automation of test development, test execution and diagnosis of failures.
- 17 ▪ end-users to strategize and develop test methodologies in a standardized way, making full use  
18 of the automation provided by tools, to allow them to produce very large and complex boards  
19 and system more rapidly and efficiently.

## 20 **7.2 Documentation**

21 Because adherence to this standard implies adherence to IEEE Std 1149.1, all ISC devices shall  
22 have a description supplied in Boundary-Scan Description Language (BSDL) provided with IEEE  
23 Std 1149.1b-1994.

### 24 7.2.1 Specification

#### 25 Rules

26 a) A component conforming to this standard shall be documented with a Boundary-Scan  
27 Description Language (BSDL) description.

28 NOTE – See IEEE Std 1149.1b-1994 for a description of IEEE BSDL. The precursor to IEEE BSDL  
29 developed in 1990 cannot be used for documentation because it does not support the concept of “BSDL  
30 Extensions”.

31 b) A component shall have the AC\_EXTEST instruction and register relationship and  
32 optional provisions documented via the syntax provided by BSDL and the BSDL  
33 extension provided by this standard.

34 NOTE – New BSDL syntax (contained within a “BSDL extension”) for describing concepts and structures  
35 introduced by this standard are given in 7.4. A BSDL extension is a mechanism provided by IEEE Std  
36 1149.1b-1994 (see “User extensions to BSDL”) which allows proprietary syntax to be provided that will  
37 allow tools to work that are unaware of this syntax.

1 c) Other properties of a device not described in BSDL shall be documented by the  
2 manufacturer.

3 NOTE – For example, this includes TAP signal voltage level requirements, and any additional power  
4 requirements of the device.

## 5 7.2.2 Description

6 Consider a device with a full set of 1149.1 instructions and registers as well as the new  
7 AC\_EXTEST instruction. Here are fragments of BSDL needed to document this device.

8 First, for devices that have AC differential outputs, a “Port\_Grouping” attribute must be given  
9 that identifies the positive and negative legs. Notice that because the implementation of  
10 AC\_EXTEST requires single-ended receivers for differential input pin pairs, the test behavior of  
11 these pins is single-ended and thus should not be included in a port grouping description. (An  
12 error would result during compilation.) For example, for a device with four pairs of differential  
13 data drivers, the Port\_Grouping could be:

```
14 Attribute PORT_GROUPING of ACDEV:entity is  
15     "Differential_Voltage ( "  
16         " (D(1), Dbar(1)), "  
17         " (D(2), Dbar(2)), "  
18         " (D(3), Dbar(3)), "  
19         " (D(4), Dbar(4)) )";  
20
```

21 NOTE 1 – Refer to IEEE Std 1149.1b-1994, section B.8.8, titled “Grouped Port Identification”, for precise  
22 information regarding the Port\_Grouping attribute.

23 NOTE 2 – The entity name in these examples is shown as “ACDEV”. This would be replaced with a name  
24 unique to the device.

25 Since AC coupled circuits cannot transmit current, the “Differential\_Voltage” BSDL keyword is  
26 used rather than “Differential\_Current”.

27 At a board or system level, differential pairs are interconnected with pair-wise wiring or AC  
28 blocking capacitors. With the information from the port grouping attribute, software can trace the  
29 pathways of the positive and negative legs of each pair starting at the drivers. Thus, though the  
30 receivers are not identified as differential, their differential relationship can be discovered via this  
31 tracing exercise.

32 Next, an “Instruction\_Opcode” attribute used to define instruction names and binary code  
33 assignments should be given:

```
34  
35 Attribute INSTRUCTION_OPCODE of ACDEV:entity is  
36     "BYPASS (111111), " &  
37     "EXTEST (000000), " &  
38     "SAMPLE (000001), " &  
39     "IDCODE (010001), " &  
40     "USERCODE (010010), " &  
41     "AC_EXTEST (000010) ";  
42
```

43 NOTE – Refer to IEEE Std 1149.1b-1994, section B.8.11, titled “Instruction Register Description”, for  
44 precise information regarding the Instruction\_Opcode attribute.

45 Later, a Register\_Access attribute is given:

```
46  
47 Attribute REGISTER_ACCESS of ACDEV:entity is  
48     "Boundary (AC_EXTEST)";
```

1  
2 The Register\_Access attribute defines the existence of optional registers, their length, the  
3 instruction(s) that target them, and any consistent capture data they may be loaded with in the  
4 *Capture-DR* TAP Controller state. The above attribute documents the fact that AC\_EXTEST  
5 targets the Boundary Register.

6 NOTE 1 – Refer to IEEE Std 1149.1b-1994, section B.8.13, titled “Register Access Description”, for  
7 precise information regarding the Register\_Access attribute.

8 NOTE 2 – This attribute may also (though redundantly) document the associations of EXTEST, SAMPLE,  
9 BYPASS, USERCODE and IDCODE as well. This was omitted here.

### 10 **7.3 BSDL Extension for AC\_EXTEST Description (STD\_xxxx\_yyyy)**

11 The information provided above in 7.2 showed how to document features of a device  
12 implementing AC\_EXTEST using the existing syntax of BSDL. This information is incomplete.  
13 BSDL has been defined (see IEEE Std 1149.1b-1994) to be extensible using a mechanism called  
14 a “BSDL Extension”. A BSDL Extension for describing additional features of AC\_EXTEST  
15 devices is given here.

16 NOTE – Refer to IEEE Std 1149.1b-1994, section B.8.17, titled “User extensions to BSDL”, for precise  
17 information regarding BSDL extensions.

18 The extension mechanism chosen for describing devices is based on the definition of a VHDL  
19 package with the name “STD\_xxxx\_yyyy” which contains the definitions of attributes that will  
20 be used to supply relevant data. Therefore, an compliant device BSDL will contain an additional  
21 “use” statement appearing just after the “standard use statement” as in this excerpt of a BSDL  
22 file:

```
23  
24     ...  
25     use STD_1149_1_1994.all;      -- Standard 'use' statement  
26     use STD_xxxx_yyyy.all;      -- BSDL Extension for AC_EXTEST  
27     ...
```

28  
29 NOTE – Refer to IEEE Std 1149.1b-1994, section B.8.5, titled “Use Statement”, for precise information  
30 regarding references to additional packages.

31 Utilization of the extension mechanism of BSDL guarantees that AC\_EXTEST information can  
32 be supplied to applications that are cognizant of this functionality without hindering other  
33 applications that may not be aware of this functionality. Non-cognizant applications will simply  
34 ignore the extension.

35 The VHDL package STD\_xxxx\_yyyy contains the definition of additional attributes used to  
36 complete the description of the ISC features of a device. The content of this VHDL package is  
37 given here.

38 Syntax

```
39  
40     Package STD_xxxx_yyyy is      -- Attribute definitions for AC_EXTEST  
41     description  
42         use STD_1149_1_1994.all;  -- Refer to BSDL definitions  
43  
44         attribute AC_EXTEST_Pin_Behavior:    BSDL_Extension;  
45         attribute AC_EXTEST_Frequency_Ref:   BSDL_Extension;  
46     end STD_xxxx_yyyy;  
47  
48     Package Body STD_xxxx_yyyy is
```

```
1      -- No content, this package body is required by BSDL syntax
2      end STD_xxxx_yyyy;
```

3  
4 This VHDL package is “read-only” and may be maintained within a given system in the same  
5 location as the standard package STD\_1149\_1\_1994.

## 6 **7.4 BSDL Extension Structure**

7 The following sections define the syntax and applicable semantics for the BSDL attributes  
8 defined by the AC\_EXTEST extension. The form of the syntax used is defined in IEEE Std  
9 1149.1b-1994.

10 NOTE 1 – See IEEE Std 1149.1b-1994, “Lexical elements of BSDL” and “Notes on syntax definitions” for  
11 the conventions used herein to describe the parsing requirements for BSDL.

12 NOTE 2 – Syntactic items are shown surrounded in “< >” brackets when referenced in this text. Many of  
13 these items will be defined here, but some will be adopted from IEEE Std 1149.1b-1994. Those that are  
14 adopted will be underlined to indicate their source.

15 When an AC\_EXTEST extension exists in the extension area of a BSDL description, it must have  
16 the structure shown here. The various attributes, both mandatory and optional must appear in a  
17 prescribed order and not be intermixed with other statements.

18 NOTE – These other statements include BSDL attributes, attributes for other BSDL extensions and general  
19 VHDL constructs.

### 20 **7.4.1 Specification**

#### 21 **Syntax**

```
22     <AC_EXTEST Extension> ::=
23         <AC_EXTEST pin behavior description>                (see 7.5.1)
24         <AC_EXTEST Frequency Ref description>              (see)
25
```

#### 26 **Rules**

27 a) The syntax for an <AC\_Exttest Extension> as it appears in the extension area of a BSDL  
28 description shall be that shown above.

29 NOTE – The attributes must appear in the order shown above.

#### 30 **Permissions**

31 b) An <AC\_EXTEST Extension> may appear anywhere in the extension area of a BSDL  
32 description, subject to any rules defined by other extensions as to ordering.

33 NOTE – If more than one extension exists, an <AC\_EXTEST Extension> may appear before or after any of  
34 them within the limits of their definitions.

### 35 **7.4.2 Description**

36 The two mandatory attributes of an <AC\_EXTEST Extension> must appear in the order shown.  
37 No other statements may be intermixed within the extension, as the syntax above specifies. This  
38 extension may coexist with a number of other extensions.

### 39 **7.4.3 Keywords for AC\_EXTEST BSDL**

40 This subsection lists the keywords of AC\_EXTEST BSDL. These keywords are in addition to the  
41 reserved words of BSDL and VHDL. (See “BSDL reserved words” and “VHDL reserved and  
42 predefined words” in IEEE Std 1149.1b-1994.)

1 AC\_EXTEST\_Pin\_Behavior  
2 AC\_EXTEST\_Frequency\_Ref  
3 cycles  
4 seconds

## 5 **7.5 BSDL Attribute Definitions**

6 The mandatory and optional attributes needed to describe the ISC properties of a device are given  
7 in the remainder of this section. They must appear in the order given in 7.4.1.

### 8 7.5.1 Attribute AC\_EXTEST\_Pin\_Behavior

9 The mandatory AC\_EXTEST\_Pin\_Behavior attribute is used to enumerate those system pins of a  
10 component that are “AC” pins, per rule xx, and have been provided with AC\_EXTEST  
11 capability.

#### 12 7.5.1.1 Specification

13 Syntax

14 <AC EXTEST pin behavior description> ::= **attribute AC\_EXTEST\_Pin\_Behavior**  
15 **of <component name> : entity is <AC pin string> ;**  
16 <AC pin string> ::= " <AC pin list> "  
17 <AC pin list> ::= <AC pin> { , <AC pin> }  
18 <AC pin> ::= <port ID>

19  
20 Rules

- 21 a) The syntax for the mandatory AC\_EXTEST\_Pin\_Behavior attribute shall be that shown  
22 above.
- 23 b) The value of <port ID> shall contain a <port name> declared in the logical port  
24 description for the device.

25 NOTE – A <port ID> may consist of a <port name> or a <subscripted port name> as described in  
26 “Commonly used syntactic elements” in IEEE Std 1149.1b-1994. See also “Logical port description  
27 statement” in that standard.

- 28 c) The value of <port ID> shall refer to a system pin only and not to any pin that is a scan  
29 port signal or a compliance port pin; further, the <pin type> of the <port name> shall not  
30 be “linkage”.

#### 31 7.5.1.2 Description

32 The AC\_EXTEST\_Pin\_Behavior attribute can refer to individual system pins as <subscripted  
33 port name> elements or as <port name> elements that refer to individual system pins or  
34 collections of system pins.

35 Example

36 **attribute AC\_EXTEST\_Pin\_Behavior of ACDEV : entity is**  
37 **"Enable, Data\_bus, Cntl(2), Cntl(1), Addr\_bus" ;**  
38

## 1 8 Test Application

2 An AC Boundary-Scan test consists of a sequence of “test frames” applied by serially shifting  
3 commands and data into the TAPs and Boundary-Scan registers of the chips on a board or  
4 system. A given test frame for AC EXTEST will look identical to one for (DC) EXTEST, with  
5 the only exception being that the AC EXTEST instruction is executed:

6 On the board being tested:

7 1. {board level preparation}

8 On all chips:

9 2. Load SAMPLE/PRELOAD into all chips that will participate in EXTEST (either AC  
10 or DC) testing.

11 3. UPDATE\_IR: make SAMPLE/PRELOAD operational.

12 4. SHIFT\_DR: load all Boundary Registers with driver data for first frame of testing  
13 (both AC and DC).

14 5. UPDATE\_DR: transfer test data to update latches of Boundary Register.

15 6. SHIFT\_IR: load AC EXTEST instruction into all chips that possess it, and ordinary  
16 (DC) EXTEST into all other chips participating in the test.

17 7. UPDATE\_IR: make EXTEST instructions (AC or DC) operational: {describe what  
18 happens in both AC and DC EXTEST ICs.}

19 8. RUN-TEST/IDLE: {If needed, what happens here...}

20 9. CAPTURE\_DR: Those input pins that possess the AC capability {capture the bits  
21 transmitted via the transfer protocol.}

22 10. SHIFT\_DR: scan new frame data into the Boundary Registers while scanning out the  
23 captured data from the current frame for analysis.

24 11. UPDATE\_DR: for the new frame, {set up new transfer of data.}

25 12. Until there is no more frame data, go to step 8.

26 13. If the last frame has been executed, the last capture step will capture its results that  
27 must be shifted out. The data shifted in is "don't care" data and can be chosen from  
28 the "safe" bits specified in BSDL.

29 When a defect causes {no test signal} to be detected (as is the case for many defects), the  
30 {receiver} circuit must output a deterministic and consistent value. Upon execution of multiple  
31 test frames expecting different values from the receiving Boundary-Scan registers, the defect will  
32 result in one or more of the frames failing in certain bit locations.

33 Once all the frame result data is collected, failure analysis using well-known Boundary-Scan  
34 diagnostic routines can be done. One item must be considered however. Since a single data cell is  
35 used to initiate a data transfer over a differential pair but two cells (that capture positive and  
36 inverted copies of this data) receive this data, diagnostic routines that are unfamiliar with  
37 differential signaling may need to be improved to recognize this.

38