Draft Standard for Boundary-Scan Testing of Advanced Digital Networks

Prepared by the AC EXTEST Working Group of the Test Technology Standards Committee of the IEEE Computer Society

Abstract: This standard augments IEEE Std 1149.1 to improve the ability for testing differential and/or AC coupled interconnections between Integrated Circuits on boards and systems.

Keywords: AC Coupled Signals, Boundary-Scan, Differential Signaling, Interconnect Testing

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Introduction

(This introduction is not part of this standard.)

The development of this standard was begun May 21, 2001 by an ad-hoc industry Working Group called by Agilent Technologies and Cisco Systems. This group formulated this draft standard, with the intention of handing it over to the IEEE for formal standardization when the underlying technology became understood.

The group adopted as its mission:

To define, document and promote a means for designing ICs that support robust Boundary-Scan testing of boards where signal pathways make use of differential signaling and/or AC coupled technologies. This technology utilizes and is compatible with the existing IEEE 1149.1 standard. The goal is to upgrade the capabilities of IEEE Std 1149.1-2001 to maintain the rapid and accurate detection and diagnosis of interconnection defects in boards and systems despite the fault masking effects of differential signaling and the DC blocking effects of AC coupled signaling.

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1 Overview

1.1 Scope
This document describes the details of a solution for testing differential and/or AC-coupled nets between integrated circuits on printed circuit boards or in systems. Traditionally, such interconnect has been DC-coupled and can thus be tested with well-known Boundary-Scan methods, specifically with the EXTEST instruction as codified in IEEE Std 1149.1-2001. However, the use of AC-coupling technology disallows DC-based techniques, and differential signaling can cause fault masking effects, giving rise to the need for an extension of Boundary-Scan into the AC and differential realms.

1.2 Organization of the Standard
Clause 1 provides an overview and context for this standard.
Clause 2 provides references necessary to understand this standard.
Clause 3 defines terminology used in this standard.
Clause 4 outlines the technologies addressed and utilized by this standard.
Clause Error! Reference source not found. discusses the on-chip resources needed for testing.
Clause 6 provides rules for implementation.
Clause 7 provides rules for conformance and documentation of devices designed to this standard.
Clause 8 shows how this standard is used in typical testing applications.

1.3 Context
Figure 1 shows a printed circuit board containing many types of devices. Of these, some could be compliant with IEEE Std 1149.1 for the support of testing activities. These devices contain Boundary-Scan testability circuitry which allows them to participate in manufacturing tests that detect and diagnose faults such as open solder joints, shorts and missing devices.
The additional testability elements added by this standard to these same ICs allow this interconnect testing to be conducted on differential signal pathways and/or where AC coupling (which blocks normal DC test signals) has been used on signal paths between ICs.

1.4 Objectives
The objective of this standard is to provide design guidance for testability circuitry added to an IC in addition to testability provisions specified by IEEE Std 1149.1, such that when such an IC contains differential signaling and/or is AC coupled with other ICs compliant to this standard, board and system level tests can be readily and accurately conducted.
Devices that adhere to this standard that are used in differential and/or AC coupled signaling environments will realize significant savings in testing costs for boards and systems. Tools that are cognizant of the capabilities provided by this standard will be able to prepare, run and interpret these tests in a highly automated fashion, with high diagnostic resolution.
This standard allows devices created by multiple vendors to operate together during testing despite the differing characteristics and parameters of the IC processes used to fabricate the devices.

This standard also provides design guidance to board and system designers that will enhance the performance of the testability features of their products. This in turn will reduce system and production costs.

Figure 1: A printed circuit board containing a variety of components interconnected by printed wiring. Some ICs contain IEEE 1149.1 features that support Boundary-Scan interconnect testing.
2 References

This document shall be used in conjunction with the following standards. When the following standards are superseded by an approved revision, the revision shall apply.

3 Definitions and Acronyms

In the following definitions, defined terms appear in **bold font**.

### 3.1 Definitions

**AC Coupling:** The use of series capacitance in a *signal path*. This coupling will block DC voltages on the drive side of the path from appearing on the receive side. Only the AC component of the driven signal will pass through the coupling, with the effect of high-pass filtering imposed on the original signal. *Contrast with DC coupling.*

**NOTE** – AC coupling may also be accomplished with transformers. While the principles used in this document can be applied to transformer coupling, this coupling technology is not often used and is thus ignored to simplify discussion.

**Bias:** A high impedance (typically >1000 ohms) voltage source often used on the input of a receiver to cause it to output a deterministic state in the absence of an input signal, and/or to select the common mode voltage seen by a *differential receiver* in AC coupled signal paths.

**Bias network:** A network of impedances, usually higher-valued than *termination* impedances, used to establish a common mode or reference voltage.

**Channel:** A *signal path* or set of signal paths that transmits a single data stream from a source to a destination. See *differential signaling* and single-ended signaling.

**Characteristic Impedance:** the ratio of the complex voltage and complex current of a signal traveling forward on a conductive path. A signal path is often terminated with an impedance that matches the characteristic impedance of the path. This makes the path appear to be infinitely long and prevents signal degradation due to reflections that occur at unterminated ends of the path. See *termination*.

**Common mode noise:** A noise signal added equally to both signal paths in a differential signal channel. Common mode noise will affect or completely disrupt a single-ended measurement of a signal on one leg of a *differential receiver*, yet this receiver will accurately recover the signal within the noise.

**Common mode range:** The range of common mode voltage that a differential receiver is capable receiving while maintaining reliable signal recovery. A differential signal with common mode voltage within this range will be received correctly. Outside this range the receiver may fail to recover the data signal.

**Common mode voltage:** The offset from ground of the mean of the maximum and minimum voltages that appear on a pair of differential signals. A *differential driver* will, by it operational characteristics, define a common mode voltage. A *differential receiver* will properly receive data over a range of common mode voltages, but will likely have an optimal common mode voltage where its performance is best. When the optimal common mode voltage of a receiver is significantly different than that of its associated driver, AC coupling can be used to match the two components of a differential *signal path*. 
Comparator: An amplifier with two inputs labeled positive and negative, typically with very high input impedance. The amplifier usually has very high gain and produces an output signal that is the amplified difference of the positive and negative input signals. For all but the smallest differences, the output will be \( V_{\text{max}} \) or \( V_{\text{min}} \), which are the most positive and most negative voltages the amplifier can produce on its output. A comparator can be used as a differential receiver. A comparator can be used to determine if an input signal is logically above or below a reference voltage.

Current signaling: A signal encoded by the amplitude and direction of current flow. In a differential pair, a current signal is positive when current flows from positive to negative legs, and negative in the reverse direction. The voltage that may appear on these same legs does not carry information. Contrast with voltage signaling.

DC Coupling: The use of simple wires or small series resistances in a signal path. Contrast with AC coupling.

Derived voltage reference: a voltage reference derived from: 1) other references, such as a resistive divider between power and ground, or 2) a resistive divider between two differential signals that recovers the common mode voltage of the signals.

Differential driver: A driver that accepts a single data stream and drives it onto two independent signal paths where one signal is the inverse of the other. The two signals are centered at the common mode voltage.

Differential receiver: A receiver that recovers a single data stream encoded differentially on two signal paths. It effectively subtracts the signal on its negative leg from that on its positive leg. This eliminates common mode noise appearing on both legs.

Differential signaling: The use of two independent signal paths in a channel to carry a single data signal, where one path carries an inverted copy of the signal that appears on the other path. The original data signal can be reconstructed by taking the difference of the two signals and there is no reliance on a reference voltage for determining this signal. This has the property of eliminating common mode noise in the transmitted signal. Contrast with single-ended signaling.

Encoding protocol: A stream of data bits may be encoded into a new (typically longer) data stream that has characteristics favorable for its transmission on a channel. The encoded stream may have added redundancy to support error correction. The encoded stream may have extra bits added to deliberately increase the number of transitions that appear in the stream, effectively raising its apparent frequency and facilitating data transmission that encodes clocking information into the stream.

Frequency: The maximum number \( f \) of transition pairs that occur on a signal path expressed in Hertz (cycles per second). With respect to AC Coupling, a frequency is high when the period \( 1/f \) is small compared to the time constant of the coupling. A frequency is low when the period is large compared to the time constant of the coupling. The frequency appearing
on a signal path may vary greatly over time as a function of the data being transmitted and the data encoding protocol.

**Float:** The input to a receiver that is connected to an undriven signal, or a high impedance connection to a receiver input, is said to float.

**High pass filter:** An electrical network that passes higher frequencies and attenuates lower frequencies. DC current is blocked.

**Hysteresis:** From magnetics: lagging in the values of resulting magnetization in a magnetic material (such as iron) subjected to a changing magnetizing force. In this document, hysteresis refers to the memory of an input state to an amplifier or buffer after that state is removed but before a different input state is applied. Typically there is a hysteresis threshold that defines the difference between “no input” and “input.” As applied to electronics, a digital output circuit such as a comparator where the output switches to one output state when the input is above one level and switches to the opposite output state when the input is below a lower level, and the output does not switch at any intermediate level. Example: a buffer produces a high output when a voltage above 0.5 volts is applied, produces a low output when a voltage below 0.3 volts is applied, and does not change its output for voltages between 0.3 and 0.5 volts.

Hysteresis symbol in a buffer symbol:

```
[Diagram of hysteresis symbol]
```

**Hysteretic:** Adjective form of hysteresis, as in “hysteretic amplifier.”

**Interconnect test:** An IEEE Std 1149.1 Boundary-Scan test designed to detect and diagnose defects in the interconnection wiring between ICs. This standard extends the concept to include the testing of channels, where single-ended and differential signaling, and DC or AC coupling may exist.

**Load termination:** A termination placed at the far end (away from the driver) of a signal path used to match the characteristic impedance of the path. Contrast with source termination.

**Low pass filter:** An electrical network that passes lower frequencies, including DC levels, and attenuates higher frequencies.

**Mission logic:** The circuitry inside an IC that performs its primary design function. See test logic.

**Mission mode:** A device or pin of a device performing its primary design function. Contrast with test mode.

**Negative leg:** The signal path of a differential signal pair that has the opposite polarity as the original data signal.

**Null:** The input state where the two inputs to a differential receiver which are supposed to be different (complementary) are instead receiving the same value.
Offset voltage: A constant DC voltage added to an AC signal.

Operational modes: A device or pin of a device may operate in one of two modes, see mission mode and test mode.

Positive leg: The signal path of a differential signal pair that has the same polarity as the original data signal.

Reference voltage: A low impedance voltage source typically used to define a threshold for comparing signals. The low impedance characteristic means it is resistant to conducting noise signals.

Referenced termination: A termination for a differential channel where the two legs are both terminated to a reference voltage.

Self-referred comparison: The comparison of a signal with a delayed version of the same signal, used to detect signal transitions. This process does not need a static reference voltage to find a transition in a signal.

Signal Path: An electrical pathway formed by a simple conductor, or a terminated pathway containing a series resistance, or an AC coupled pathway containing a series capacitance, that transmits a signal from a driver to a receiver.

Signal reflection: A signal wavefront traveling across a discontinuity in the characteristic impedance of the signal path may have a fraction of its energy reflected in the opposite direction on the path. The reflection may be of the same or opposite polarity and will add into the waveforms appearing on the path, impacting their shape. See also transmission line.

Single-ended signaling: The use of a single signal path in a channel to carry a data signal. The signal is referenced to a static reference voltage. Contrast with differential signaling.

Slew rate: Rate of change in either direction of voltage in a specified time, measured in units of volts per second.

Source termination: A termination placed near the source driver of a signal, to satisfy DC current requirements of a driver and/or to match the characteristic impedance of a transmission line structure to reduce signal reflections. Contrast with load termination.

Termination: An impedance usually near the end of a signal path used to satisfy the electrical matching requirements of the characteristic impedance of the signal path and reduce signal reflections. The impedance is typically low, often 100 ohms or less. See also characteristic impedance, referenced termination, source termination, load termination and unreferenced termination.

Test logic: Testability logic defined by this standard and IEEE Std 1149.1. Contrast with mission logic.

Test mode: A device or pin of a device that, in response to the EXTEST or AC_EXTEST instruction, is now driving and/or receiving test data as controlled by the test logic of the IC. It has been disconnected from the internal mission logic of the IC. Contrast with mission mode.
Time constant: Typically the product of resistance and capacitance of an RC network (e.g., a high pass filter) measured in seconds. One time constant is the time for a capacitor to discharge 63% of its voltage through a resistor. In AC coupled systems, the termination resistance combined with the coupling capacitor forms a high pass filter.

NOTE – In discussions comparing time periods to time constants, a period is significantly longer (shorter) than a time constant if it is five (one-fifth) times the time constant value. For example as shown in Figure 2 using the five-time-constant rule, a signal will decay to 0.7% of its original value. The one-fifth-time-constant rule means that 81.9% of a signal still remains.

Figure 2: Signal decay versus time in units of time constants.

Transition: A voltage transition occurs when a signal traverses a specified voltage range in a specified time in either direction. See slew rate.

Transmission line: A signal path with a specific construction that produces a uniform, known characteristic impedance along its length. This minimizes degradation of a signal passing along this path that can result from impedance variations.

Unreferenced termination: A termination for a differential channel where a termination impedance is connected between the two legs with no connection to a reference voltage.

Voltage signaling: Signals are encoded by the voltage appearing on a wire compared to a reference voltage (single-ended) or the voltage appearing on a pair of wires (differential). Contrast with current signaling.

3.2 Acronyms

CML: Current mode logic

HSTL: High-Speed Transceiver Logic

LVDS: Low Voltage Differential Signaling

LVPECL: Low voltage PECL (Pseudo Emitter Coupled Logic)

PECL: Pseudo Emitter Coupled Logic

TAP: Test Access Port (from IEEE Std 1149.1).
4 Technology

The presence of coupling capacitors on chip interconnects, whether they are discreet devices mounted on a PC board or integrated inside an IC, prevents DC values from being driven between chips. An AC Boundary-Scan methodology must therefore use a time-varying signal to pass through the AC coupling when in AC EXTEST mode.

Differential signaling is often used to increase signaling speeds and noise immunity, compared to single-ended coupling. Differential signaling, combined with termination schemes, can have significant defect masking properties that reduce test effectiveness.

4.1 Signal Pin Types

It is expected that a chip possessing pins requiring AC coupling may also possess “normal” (i.e., DC coupled) pins as well. These DC pins would supply data and/or control to/from portions of the chip that do not require AC coupling. For test purposes, it is necessary that all these pins be tested simultaneously with an EXTEST-like capability because that is how shorts (unwanted connectivity) between these pins are reliably detected. This document will refer to DC and AC pins henceforth. DC pins are those that IEEE Std 1149.1 currently governs for testing. AC pins have been treated by 1149.1 as an "analog" problem and effectively ignored.

AC pins are a principle target of this standard. IC designers implementing this standard are expected to identify such pins and add new test capabilities for them.

4.2 Signal Coupling and Coupling Combinations

This section reviews a range of coupling options.

4.2.1 Single-ended DC

A basic, single-ended connection scheme is shown in Figure 3, along with the Boundary-Scan control and observation capability specified by IEEE Std 1149.1. This type of coupling has been quite common and is very testable using Boundary-Scan.

Figure 3: Basic single-ended signaling with Boundary-Scan control and observation.

It is important to note that in a standard Boundary-Scan test, the time between launching a signal from a driver (at the falling edge of TCK in the Update-DR or Update-IR TAP controller state) and capturing that signal (at the rising edge of TCK in the Capture-DR TAP controller state) is no less than 2.5 TCK cycles. Further, the time between successive launches on a driver is governed not only by the TCK rate, but by the amount of serial data shifting needed to load the next pattern data in the accumulated Boundary Registers of the Boundary-Scan chain. Thus the effective data rate of a driver could be thousands of times lower than the TCK rate. For DC coupled
interconnect this time is of no concern. For AC coupled interconnect, the signal may easily decay partially or completely before it can be captured. If only partial decay occurs before capture, that decay will very likely be completed before the next edge is produced by the driver.

4.2.2 Single-ended AC

Figure 4 shows an AC coupled single-ended connection. (The termination resistor and voltage source shown may not be necessary thus would be omitted.) While the devices may have been designed for DC coupling and actually contain Boundary-Scan resources, the AC coupling will block their operation. This interconnection configuration is thus untestable with standard Boundary-Scan algorithms. This is due to Boundary-Scan test data rates being relatively low since they are a function of the test clock (TCK) rate which may be significantly lower than the normal operating frequency of the channel being tested. The data seen by the receiver may decay before it can be captured.

Figure 4: Basic single-ended signaling with AC coupling.

In general, AC coupling can distort a signal transmitted across a channel depending on its frequency. For example, Figure 5 shows a channel transmitting a high and low frequency waveform. The high frequency signal is relatively unaffected by the coupling. The low frequency signal is severely impacted. First, it decays to $V_T$ after a few time constants. Second, its amplitude is double the input amplitude. A key item to note is that the transitions in the original signal are preserved, although their start and end points are offset compared to where they were in the high frequency case.

Figure 5: High and low frequency response of an AC coupled channel.

4.2.3 Differential DC

Figure 6 shows a basic differential DC coupled signal path. The termination resistor may exist for impedance matching and/or source termination of the driver. The placement of Boundary-Scan resources is optional per IEEE Std 1149.1 in that they can be omitted altogether. The 1149.1 standard allows a designer to designate the differential signal path as “analog”. Then the digital-to-analog and analog-to-digital interfaces (optionally) can be provided with Boundary-Scan
resources as shown in Figure 6. When this option is taken, it is then possible to test the “analog”
signal path with Boundary-Scan algorithms. In this case the signal path is viewed by the test
logic as if it were single-ended, leading to diagnostic ambiguity.

Figure 6: Basic differential signaling with DC coupling and source loading.

The driver in Figure 6 could be producing a voltage signal and the resistor is used to match the
signal line impedance. Alternatively, the driver could be producing a current signal, where the
direction of flow represents data, and the resistor is needed not only to match signal line
impedance, but also to provide a DC current path to satisfy the driver’s requirements. This is
called a source termination.

The driver in Figure 6 is looking into a termination $R_S$ and transmission lines with characteristic
impedance $R_S$ as well. This forms a voltage divider which sends $\frac{1}{2}$ the signal into the
transmission lines. When the signal wavefront reaches the receiver (after delay $d$) its high
impedance does not match the characteristic impedance which reflects the signal back down the
lines to the receiver. This signal ($1/2$ the driver voltage) adds to the signal received so that the
receiver perceives a full voltage swing. After the second transmission line delay $d$, the reflected
signal reaches the driver and brings the voltage seen there to the full level. Thus a clean transition
is seen at the receiver, but the signal seen at the driver is a two-step staircase. Since there is an
impedance match at the driver, no new reflections occur.

In the case where the impedance $R_S$ is moved to the receiver, (to the right of the transmission
lines) this is called load termination (and the resistor is renamed $R_L$) as shown in Figure 7. Now
the driver is looking into the transmission lines with characteristic impedance $R_L$. The full
waveform is transmitted (no divider is now present) and this edge propagates to the receiver. At
the receiver the termination resistor matches the line impedance, and thus there is no reflection.
The waveforms at both the driver and receiver are full transitions.

Figure 7: DC coupled driver and receiver with load termination.

Figure 8 shows a driver/receiver pair that has been both source and load terminated. In this case
the voltage swing seen on both sides of the transmission line has been divided by two (note $R_S$,
equals $R_L$). This type of termination assures that in the case of an imperfect impedance match, the resulting reflections can be attenuated at both ends of the line.

![Figure 8: DC coupled driver and receiver with both source and load termination.](image)

4.2.4 Differential AC

Figure 9 shows AC coupling of a voltage driver and receiver that could be completely incompatible for DC coupling because the voltage levels used by the driver are too far removed from the acceptable common mode range of the receiver. The termination network referenced to the common mode voltage source $V_T$, along with the DC blocking effect of the coupling capacitors, allows this configuration to work properly. This enforced compatibility is a common reason why board designers may use AC coupling.

NOTE 1 – The receiver waveforms in Figure 9 will decay to $V_T$ if the driver frequency is low compared to the time constant of the coupling network. Since Boundary-Scan test data application rates can be low, the receiver may indeed see null levels due to signal decay.

NOTE 2 – It is assumed in Figure 9 that the distance between $R_L$ and the receiver inputs is small, such that there are no significant transmission line effects beyond $R_L$.

![Figure 9: A basic differential AC signal path with load termination and common mode generation.](image)

Figure 10 shows a basic differential AC signal path with an unreferenced termination. The termination is used for impedance matching. The driver is a voltage driver and thus does not need a source termination to provide a current path.

![Figure 10: A basic differential AC signal path with unreferenced termination.](image)

Figure 11 shows a basic differential AC signal path with a current driver and source termination, and also a referenced bias generator to select the common mode voltage appropriate for the
receiver. The source termination may also serve as an impedance match for the line. The bias
network may use significantly larger resistors as long as the line distance from the capacitors to
the receiver is small. This will significantly increase the time constant of the coupling network.

Figure 11: Basic differential AC signal path with source termination and bias provision.

Finally, all the terminations, bias networks and even the coupling capacitors may ultimately be
integrated into the receiver IC. Externally, the signal path appears to be DC coupled but internally
it is still AC coupled, as shown in Figure 12. On-chip component defects will not need to be
tested during board test. Thus only the interconnect defects (typically solder) will be relevant.

Figure 12: AC coupling, termination and bias generation internal to the ICs.

4.2.5 Intention: When AC Capability Is DC Coupled

The standard for AC EXTEST proposed herein is intended to be implemented on AC pins of an
IC. However, there is the possibility that a board designer may still choose to use DC coupling
between devices that are DC compatible. Thus a test developer could find a situation where AC
EXTEST is needed to test a DC coupled signal path. This could occur when more than one AC-
capable interface exists on an IC and one is AC coupled while another is DC coupled. The test
developer would need to load the AC EXTEST instruction into the device to test the AC coupled
interface. It is the intention of this standard that if DC coupling of AC-capable interface is
possible and gives acceptable mission performance, then the AC EXTEST test performance will
also be acceptable.

Figure 13: An AC-capable receiver connected to an AC-capable driver and a conventional driver.

For example, in Figure 13 a conventional IC (TX1, containing only EXTEST support) is DC
coupled to a receiver in RX. An AC-capable driver TX2 is also connected to the receiving IC. To
test all the signal paths simultaneously, the conventional device TX1 must be in EXTEST while
the other two use the AC EXTEST instruction. See a summary of capture behaviors for various coupling and testing scenarios given in section 4.9.

### 4.3 The Effects of Defects

Defects are abnormalities in the structure of a board that occur during manufacturing that must be found and corrected. This “manufacturing defect” model includes things like open solder joints, shorts, missing components and dead devices. Not included in this model are performance-related issues, for example, the failure of a device to operate at its highest specified frequency at –40 degrees. This recognizes the traditional role of IEEE 1149.1 as a test standard for manufacturing defects.

The advent of AC coupling, especially in the differential signaling domain, threatens this role. There is inherent redundancy in differential structures that can mask the presence of seemingly obvious defects. An example is shown in Figure 14.

![Figure 14: An AC coupled differential path containing a defect (A) and an equivalent circuit (B).](image)

In this case, the positive leg of the circuit is eliminated by a defect, for example, an open solder joint on the capacitor. Yet the receiver still receives the negative leg signal and compares it to the $V_{\text{ref}}$ voltage. The receiver will still produce the correct output, although its common mode noise rejection capability is completely compromised. This might not be noticed until subsequent functional or performance testing is encountered. There it may show up as an elevated bit error rate which would not provide very much diagnostic information. This simple example illustrates why it is important to monitor both legs of a differential pair, as covered in section 4.5.4.

One defect in particular may be troublesome to detect in AC coupled structures: the shorted capacitor. This defect restores DC coupling. This defect may go unnoticed particularly in differential signal paths, especially when the DC characteristics of the driver and receiver are similar. For this reason, it is important to support the standard EXTEST instruction, because it can be used to test for shorted capacitor defects. This can be done by supplying a stream of 0s and 1s to the driver side of the capacitor and showing that this stream does not show up on the receive side.

Finally, it is important to realize that defects that occur in high-speed circuits (where slew rates are often faster than signal path transmission times) there may be transmission lines that affect the circuit’s faulty behavior as shown in Figure 15. Simulation of the circuit’s behavior may be necessary to understand the effects of defects. It is important to consider transmission lines as components of the simulated model when slew rates are elevated.
4.4 Differential Termination and Testability

Extensive study of differential channels and the effects of defects within those channels has shown that the effects of defects are heavily influenced by the termination schemes used. There are three functions of terminations:

- to provide for proper DC paths needed for proper driver functioning, (usually source termination),
- to provide impedance matching of transmission lines, and
- in some AC coupled cases, to set common mode operating points for the receiver.

A given termination may provide one or more of these functions. The following subsections discuss termination options.

4.4.1 Unreferenced Termination

Source termination is usually needed for current signaling technologies, where the direction of current flow is used to encode binary data. A typical example is a Low Voltage Differential Signaling (LVDS) driver/receiver pair. Since all differential receivers operate by comparing voltages, a current signal is translated into a voltage signal for that comparison. Figure 16 shows an LVDS driver DC coupled to a voltage receiver, where \( R_S \) provides both source termination and impedance matching. The direction of current flow represents data.

NOTE – It is assumed that \( R_S \) is placed very close to the receiver so that any transmission line effects are only present between the driver and the resistor.

This form of termination is called unreferenced because there is a single resistor \( R_S \) rather than two resistors center tapped to a reference voltage (seen later in Figure 18). In effect, the receiver is referenced to the common mode voltage of the driver/resistor combination. This means the receiver’s common mode range must be compatible with the driver’s output.
Figure 16: LVDS driver and receiver, DC coupled.

Figure 17 shows an unreferenced AC termination. Resistor $R_S$ still provides source and line termination. Resistor $R_L$ provides termination and a current path on the receive side, since the comparator input impedance is effectively infinity. Note $R_L$ and $C$ determine the time constant of this coupling.

Figure 17: LVDS driver and receiver, AC coupled with unreferenced termination on the receive side.

NOTE – The receiver in Figure 17 will have its own biasing circuitry built in to establish its common mode operating point.

If the time between signal transitions is long, the voltage across $R_T$ will decay to zero volts, or a null input condition with results that may be undefined. Note that some defects can also cause this
to occur, such as either capacitor C missing. A null input condition during testing is undesirable
due to its non-determinism and the ways it can interact with defects (see 4.3). Because of this,
unreferenced termination is not preferred even though it saves one resistor.

4.4.2 Referenced Termination

Figure 18 shows an AC coupled, referenced termination. This type of termination is used to set
the common mode voltage of the receiver at its optimal value (here, $V_T$). Resistors $R_B$ along with
capacitance C determine the time constant of the coupling. The value of $R_B$ may be larger, simply
providing bias and a larger time constant, or may be smaller to provide both bias, load impedance
matching and a smaller time constant.

Figure 18: LVDS driver and receiver, AC coupled with referenced termination on the receive side.

In the referenced termination case, if a defect such as a missing capacitor is present (this defect is
shown in Figure 14) the leg with the missing capacitor will see $V_T$ while the other leg will see a
valid signal. (The unreferenced case presented both legs with a null condition.) Since test
structures are to be added to both legs (see 4.5.4) they will respond in a deterministic way. This is
the preferred behavior of an AC coupled link.

4.5 Test Signal Implementation

In order to test the various combinations of single-ended and differential signal paths with
variations on coupling, modifications have to be made to the drive and receive sides of the path.

4.5.1 Single-ended Drive

Figure 19 shows a single-ended output stage modified in the familiar way given by IEEE Std
1149.1 for test purposes. One of two signals, the normal mission signal or test data are selected
for transmission by a mode signal. (This figure does not show the full detail of the Boundary-
Scan register cells that supply test data.) The test data is either the content of the Update Latch
(U) when executing the (DC) EXTEST instruction, or a “Test Signal” when the AC EXTEST
instruction is loaded into the device. The test signal is an AC waveform suited for transmission
through AC coupling. (See section 5.1.) The concept here is that the single-ended driver itself is not modified.

![Diagram of a single-ended driver path.](image)

**Figure 19:** A single-ended driver path.

### 4.5.2 Differential Drive

There are two options for implementing a differential driver when incorporating test. The first is shown in Figure 20 where the selection between test and mission data is performed before the conversion to differential signaling. This means there will be only one data stream presented to the two differential pins and that the data will be transmitted in true differential form, using either current or voltage modes of the driver in question. Due to aggressive performance requirements in some higher-speed driver designs, it is expected that this option will often be chosen.

![Diagram of a full differential driver for both mission and test modes.](image)

**Figure 20:** Full differential driver for both mission and test modes.

![Diagram of a differential mission/single-ended test mode driver.](image)

**Figure 21:** Differential mission/single-ended test mode driver.

A second option for implementing testability in a differential driver is shown in Figure 21. In this case the mission mode signal path is differential, while in test mode the mission driver is disabled and two single-ended drivers with independent test data sources are enabled. Each controls a single side of the differential signal path. During test, the path is now a pair of independent
single-ended signals. The two new single-ended test drivers must have similar drive characteristics as the mission driver to assure they are compatible with the loading and coupling that the mission driver would encounter.

NOTE 1 – In describing this case in BSDL (see section 7.2) the test mode of the driver signals are described which are single ended. Thus the signal pair is not described as differential. (See the “Grouped Port Identification” section B.8.8 in IEEE Std 1149.1-2001.)

NOTE 2 – If such a device supports IEEE Std 1149.4, then the structure in Figure 21 may be implemented, but with drivers of insufficient drive capacity to drive the load impedance. In this case, a hybrid of Figure 20 and Figure 21 may be implemented where AC EXTEST operates using the model in Figure 20. This option has desirable testability and diagnosibility features in that it removes some of the redundancy inherent in differential signaling, but it also reduces some of the noise immunity that differential signaling affords and may generate more noise during testing since the test signals on the two legs are no longer balanced and offsetting. There is additional cost in that the drive specifications (slew rate and amplitude) for the two added drivers must be substantially similar to those of the mission driver, into the mission load. There may be unacceptable mission performance degradation with this approach that makes it the less commonly chosen option.

4.5.3 Single-ended Test Signal Reception

Figure 22 shows two options for single-ended test signal reception, again familiar from IEEE Std 1149.1, but with a provision for detecting an AC test signal when the AC EXTEST instruction is loaded in the device. When AC EXTEST is loaded, a specialized test receiver (see 4.6) digitizes the test signal seen at the input and a detector block (Det) determines if this represents a ‘0’ or ‘1’. When EXTEST is loaded, the mission signal is passed to the Boundary Register cell. One option shown in Figure 22 supports INTEST (control and observe capability) and the other uses a simpler observe-only structure that will not support INTEST.

NOTE – The test receiver may be connected to the output of the mission input amplifier if it is a true amplifier (e.g., unity gain) rather than a threshold comparator. The test receiver is intended to process the actual waveform seen at the input pin, not an interpretation of the waveform.

A single-ended receiver has some form of reference used to distinguish a ‘0’ from a ‘1’ and this feature is used during (DC) EXTEST as well. However during AC EXTEST, the signal may decay to some intermediate value that cannot be reliably received by the mission receiver. The test receiver is used to sense the AC test signal.

4.5.4 Differential Test Signal Reception

A differential receiver is modified for testability as shown in Figure 23. The mission differential receiver path is modified to capture test data seen by the mission receiver in differential mode. The mission receiver itself is unmodified.
NOTE – As shown, the mission receiver path supports INTEST, but an observe-only structure can be used instead if INTEST is not supported.

Each leg of the differential signal path has its own added test receiver. The purpose of this receiver is to monitor a leg of the signal path independently. This gives additional defect detection and diagnosis capability.

NOTE – No variations in the test receiver are needed for INTEST support since this is an observe-only monitor.

On each leg, in addition to the test receiver, there is a fixed threshold comparator (called the “EXTEST comparator”) that compares the input waveform with a reference $V_T$, to produce a logical interpretation of the input. This is used for EXTEST-based testing. The value of $V_T$ is set to the optimum common mode point of the mission receiver, which is the same as a referenced termination would use.

The EXTEST comparator is designed to produce a deterministic output when presented with a null input (both legs at the same voltage). When this receiver is AC coupled to a driver the EXTEST instruction, when run at a low enough testing rate to fully discharge the coupling capacitors, will not be able to capture the driven data, and will thus see a null condition. This will be captured as a deterministic value. If a defect such as a shorted capacitor exists, then one of two effects will be seen:

- if the driver levels bracket the value of $V_T$, the driven data will be captured via the EXTEST comparator rather than a static value, or
- if the driver levels are both above or both below the value of $V_T$, then a static value will be produced by the EXTEST comparator that may or may not match the null default value.

**Figure 23: Differential signal reception, with and without support for the INTEST instruction.**

This is an unapproved draft, subject to change, published for comment only.
These facts are useful for detecting shorted coupling capacitors. An EXTEST-based interconnect test can be constructed that causes the drivers to produce a stream of data and expects the AC coupled receivers to register a known constant value if the capacitor is not shorted.

NOTE – If the driver levels do not bracket the value of $V_T$, then depending on the default value picked for a null input, the shorted capacitor may produce the same value and thus not be detected. The choice of the default value should be considered with respect to possible driver technologies that might be AC coupled to this receiver to attempt to avoid this.

When this receiver is DC coupled to a driver and the EXTEST instruction is executed, then one of two effects will be seen:

- if the driver levels bracket the value of $V_T$, the driven data will be captured, in other words, the drive levels are “close enough” to the optimum common mode voltage of the receiver to register as data via the EXTEST comparator, or
- if the driver levels are both above or both below the value of $V_T$, then a static value will be observed by the EXTEST comparator, respectively a ‘1’ or ‘0’.

Thus, interconnects between DC coupled differential ICs may or may not pass data when performing EXTEST. It is probable that the fact they are DC coupled indicates they will pass EXTEST data. Test generation tools should examine the logic family information of the two ICs to determine if this will happen.

NOTE – Logic family information is not included in the definition of BSDL and must come from other data sheet sources.

Since the signals on a DC coupled differential pair may contain a significant common mode offset as well as the test signal, the design of the AC EXTEST test receiver must account for the fact that there is no fixed reference available to discriminate a ‘0’ from a ‘1’. A general discussion of the test receiver is given in sections 4.6 through 4.8, and rules for its implementation are given in section 6.5.

### 4.6 Test Receiver Support for the AC EXTEST Instruction

The principle purpose of the test receiver seen in Figure 22 and Figure 23 is to extract a test signal that may contain an offset. Because of the offset, a simple comparison of the test signal to a static reference may not reliably extract the test signal. Using the opposite leg of the pair as a reference (as is done by the mission receiver) will often mask important defects. A solution is to look for information contained in the transitions of the signal. These will be independent of the offset seen in Figure 24. Valid transitions have a defined voltage swing $\Delta V$ and slew rate $\Delta t$.

![Figure 24: A signal with unknown voltage offset and the signal transitions it contains.](image-url)
One way to find the transitions in a signal with an unknown offset is to compare the signal with a delayed version of itself, that is, to use its recent history as a reference. This is diagramed in Figure 25. The original signal, a delayed version and the output of the hysteretic comparator are shown. The output is a faithful reconstruction of the original waveform, delayed by the time it takes for the input waveform to pass the hysteresis threshold. The output waveform has been converted to standard logic levels, that is, the unknown offset is removed.

![Figure 25: Delayed self-referenced reconstruction of a DC coupled input waveform with unknown voltage offset.](image-url)

It will be important to assure that the delay $D$ is longer than the transition times to be sensed. The use of hysteresis (the hysteresis offset) can eliminate unwanted response to small signal noise (runt pulses). Additional filtering in the design of the comparator (the hysteresis delay) can eliminate response to larger signal noise of insufficient duration (noise spikes).

The waveforms that are applied to the test receiver may or may not be AC coupled to the driver. When AC coupled they may or may not decay significantly depending on the coupling time constant. In the case in Figure 25 the test receiver is either DC coupled or AC coupled with a very long time constant. If AC coupled signals with periods long with respect to the coupling time constant are applied to this simple circuit, the decaying signals will cause the comparator to reset itself early (after delay $D$) in response to the delayed reference edges and the reconstructed waveform will differ from the original.

A low pass filtered delay solves this problem as shown in Figure 26. The simple low pass filter with a filtering time constant of $R_F C_F$ is used to hold the reference input to the test receiver at a constant value that is largely unaffected by short term events such as the high-pass filtered edges seen when AC coupling (low time constant) is used. If high time constant AC coupling, or DC coupling is used, then the low pass filter adjusts the reference point again to represent near term history of the input signal. The hysteresis offset and hysteresis delay are used to control response to noise.

To summarize the concepts shown in Figure 26, the test receiver reconstructs an original waveform driven from either a single-ended driver or one leg of a differential driver, that is either AC or DC coupled, and is insensitive to DC offsets that may exist in the driven waveform. It does this by responding to the edges of the original waveform that are still present despite DC or AC coupling.
Figure 26: Delayed and filtered self-referenced waveform reconstruction of both DC and AC coupled waveforms by a test receiver.

Figure 27 shows one possible implementation of the concept shown in Figure 26. There are two simple comparators, one to sense rising edges and the other to sense falling edges. The $V_{\text{Hyst}}$ voltage sources set the hysteresis offset for the comparators. The internal delay of the comparators determine the hysteresis delay. The comparator outputs set or clear a D-type flip-flop. The values of $R_F$ and $C_F$ are chosen to cause a delay longer than the expected transition times being sensed.

Figure 27: A simple test receiver implementation possibility for the concept in Figure 26.
NOTE 1 – Typical values of $R_F$ and $C_F$ might be 5 Kohms and 5 picofarads which could be integrated into an IC.

NOTE 2 – The input waveform at point A may be high-pass filtered by AC coupling, or it could be a normal DC coupled digital waveform (with an unknown offset). In either case, the edges are used to reconstruct the original digital waveform.

NOTE 3 – The D-type flip-flop element can be initialized by the Update clock to establish a known initial state at the time the drivers are triggered. The initialization value will be discussed later.

Figure 28 shows an AC coupled differential signal channel from the drive side, done differentially, to the receive side which is single-ended for test purposes. (The mission receiver has been omitted for clarity.) This supports the AC EXTEST instruction.

Figure 28: Differential driver, AC coupling, and receiver testability structure.

NOTE – In Figure 28 the mission receiver has not been shown. It would include load termination that would determine the time constant of the AC coupling.

### 4.7 Test Receiver Support for the (DC) EXTEST Instruction

The test receiver behavior for AC EXTEST has been described. However it also is important to support the standard (DC) EXTEST instruction. This amounts to “turning off” the edge integrating capability of the test receiver and having it respond only to levels. This is further complicated by the problem that there may be common mode offsets added to the signals. This necessitates choosing a reference voltage that can be used for single-ended comparison.

One choice is to use the internal bias voltage $V_{bias}$ used to set the $V_{Com}$ point of the mission receiver (the “sweet spot”) as shown in Figure 29. This bias voltage will work well as a static
reference for the test receivers when AC coupling is used. If the receiver IC is DC coupled to the
driver, then the test receiver may or may not receive data depending on whether $V_{Bias}$ is between
the high and low values driven by the driver. If data is not received, the test receiver will perceive
a constant logic value, either 1 or 0.

![Static reference](image)

**Figure 29: Static reference used to support (DC) EXTEST. Comparators are sampled just before the
rising edge of TCK in the Capture-DR state.**

If the test receiver is responding to the EXTEST instruction but the receiver is AC coupled to the
driver, there is the chance, particularly if the coupling time constant is longer, that the receiver
will respond to a change in the driven data (see waveforms in Figure 29). The flip-flop is clocked
in the Capture-DR state to set a default initial state. If there is a DC level on the test receiver
input, this will override the clocking of the initial state. If the levels have decayed due to AC
coupling, then the initial state will not be overridden. Extra time for signal decay can be inserted
by spending time in the Run-Test/Idle state.

### 4.8 A General Test Receiver for DC and AC EXTEST Instructions

A test receiver that supports both the AC and (DC) EXTEST instructions is required. This could
be accomplished simply by taking the two structures already shown and selecting between them
with multiplexers. However it is possible to merge their behaviors into a more efficient structure
as shown in Figure 30. In this structure an analog multiplexer selects between (DC) EXTEST
support and AC EXTEST support.
4.9 Boundary-Scan Capture Data Versus Configuration

The content of Table 1 shows what Boundary-Scan data will be captured by a test receiver for various combinations of coupling, DC compatibility and whether a given IC is executing EXTEST or AC EXTEST.

Editor's Note: Because we haven’t yet decided on the data protocol being used, the info in Table 1 below contains some “protocol dependent” fields that will be filled in when we pick a protocol.
Table 1: Boundary-Scan capture results for various combinations of coupling, test instruction and driver-to-receiver DC compatibility.

<table>
<thead>
<tr>
<th>Coupling</th>
<th>Driving IC</th>
<th>Receiving IC</th>
<th>Test Instruction loaded in:</th>
<th>Capture result when DC levels of driver and receiver are:</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC</td>
<td>EXTEST</td>
<td>EXTEST</td>
<td>AC EXTEST</td>
<td>Data (Note 1)</td>
<td>Typical test for DC coupling</td>
</tr>
<tr>
<td>AC</td>
<td>AC EXTEST</td>
<td>AC EXTEST</td>
<td>AC EXTEST</td>
<td>Protocol Dependent (Note 3)</td>
<td>AC on DC coupled paths may be forced by board topology.</td>
</tr>
<tr>
<td>AC</td>
<td>AC EXTEST</td>
<td>AC EXTEST</td>
<td>AC EXTEST</td>
<td>Protocol Dependent</td>
<td>Edge based approach will not get its “throat cleared” because driver is in EXTEST. May transmit data but there is a noise issue.</td>
</tr>
<tr>
<td>DC</td>
<td>AC EXTEST</td>
<td>AC EXTEST</td>
<td>AC EXTEST</td>
<td>Protocol Dependent (Note 3)</td>
<td>Edge based approach will transmit data</td>
</tr>
<tr>
<td>AC</td>
<td>AC EXTEST</td>
<td>AC EXTEST</td>
<td>AC EXTEST</td>
<td>Protocol Dependent</td>
<td>Used to test shorted capacitances. Will pass data (a failure) or will register a (possibly passing) fixed value.</td>
</tr>
<tr>
<td>DC</td>
<td>AC EXTEST</td>
<td>AC EXTEST</td>
<td>AC EXTEST</td>
<td>Protocol Dependent</td>
<td>Typical test for AC coupling.</td>
</tr>
<tr>
<td>AC</td>
<td>AC EXTEST</td>
<td>AC EXTEST</td>
<td>AC EXTEST</td>
<td>Protocol Dependent</td>
<td>Edge based approach will not get its “throat cleared” because driver is in EXTEST. May transmit data but there is a noise issue.</td>
</tr>
<tr>
<td>DC</td>
<td>AC EXTEST</td>
<td>AC EXTEST</td>
<td>AC EXTEST</td>
<td>Protocol Dependent</td>
<td>With edge based approach, may be used to test shorted capacitators.</td>
</tr>
</tbody>
</table>

NOTE 1 – In Table 1, “data” indicates Boundary-Scan data is successfully transmitted.

NOTE 2 – “Fixed 0 or 1” indicates the incompatible levels will be seen as either a 1 or 0 depending on where the receiver threshold is set.

NOTE 3 – “Protocol Dependent” indicates the signaling protocol will determine the result (TBD). In some cases data may be transmitted. In other cases the result is nondeterministic.

NOTE 4 – “Default” indicates the response is the same that a floating test receiver would produce.
4.10 Noise Sources and Sensitivities

Editor's Note: The following section will discuss the sources of noise, how the Test Receiver is sensitive to noise, and how to avoid susceptibility. This will offer guidance to IC designers, board designers, and test engineers. Rules that appear in later clauses will specify Test Receiver noise characteristics relative to the mission mode of the system. Not clear if we can impose rules on board designers or test engineers.

4.10.1 Noise Sources that Affect Mission Operation
Ground bounce, signal coupling, EMI

4.10.2 Noise Sources Unique to Testing
Intra-IC noise generation (lobotomy effect), rogue signals on the board, impedance mismatches

4.10.3 Noise Sources Exacerbated by Testing
Ground bounce, signal coupling

4.10.4 Avoiding Noise
Hysteresis offsets, hysteresis delay, self-reference filtering, use of the Run-Test/Idle state, noise rejection of the data protocol, limits on ATPG
5 AC EXTEST Signaling Protocol

5.1 The AC Test Signal

5.2 Driver Test Structure

5.3 Receiver Test Structure

5.4 On-Chip Coupling and Termination

5.5 Boundary-Scan Cells

5.5.1 Cell Architecture

5.6 TAP

The TAP modifications are straightforward. An AC_EXTEST instruction must be added.
6 Implementation Specifications

6.1 General Implementation

6.2 Input Test Receivers

All AC input pins are equipped with test receivers. The IC designer will design the mission performance of the input to accept some range of voltage changes and slew rates. The rules given below assume that an input will respond to a minimum input voltage change and that the slew rate of input changes will be at or above some minimum, because AC coupling is anticipated or even built into the IC itself. These minimums are defined by the performance requirements of the mission of the IC and are depicted in Figure 31 for both AC and DC coupled signals.

![Diagram of input test receivers showing minimum input swing and transition times for waveforms presented to the test receiver using either DC or AC coupling.]

The minimum input swing, termed $\Delta V_{\text{Min}}$, is the smallest change in voltage that is considered a reliable data transition by the designer of the mission receiver. The time $T_{\text{Trans}}$ is the maximum amount of time this minimum input swing is expected to take. Signal transitions that take longer than $T_{\text{Trans}}$ are not considered valid. For example, the decay on a capacitively coupled signal that was actively driven high but is slowly decaying to zero is not a valid falling transition.
NOTE – If the transition times of rising and falling edges are different, then the longer of the two is defined as the maximum.

The offset voltage shown in Figure 31 may vary depending on different circuit configurations. For example, an IC with an input pin possessing a test receiver may be AC or DC coupled to a driver intentionally by a board designer. Depending on which is chosen, there could be different offsets observed at the test receiver. When a defect occurs, the coupling may be affected. For example, a shorted coupling capacitor may institute DC coupling to a receiver.

The value of $T_{\text{Test}}$ is the minimum time between signal transitions that can be caused by Boundary-Scan testing. This value is governed by test-related parameters such as TCK frequency and time spent in the Run-Test/Idle TAP controller state.

When AC EXTEST is in effect, it is the purpose of the test receiver to reconstruct the test waveform driven by the upstream driver when either AC or DC coupling is used. It does this by reacting to the edges and not the levels of the input waveform. When DC EXTEST is in effect, the test receiver behaves as a level detector.

6.2.1 Rules

a) All AC pins that receive input data, whether they are single-ended or part of a differential pair, shall have a test receiver attached to the pin.

NOTE – This rule applies to input and bidirectional pins. See also permission 6.2.2a).

b) When the AC EXTEST instruction is loaded, the test receiver shall respond to signal transitions that are greater then 70% of the minimum input swing ($\Delta V_{\text{Min}}$) and shall not respond to signal transitions that are less than 30% of the minimum input swing.

NOTE 1 – See rules e), f) and g) below for further definition of the meaning of “respond”, and rule c) for additional requirements on the validity of signal changes. Rule d) governs the measurement of signal transitions.

NOTE 2 – This rule establishes the hysteresis offset $V_{\text{Offset}}$ of the test receiver and provides bounds on its range.

NOTE 3 – The range between 30% and 70% is the target for a designer to set a trip point for test receiver response and allows for significant margin. See recommendation 6.2.3b).

NOTE 4 – This rule applies to signal transitions within any common mode or fixed voltage range definition of the mission of the pin. Changes outside of this range may not cause a test receiver response. For example, a signal transition that turns on input protection diodes would be outside the normal operating range of the receiver.

c) When the AC EXTEST instruction is loaded, the test receiver shall respond to valid signal transitions defined in rule b) above only when the new signal level persists for at least a minimum period of time called the hysteresis delay, and this delay period shall be chosen by the designer by considering recommendation 6.2.3a).

NOTE 1 – The hysteresis delay time is denoted by $T_{\text{Hyst}}$.

NOTE 2 – If the signal change does not persist long enough (for example, it is a short noise pulse) the hysteresis delay will suppress the receiver’s response to it. This gives the test receiver two methods for ignoring noise. The hysteresis offset will ignore small-amplitude noise and the hysteresis delay will ignore large-amplitude pulses of insufficient duration.

NOTE 3 – There may also be a propagation delay in the test receiver. This time is not included in the value of the hysteresis delay. This delay should be small compared to the hysteresis delay.
d) When the AC EXTEST instruction is loaded, the test receivers shall determine the amount of input swing by comparing the instantaneous voltage on a pin to the recent average of the voltage on the pin, determined by a method equivalent to that given in recommendation 6.2.3c).

NOTE – See Figure 26 (page 26) for an example of one way to do this comparison.

e) In response to a valid signal transition as governed by rules b), c) and d) above, the test receiver shall output a one when the signal transition is a rising transition and it shall output a zero when the signal transition is a falling transition.

NOTE 1 – There may also be a nominal propagation delay in the test receiver.

NOTE 2 – The signals representing one and zero are chosen by the IC designer.

f) After a valid signal transition as governed by rules b), c) and d) above occurs, a test receiver shall continue to produce the same output until the next valid signal transition occurs.

g) If a test receiver has not received a valid signal transition as governed by rules b), c) and d) above, it shall produce a default output of either a one or zero.

Editor's note: The treatment of “default output” is yet incomplete as it is dependent on how we implement the signaling protocol.

h) When an AC input pin is AC coupled to a driver, the time constant of the effective high-pass filtering of the coupling shall be no less than 15 (fifteen) times the value of the hysteresis delay $T_{Hyst}$.

NOTE 1 – This time constant is denoted by $T_{HP}$. The driver is expected to produce edges that meet or surpass the minimum input swing ($\Delta V_{Min}$) within time $T_{Trans}$. These edges will pass through this coupling virtually unchanged. This rule assures the subsequent decay will be much slower than a valid signal edge so it will not be confused with a valid signal transition, as depicted in Figure 31.

NOTE 2 – When the AC coupling is implemented on a board rather than inside an IC, the IC designer shall communicate to the board designer this minimum time constant required for AC coupling.

NOTE 3 – In practical design examples, the value of $T_{HP}$ will usually be much larger than this minimum. The resistive component of the time constant may be determined by the characteristic impedance of the channel. The capacitive component is selected after this constraint is considered.

i) The time constant of the low-pass filter given in recommendation 6.2.3c) shall be no less than 8 (eight) times the value of $T_{Hyst}$.

NOTE – This time constant is denoted by $T_{LP}$.

j) Tools that perform tests shall assure, when the AC EXTEST instruction is in effect in any IC participating in those tests, that the time between subsequent test data changes ($T_{Test}$) is no less than 3 (three) times the low-pass filter time constant ($T_{LP}$) of any IC.

Editor's note: I expect some debate on this rule. It intends to assure that the recent history of a signal is not influenced by the recent history of the test!

k) When the (DC) EXTEST instruction is loaded, the test receivers shall determine the logic value on the pin by comparing the current voltage plus (minus) the hysteresis offset $V_{Offset}$ on the pin to a fixed threshold voltage and shall output a zero (one) if the voltage compares greater (less) than this threshold.

Editor's note: If we decide we do not need hysteresis during DC EXTEST (potentially making the test receiver more complex) we will need to delete the next 2 rules and fix a few figures.
NOTE 1 – See Figure 29 (page 28) for an example of one way to do this comparison.

NOTE 2 – The IC designer may choose a threshold value at the midpoint of a voltage swing deemed optimal for the mission receiver. This may be the same voltage used to bias the mission receiver when it is AC coupled as seen in Figure 12 (page 16).

l) When the (DC) EXTEST instruction is loaded, the test receiver shall sample and hold (in the hold state memory) the logic value of the DC level of the pin on the falling edge of TCK in the Capture-DR TAP controller state.

NOTE – See also rule m) below for the case where the DC level on the pin does not have a logic value. This occurs when the level is not above or below the test receiver’s static threshold value (used during (DC) EXTEST) by an amount exceeding the hysteresis offset.

m) When the (DC) EXTEST instruction is loaded and there is no logic level on a pin at the falling edge of TCK in the Capture-DR TAP controller state, the initial value of the hold state memory in the test receiver shall be preserved.

Editor’s note: The treatment of “hold state memory” is yet incomplete as it is dependent on how we implement the signaling protocol.

NOTE – This rule states what must happen when an AC coupled signal decays before the sample time.

6.2.2 Permissions
   a) A test receiver may be isolated from its pin with a linear buffer as long as it is still seeing the actual waveform appearing on the pin.

6.2.3 Recommendations
   a) The amount of hysteresis delay $T_{Hyst}$ should be chosen by the designer to reject common noise sources such as ringing or over/undershoot that may occur on a signal pin.

NOTE – For example, if the hysteresis delay is set to 5 times the value of $T_{Trans}$, this will allow the receiver to ignore typical ringing that may occur on transitions. The designer should contemplate the nature of noise sources that may impact signals received at a pin when choosing the hysteresis delay. (See section 4.10.)

   b) For better small amplitude noise immunity, the value of $V_{Offset}$ should be set closer to the high limit.

   c) The “recent average” of a signal may be generated with a low-pass filter.

6.2.4 Description
Given a model of the basic test receiver circuit that uses high-pass coupling and low-pass filtering to generate a self-referenced edge detector (one half shown in Figure 32) the effects of the rules given in section 6.2.1 are plotted in Figure 33 for a single rising edge transition.
Figure 32: Model with recurrence equations for a portion of test receiver circuitry. The comparator has hysteresis delay. The hysteresis offset has been omitted.

Voltage at A = Input Stimulus
Voltage at B (VB) = VA - VC
Current through RC (IRc) = VB / RC
Current through RF (IRf) = (VB - VC) / RF

Figure 33: Relationships of key delay times and time constants given by rules in section 6.2.1 for the detection of a rising edge.

Figure 33 shows the output of the non-hysteretic comparator in Figure 32 to illustrate the effects of the selected time constants and offsets for a single rising edge, on that portion of circuitry devoted to detecting a rising edge. Rule 6.2.1b) gives the two horizontal lines for 30% and 70% input voltage swings. The worst case is the 70% swing. Given a signal with a valid rising edge
with rise time $T_{\text{Trans}}$, the output of the high-pass filter will decay as shown. There must be, by rule 6.2.1c), a hysteresis delay $T_{\text{Hyst}}$ where the comparator does not respond. The time constant $T_{\text{HP}}$ of decay due to the high-pass filter must be no less than 15 times the value of $T_{\text{Hyst}}$. However, due to the low pass filtering (set to no less than 8 times the value of $T_{\text{Hyst}}$), the decay of the difference signal is faster, as shown. The choice of multipliers (8 and 15) assure that the minimum time that the voltage difference exceeds 70% of the minimum input swing is significantly greater than the hysteresis delay. If the either or both multipliers are increased, this minimum time will increase. If the hysteresis offset is decreased from 70%, the minimum time will increase. Finally, if the circuit is DC coupled (equivalent to an infinite coupling time constant) the minimum time will increase.