

# AC Extest Tools Tiger Team Report

July 13, 2001

## Evaluation of Proposals

- 1) The proposal is capable of what defect coverage? How much change is required to the test generation and tester software to achieve that coverage?

**Criteria:** The defect coverage for both AC and DC coupled nets should be the same as 1149.1 provides today (shorted, open, "stuck-at", etc.) on single-ended DC coupled nets, with little or no changes to existing PCB test generation and tester tools.

**Evaluation of Proposals:** We concluded that we should follow a data model, as opposed to error bits, for test generation. A data model views test data as being sent over a wire, where the captured data value at the receiver is the same value that was sent over the net by the driver -- under fault free conditions. This allows the test generation software to remain independent of the transport layer (as it is for DC today).

For defect coverage we concluded that tools would require the least amount of change where two separate detectors, i.e. one on differential each leg, were required on the receiver side. We would recommend a third "clobber" detector that monitors both legs. This would provide additional defect coverage, for example one leg open on the receiver where there is a termination across both legs (e.g., LVDS). Also, with this approach DC and AC nets can be tested together. This would seem to be best for coverage and there would not need to be separate AC/DC test vector sets. It should be noted that this assumes a single cell on the differential driver. We do not preclude a cell on each leg of the driver (if deemed feasible by the designer), essentially making the nets single ended for AC Extest.

- 2) The proposal is capable of what diagnostic resolution? How much change is required to the test generation and tester software to achieve that resolution?

**Criteria:** Provide diagnostic capability to the failing net(s) and potential defect type(s), with little or no change to existing PCB test generation and tester tools.

**Evaluation of Proposals:** The data model, separate receive cells on each input of the differential receiver and optional clobber monitor (as in 1 above) would provide the best diagnostic resolution and have the least impact on tools. This would provide diagnosis to the failing net.

The caveat here is that the failing values may not necessarily be as expected with existing DC tests. For example, a stuck-at one may be captured as a zero on the + leg of the receiver. So tools should not depend on the values captured in failing cells for diagnosis of stuck conditions.

- 3) The proposal will have what impact on test time?

**Criteria:** The presence of AC\_EXTEST devices should not appreciably increase the interconnect test time. AC-coupled and DC-coupled, Single-ended and differential nets should all be testable concurrently.

**Evaluation of Proposals:** We did not see any appreciable difference between the proposals here. We felt that the best test time would be achieved with concurrent testing of AC and DC nets. However, even with separate test of AC coupled nets, there would not likely be an impact due to test time

considering the entire board manufacturing flow/process. All proposals would be significant reductions in test time over using 1149.4.

- 4) Is the proposal backward compatible with 1149.1?

**Criteria:** Nothing in the proposal should break any traditional 1149.1 tools, methodology, or test. Changes to 1149.1 infrastructure required by AC\_EXTEST should be transparent to existing tools, and the tools should be able to safely ignore them with no penalty other than not achieving the new capabilities (enhanced defect detection for AC and differential signals).

**Evaluation of Proposals:** In order to support new AC Extest capability, all proposals would require tools to be modified. We broke this into two parts as follows.

- a) Backward compatibility of new AC Extest devices, with existing tools, for performing DC EXTEST. With current tools we do not see any problems doing DC Extest with any of the proposals, provided that new features are described by BSDL extensions that existing tools can ignore. One issue is with AC Control cells. Old tools would not understand how to control these without a modified BSDL. Also, we would expect that coverage would be affected since AC Extest would not be performed in this case.
- b) Compatibility with the 1149.1 methodology for extending the architecture to support AC Extest capabilities. All proposals follow prescribed methods to extend the 1149.1 architecture. The AC Extest control cell may be an issue with regards to BSDL. However, the tools group feels that this cell-by-cell control of AC/DC Extest operation is a required capability.

The group noted that the following items will require upgrade of testers and tester software to support AC\_EXTEST: topological analysis of nets with AC coupling capacitors; support for the single driver – dual receiver topology (may already be done); management of any separate test frequency (fg); use of the new AC\_EXTEST control cell; and reading new BSDL extensions.

- 5) Does the proposal require an AC test clock (frequency) source other than TCK? How is it provided?

**Criteria:** Current testers provide TCK in many ways, it may be free running, in bursts, stopped at arbitrary times and for arbitrary periods, have an arbitrary duty cycle, and run at different rates at different times. There should not be any dependency on TCK characteristics in order to support AC\_EXTEST.

It is preferred that any other clocks required for AC\_EXTEST, e.g. fg, should not have to be provided by the tester. These clocks should be free running, or controlled through 1149.1 infrastructure, and may be asynchronous to TCK. If a controlled AC test signal must be provided from the tester, a separate pin for a free-running signal is preferred.

**Evaluation of Proposals:** We agreed that there be no new requirements or restrictions placed on TCK over what 1149.1 requires today. This also applies to the frequency discrimination window. This means TCK would be allowed to stop or pause, and that very slow TCK rates (e.g., a bit-banged TCK from a parallel port) should be supported. If an edge counting approach is used, then it was felt that TCK could be used for the AC Extest frequency and that no new requirements would be required.

Beyond that, there did not seem to be a clear consensus from the group on this issue. When it came to having a separate fg, some were opposed to any extra pins or clocks. Some were opposed to requiring TCK to change on the fly in RTI, due to constraints in some existing testers.

- 6) Is compliance with the proposal verifiable from behavior at the chip pins? How much change is required to the test software to perform compliance verification?

**Criteria:** Compliance testing is currently done for 1149.1 by verification of behavior at the chip pins. This behavior is strictly defined by the rules, permissions and recommendations of the Standard, and not by the implementation examples. 1149.1 Compliance checking tools would have to be modified to support new AC\_EXTEST behavior, but any requirements for structural verification for AC\_EXTEST compliance would likely have a major impact on these types of tools.

**Evaluation of Proposals:** We concluded that there were no problems with compliance verification as long as the various circuits could be modeled as digital logic for simulation purposes. For compliance verification of the actual chip, there did not seem to be any problems with any of the proposals being verified from the chip pins.

- 7) Can the proposed structures be modeled as digital logic for verification (simulation)?

**Criteria:** Compliance verification tools, and simulation tools in general, require gate-level or RT-level simulation models, such as Verilog or VHDL. Any analog structures that could not be easily modeled with digital behavior would have significant impact on chip design and verification methodologies.

**Evaluation of Proposals:** See 6 above.

- 8) Does the proposal provide sufficient description in extended BSDL and a Package file for the new Standard to permit insertion tools to insert the test structures, and test generation tools to generate tests, and test and diagnostic tools to detect and resolve defects? How much change is required to these tools to read and use the BSDL extensions?

**Criteria:** There will probably be at least one new predefined instruction (AC\_EXTEST), probably some new standard boundary cell (BC\_x) definitions, and a new Package file that provides the CELL\_INFO data for both the new instruction and the new cells. There may be BSDL\_EXTENSION attributes also defined in the Package. None of this should break today's BSDL parsers and syntax checkers.

**Evaluation of Proposals:** The only issue from the proposals we identified was the addition of AC Extest control cells. Otherwise all proposals should be able to be described using BSDL extension attributes.

- 9) Are the proposed structures compatible with current chip manufacturing testers and test processes?

**Criteria:** What is the impact of AC\_EXTEST on production test of the chips. What needs to be tested, are there any analog testing requirements, are there any specific frequency testing requirements, etc. These issues have an impact on DFT for the chip, choice of chip manufacturing tester, cost of test, defect detection and test quality, and on ATPG tools.

**Evaluation of Proposals:** None of the proposals seemed to be incompatible with current chip tester capabilities. It was felt that (digital) chip testers could handle the required waveforms/encoding. The major concern here was whether or not the proposal would require analog circuit test. Requirements for very high-speed system clocks would also be of some concern.

- 10) Does the proposal provide sufficient requirements with sufficient flexibility for circuit designers to easily implement compliant analog portions of the structure?

**Criteria:** This standard may require some analog circuitry (typically included in the receiver I/O book). Implementation of this circuitry will have to be done for every type of interface and every technology. The requirements must be clear and yet provide flexibility to allow the designers to optimize their design.

**Evaluation of Proposals:** It was felt that the MSA proposal is not fully specified to permit implementation. Other proposals seem to provide sufficient information.

11) Are the proposed solutions compatible with current board manufacturing testers and test processes?

**Criteria:** What is the impact of AC\_EXTTEST on board test? Are there any testing requirements that would impact existing ICT or Boundary Scan testers? These issues have an impact on tester equipment capabilities, whether or not new testers will be needed and whether or not coverage/test quality will be affected.

**Evaluation of Proposals:** A major issue here is the capability of existing ICT equipment to provide AC Extest via the edge connector of the PCB. Testers would need to provide the driver/receiver waveforms to/from differential channels going to/from the card edge. It was not felt that current testers would be able to provide this capability and that would impact test coverage or tester design.